Analytical Study, Performance Optimisation And Design Rules For Customary Static And Dynamic Subthreshold MOS Translinear Topologies

Konstantinos I. Papadimitriou*, Alexandros Houssein, Emmanuel M. Drakakis**

Department of Bioengineering, Imperial College London, South Kensington Campus, SW7 2AZ, London, U.K.

Abstract

This paper aims to provide qualitative and quantitative answers to questions related to the impact of transistor-level design parameters upon the performance and accuracy of static and dynamic translinear (TL) circuits in subthreshold CMOS. A methodical, step-by-step, symbolic analysis, exploiting a simplified EKV-based approximation is performed upon customary static TL topologies, including the four MOS transistor (MOST) multiplier/divider, the squarer circuit and the alternating formation of a six MOST multiplier/divider. The logarithmic integrator is treated as a typical dynamic TL analysis example. The produced EKV-based symbolic analysis results are compared against the ideally expected behaviours and Spectre® - BSIM3V3 model - simulations. The satisfying agreement between the proposed EKV-based model and Spectre simulator allowed us to proceed further and investigate the conditions under which optimal behaviour is achieved. Optimisation techniques, based on MOSTs' geometrical parameters combinations, resulted in the articulation of practical design rules.

Keywords: EKV Model, Log-Domain Circuits, Optimisation, Subthreshold MOSFETs, Translinear Circuits

1. Introduction

In 1975, Gilbert introduced and articulated the Translinear Principle (TLP) in [1], which was originally formulated to be applied on circuits comprised solely of bipolar junction transistors (BJTs). Remarkably, early monolithic TL BJT implementations of analogue multipliers were available since the late 60's [2, 3]. However, the vast increase in commercial demand for VLSI and ULSI systems has resulted in the domination of MOSTs over BJTs, since the former demonstrate lower power-demand properties, in conjunction with smaller device area and an ever decreasing production cost per transistor.

In biomedical applications for example, where, in general, portability, wearability and implantability is sought after, analogue electronics need to consume as little power as possible, occupy minute chip area and operate with sufficient, for the specific application, accuracy. Therefore, for such applications, MOST weak-inversion (WI) operation is one of the preferred basic options. Within WI region, MOSTs exhibit their low power properties, are characterised by the maximisation of the g_m/I_D ratio (transconductance generation factor) and also comply with the TLP. The usefulness of subthreshold operation has been repeatedly illustrated in numerous publications in the literature. Recent, indicative, low-power biomedical examples include nonlinear cellular/molecular dynamics computation circuits [4, 5, 6, 7, 8] and linear, high-dynamic range, filtering

topologies [9, 10, 11, 12, 13, 14, 15, 16, 17]. The TLP is always one of the necessary, basic tools required for the mathematical description and subsequent implementation of such circuit topologies, thanks to the flexibility that it provides when it comes to the real-time realisation of linear or nonlinear mathematical operations [18].

A detailed analysis on subthreshold MOST-comprised TL circuits has been performed by Andreou and Boahen in [19], showing experimental data from topologies exploiting the logarithmic current-voltage relation of MOS devices operating in WI. Seevinck and Wiegink have proposed conditional generalisations of the TLP, which include MOSTs operating in strong inversion [20]. Recently Minch, inspired by Lopez-Martinez *et al.* [21] and based on the originally proposed TLP and a simplified version of the EKV model [22, 23], succeeded in tailoring the TL formalism and confirming its validity for all regions of MOS operation through chip measurements [24].

Commonly, the initial basic stages of the synthesis of a subthreshold TL circuit aimed at realising a specific operation are dictated by the ideal TLP relation stemming from the, ideally, exponential relation between drain current and gate-source voltage difference (assuming $V_{BS} = 0$). The later stages of the design process usually call for extended simulations, which lead to the empirical optimisation of the circuit. In practice, subthreshold MOST TL circuits are often required to operate in such a manner that the instantaneous magnitudes of two (or more) transistor currents involved in the operation of the TL loop may vary considerably (by one order of magnitude or more, e.g. [13]), which suggests that for given device aspect ratios, certain devices may instantaneously migrate from the weak to the moderate inversion region, when asked to process very large,

*Corresponding author

**Senior corresponding author

Email addresses: kp2509@imperial.ac.uk (Konstantinos I. Papadimitriou), e.drakakis@imperial.ac.uk (Emmanuel M. Drakakis)

for their size, currents. This, in turn, means that the ideal expression for the TLP (the well-known pristine equality of transistor currents) is violated, at least instantaneously, since certain of the loop transistors momentarily fail to comply with the exponential law, in accordance with interpolating “*all regions of operation*” models treated in detail in [24, 25, 26]. Interesting measured and simulated examples of how large currents processed by WI MOST TL circuits affect operation and performance can be found in [16, 27].

With the above borne in mind, certain questions arise naturally: How is the operation and performance of a given WI TL circuit (whose topology is synthesised in compliance with the ideal TLP relation) affected for different device sizes and current magnitude levels, when deviations from the ideal exponential device relation are taken into consideration? Based on the results of such a detailed transistor-level analysis, how can the accuracy of the operation of such a circuit be optimised and how can its deviation from the ideal operation be mitigated? This paper aims at providing such a MOST-level detailed analysis, shedding light on the associated technical trade-offs and proposing practical design rules for the optimal configuration of TL circuits.

The paper is structured as follows: Section 2 presents the ideal and EKV-based models of MOST subthreshold operation. In Section 3, generic types of static and dynamic TL circuits are analysed following both approaches. In particular the following circuits are analysed: a) a 4 MOS multiplier / divider (stacked formation), b) a squarer topology, c) a 6 MOS multiplier / divider (alternating formation) and finally d) a 1st order low-pass Log-domain filter. Section 4 proceeds with the comparative presentation of the mathematical analysis results (both for the ideal and the EKV-based case) and simulated results obtained from the Cadence Design Framework (CDF). Triggered by the aforementioned counter-intuitive simulation results, Section 5 and Section 6 are introduced. Section 5 provides a mathematical insight on how the level of inversion of subthreshold MOST TL circuits is affected by their geometrical parameters. Section 6 discusses practical optimisation guidelines for the fundamental TL circuits already shown in previous sections both in a qualitative and quantitative manner. This paper concludes with Section 7, where a brief but analytical insight regarding the culminating EKV-based design rules is offered.

2. MOS Transistor Models

A physical device can be termed “*TransLinear*” if the current through the device and its transconductance exhibit a linear relation. In other words, a two, three or four terminal device, whose current density is an exponential function of its control voltage, can be defined as a TL element [18]. In the case of a MOST, the control voltage that produces the drain current is the potential difference between the channel surface ψ_S and the source or drain terminal. The drain current of a MOST in WI is a function of these two factors:

$$I_D = \frac{W}{L} I_{D_o} \exp\left(\frac{\psi_S - V_{SB}}{V_T}\right) \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (1)$$

where ψ_S is a function of the bulk and gate voltage of the device ($\psi_S = \mathcal{F}(V_G, V_B)$), V_T is the thermal voltage ($\approx 26mV$ at 300K) and $[W/L]$ denotes the aspect ratio of a MOS device [19]. The drain current of a MOST can be also approximated by semi-empirical expressions that provide more than acceptable results [24]. Such a typical expression valid for all regions of inversion is the EKV interpolation model [25, 26, 28] defined below:

$$I_D = \frac{W}{L} \mu C_{ox} (2n) V_T^2 \left\{ \left[\ln\left(1 + e^{(V_P - V_{SB})/(2V_T)}\right) \right]^2 - \left[\ln\left(1 + e^{(V_P - V_{DB})/(2V_T)}\right) \right]^2 \right\}, \quad (2)$$

with μ , C_{ox} and n denoting the effective surface mobility, total oxide intrinsic capacitance and the slope factor ($1/k$), respectively. The quantity V_P defines MOST’s pinch-off voltage [25]. From (1) and (2), two current-voltage expressions can be derived that will help us analyse the following static and dynamic TL circuits. For all types of circuits treated in the paper, it has been assumed that the devices used are NMOS transistors, in deep saturation, i.e. $V_{DS} \gg 4V_T$. A similar analysis holds for PMOS devices.

2.1. Ideal Equations Approach

Based on the capacitor divider model, the surface potential ψ_S of a MOST can be described by the relation: $\psi_S = (C_{ox} V_{GB}) / (C_{ox} + C_{dep}) = k V_{GB}$, where C_{dep} is the depletion layer capacitance between the surface and its substrate [19]. Since deep-saturation operation has been assumed, the dependence on the drain potential can be ignored, thus, (1) can be re-written as:

$$I_D = \frac{W}{L} I_{D_o} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \exp\left(\frac{(n-1)V_{BS}}{nV_T}\right), \quad (3)$$

with $I_{D_o} = \mu C_{ox} (2n) V_T^2 \approx 260nA$ for an NMOS in AMS 0.35 μm technology [26, 28, 29]. From (3), two expressions for the drain current of a MOST and consequently for its control voltage V_{GS} can be derived, depending on the potential of the bulk terminal of the device with respect to the source terminal. Both expressions are shown below:

When $V_B = 0$:

$$V_{GS_j} = V_{TH} + (n-1)V_{S_j} + nV_T \ln\left[I_{D_j} / (I_{D_o} [W/L]_j)\right] \quad (4)$$

When $V_{BS} = 0$:

$$V_{GS_j} = V_{TH} + nV_T \ln\left[I_{D_j} / (I_{D_o} [W/L]_j)\right], \quad (5)$$

with j indicating the transistor index inside the TL loop.

2.2. EKV-Model-Based Approach

The deep saturation MOST operation assumption been made, allows us to safely ignore the second exponential term of (2) [24, 26, 28]. Moreover, for design purposes, from [25, 26, 28], the voltage V_P can be approximated by $V_P \approx (V_{GB} - V_{TH})/n$, therefore, relation (2) can be re-expressed as:

$$I_D = I_{D_o} \frac{W}{L} \left\{ \left[\ln\left(1 + e^{(V_{GB} - V_{TH} - nV_{SB})/(2nV_T)}\right) \right]^2 \right\}. \quad (6)$$

As in the ideal case, depending on the voltage relation between the source and bulk terminals, two different expressions can be derived for the control voltage V_{GS} . When $V_B = 0$ we can rewrite (6) as:

$$\ln\left(1 + e^{(V_G - V_{TH} - nV_S)/(2nV_T)}\right) = \sqrt{\frac{I_D}{I_{D0} \left[\frac{W}{L}\right]}}. \quad (7)$$

By exponentiating both sides of (7), yields:

$$e^{(V_G - V_{TH} - nV_S)/(2nV_T)} = e^{\sqrt{\frac{I_D}{I_{D0} \left[\frac{W}{L}\right]}}} - 1. \quad (8)$$

Taking the natural logarithm of both sides of (8) gives:

$$V_{GS} = V_{TH} + (n-1)V_S + 2nV_T \ln(e^X - 1), \quad (9)$$

where $X = \sqrt{I_D/(I_{D0} [W/L])}$. Clearly, the dimensionless quantity X is the square root of the inversion coefficient (IC), which defines the region of operation for a MOST (When in WI, $IC \ll 1$; When in MI, $IC \approx 1$; When in SI, $IC \gg 1$) [25]. Moreover, the exponential term of (9) can be expanded in a McLaurin series:

$$e^X - 1 = \frac{X}{1!} + \frac{X^2}{2!} + \frac{X^3}{3!} + \dots + \frac{X^n}{n!} \quad (10)$$

and bearing in mind that in WI (even close to MI), the IC is ≤ 1 , it is safe to approximate $e^X - 1$ with the first two terms of the series, i.e. $X + X^2/2 = X(1 + X/2)$ and transform (9) into:

$$V_{GS} = V_{TH} + (n-1)V_S + 2nV_T \ln(X) + 2nV_T \ln(1 + X/2).$$

Furthermore, based on the previous assumption regarding the range of X , the term $(1 + X/2)^2 \approx (1 + X)$ and the V_{GS} relation finally becomes:

When $V_B = 0$:

$$V_{GS_j} = V_{TH} + (n-1)V_{S_j} + nV_T \ln(X_j^2) + nV_T \ln(1 + X_j) \quad (11)$$

When $V_{BS} = 0$:

$$V_{GS_j} = V_{TH} + nV_T \ln(X_j^2) + nV_T \ln(1 + X_j). \quad (12)$$

3. Analysis Of Translinear Circuits Based On The Ideal And The EKV-Based Approach

In this section indicative generic, often used static and dynamic TL blocks will be analysed mathematically, using both the ideal and the EKV-based expressions for V_{GS} , derived in Section 2. More specifically, relations (5) and (12) will be exploited, since for the presented circuits the assumption that $V_{BS} = 0$ has been made. The selected circuits realise both linear and nonlinear relations between their input and output currents. Applying KVL along them, we derive and compare their input/output current relations, generated by both approaches (ideal and EKV-based) and detail their differences. Finally, hence forth, the aspect ratio parameter $[W/L]$ is substituted for the parameter α , for reasons of compactness; thus, $[W/L]_j = \alpha_j$.

3.1. Static Translinear Circuits (STL Circuits)

3.1.1. A 4 MOS Multiplier/Divider TL Circuit

We start our analysis by studying a classic, generic STL block, the one-quadrant, stacked-formation multiplier/divider circuit shown in Figure 1. By applying KVL along the closed loop formed by the M_1-M_4 devices: $V_{GS_1} + V_{GS_2} = V_{GS_3} + V_{GS_4}$. Exploiting (5) and (12) and setting $I_1 = I_{IN}$, $I_3 = M$, $I_4 = I_{OUT}$, $X_j = \sqrt{I_j/(I_{D0} \alpha_j)}$ ($j = 1, \dots, 4$) and the ratio $I_2/I_3 = \lambda$ (consequently $I_2 = \lambda M$), a set of ideal and EKV-based expressions (13) and (14) is derived and tabulated in Table 1. When equal-sized devices and the ideal case is considered, then confirm from (13) that $I_{OUT} = \lambda I_{IN}$ and λ represents the circuit's gain or attenuation, depending on whether $\lambda \geq 1$ or $\lambda < 1$, respectively. Observe that the incorporation of the more complicated EKV model, leads to the introduction of additional terms (the 2nd and 3rd terms in (14)). These terms exhibit dependences on the (3/2) power of I_{IN} , I_{OUT} , λ and α_j ($j = 1, \dots, 4$). For given α_j , λ and M values, relation (14) expresses I_{OUT} with respect to I_{IN} in a perplexed form $\mathcal{F}(I_{IN}, I_{OUT}) = 0$, while the quantity $\sqrt{I_{OUT}}$ exhibits a cubic relation upon I_{IN} , α_j ($j = 1, \dots, 4$).

Figure 1: An one-quadrant, 4-NMOS multiplier/divider TL circuit. The bulk terminals of the NMOS devices are connected to the source, thus $V_{BS} = 0$. The dashed green line defines the closed TL loop, where KVL can be applied along.

3.1.2. Squarer TL Circuit

The nonlinear squarer block is shown in Figure 2. This block has been frequently used for the implementation of the square of an input current over a scaling current, expressed as I_O in this case. With the help of (5) and (12) and by setting the drain current of M_1 and M_2 as I_{IN} , the drain current of M_4 as I_{OUT} and $X_j = \sqrt{I_j/(I_{D0} \alpha_j)}$, $j = 1, \dots, 4$, a pair of ideal and EKV-based equations can be derived. From the ideal relation (15), $I_{OUT} = I_{IN}^2/I_O$, when all four devices have the same aspect ratio. The EKV-based relation (16) reveals that the cubic relation with respect to $\sqrt{I_{OUT}}$ (when the values of the remaining quantities are known) now has a term which exhibits a dependence upon the (5/2) power of I_{IN} , whereas in (14), dependences only up to the (3/2) power of I_{IN} are present.

Figure 2: The 4-NMOS squarer TL circuit. The bulk terminals of the NMOS devices are connected to the source. The dashed green line defines the closed loop, where KVL can be applied along.

3.1.3. A 6 MOS Multiplier/Divider TL Circuit

It would be interesting to explore the properties of a circuit useful for the implementation of high powers of currents [30]. The circuit illustrated in Figure 3 is comprised of three different stages, however, it can also be comprised of more than five stages [30]. The alternating loop formation is usually preferred, due to its low-power consumption property.

Similarly to the previous cases, (5) and (12) (again $X_j = \sqrt{I_j/(I_{D_o}\alpha_j)}$, $j = 1, \dots, 6$) are used to produce the equations for the input and output currents of this block, presented in full,

Figure 3: An alternating formation STL block implementing the third power of an input current. The dashed green line defines the closed loop, where KVL can be applied along.

symbolic form in Table 1. The index of each drain current is depicted in Figure 3. The ideal relation (17) realises the cubic power of I_{IN} , when the M_j ($j = 1, \dots, 6$) devices have the same aspect ratio: $I_{OUT} = I_{IN}^3/I_O^2$. The EKV-based relation (18) reveals that the cubic relation with respect to $\sqrt{I_{OUT}}$ (when the values of the remaining quantities are known) has a term $\sim I_{IN}^{7/2}$.

3.2. Dynamic Translinear Circuits (DTL Circuits)

Linear filtering is the main application for DTL topologies. Treating the typical, class-A Log-domain lossy integrator as the fundamental representative of ELIN [31] DTL circuits, a detailed analysis has been conducted using both the ideal and the EKV-based approach, producing symbolic expressions for key currents and voltages, based on an indicative sinusoidal input signal.

Table 1: Summary of ideal and EKV-based static translinear circuit current expressions generated by equations (5) and (12).

4-MOS STL	$\frac{I_{IN}\lambda}{\alpha_1\alpha_2} - \frac{I_{OUT}}{\alpha_3\alpha_4} = 0$ (13)	Ideal
	$I_{D_o}^{1/2} \left[\frac{I_{IN}\lambda}{\alpha_1\alpha_2} - \frac{I_{OUT}}{\alpha_3\alpha_4} \right] + M^{1/2} \left[\frac{I_{IN}\lambda^{3/2}}{\alpha_1\alpha_2^{3/2}} - \frac{I_{OUT}}{\alpha_3^{3/2}\alpha_4} \right] + \lambda \left[\frac{I_{IN}^{3/2}}{\alpha_1^{3/2}\alpha_2} - \frac{I_{OUT}^{3/2}}{\lambda\alpha_3\alpha_4^{3/2}} \right] = 0$ (14)	EKV-based
Squarer STL	$\frac{I_{IN}^2}{\alpha_1\alpha_2} - \frac{I_O I_{OUT}}{\alpha_3\alpha_4} = 0$ (15)	Ideal
	$I_{D_o}^{1/2} \left[\frac{I_{IN}^2}{\alpha_1\alpha_2} - \frac{I_O I_{OUT}}{\alpha_3\alpha_4} \right] \left(1 + \frac{I_O^{1/2}}{(I_{D_o}\alpha_3)^{1/2}} \right) + \frac{I_{IN}^{5/2}}{\alpha_1\alpha_2} \left(\frac{\alpha_1^{1/2} + \alpha_2^{1/2}}{(\alpha_1\alpha_2)^{1/2}} \right) - \frac{I_O I_{OUT}^{3/2}}{\alpha_3\alpha_4^{3/2}} = 0$ (16)	EKV-based
6-MOS Alt. STL	$\frac{I_{IN}^3}{\alpha_1\alpha_3\alpha_5} - \frac{I_O^2 I_{OUT}}{\alpha_2\alpha_4\alpha_6} = 0$ (17)	Ideal
	$I_{D_o}^{1/2} \left[\frac{I_{IN}^3}{\alpha_1\alpha_3\alpha_5} - \frac{I_O^2 I_{OUT}}{\alpha_2\alpha_4\alpha_6} \right] \left(1 + \frac{I_O^{1/2} (\alpha_2^{1/2} + \alpha_4^{1/2})}{(I_{D_o}\alpha_2\alpha_4)^{1/2}} \right) + \frac{I_{IN}^{7/2}}{\alpha_1\alpha_3\alpha_5} \left(\frac{(\alpha_3\alpha_5)^{1/2} + (\alpha_1\alpha_5)^{1/2} + (\alpha_1\alpha_3)^{1/2}}{(\alpha_1\alpha_3\alpha_5)^{1/2}} \right) - \frac{I_O^2 I_{OUT}^{3/2}}{\alpha_2\alpha_4\alpha_6^{3/2}} = 0$ (18)	EKV-based

Figure 4: A 1st order, low-pass, Log-domain filter. The dashed lines illustrate the two voltage loops, where KVL can be applied along.

3.2.1. 1st Order Low-Pass Log-Domain Filter

Figure 4 illustrates a typical 4 MOST, Log-domain, lossy integrator. Applying KVL along the 2 loops shown using (5) and solving appropriately the resulting differential and algebraic equations, ideal expressions for the output and capacitor currents and for the capacitor voltage V_{Cap} can be produced as summarised in the dimensionally consistent Table 2. The transient terms have been omitted in the expression of I_{OUT} , I_{D2} and i_{Cap} for simplicity.

Referring to Table 2, it is clear that the consideration of the ideal relation (5) confirms that the output current I_{OUT} is a perfectly scaled and shifted version of the input sinusoid $A \sin(\omega t)$ signal (linear filtering). Such a relation, however, cannot be used for the study of the dependence of the output current's linearity levels upon, for example, device sizes or process parameters, although such dependences have been verified through measurements and simulations. The issue can be tackled by exploiting (12) instead of (5) for the circuit's analysis. Considering KVL along the loops 1 and 2 of Figure 4 and using (12) leads to the following current expressions:

$$\underbrace{\frac{I_{D0}^{1/2} I_{IN}}{\alpha_1} + \frac{I_{IN}^{3/2}}{\alpha_1^{3/2}}}_{(1)} = e^{\frac{V_{Cap}^{EKV}}{nV_T}} = \underbrace{\frac{I_{D0}^{1/2} I_{OUT}}{\alpha_4} + \frac{I_{OUT}^{3/2}}{\alpha_4^{3/2}}}_{(2)}, \quad (19)$$

where V_{Cap}^{EKV} is defining the capacitor voltage, when (12) is used for the circuitual analysis. Re-grouping (1) helps us view the LHS of (19) as:

$$\frac{V_{Cap}^{Ideal}}{e n V_T} \left(1 + \sqrt{\frac{I_{IN}}{I_{D0} \alpha_1}} \right) = \frac{V_{Cap}^{EKV}}{e n V_T}. \quad (20)$$

Assuming that the filter operates well-inside WI, then we can reasonably accept that the behaviour of its currents will

be governed by the exponential behaviour of (3). Therefore, the factor $(I_{IN} \alpha_2)/(I_{D2} \alpha_1)$ on the left of (20) can be substituted for $\exp(V_{Cap}/nV_T)$, where V_{Cap} is the “ideal” capacitor voltage, shown in Table 2. This valid substitution, allows us to express the EKV-based V_{Cap} in (20), as a function of a known, already computed expression. Both capacitor expressions tend to match each other, when X is much smaller than unity and are producing almost identical results regarding the DC levels of the currents I_{D2} and I_{OUT} (since the factors $(1 + \sqrt{I_j/(I_{D0} \alpha_j)})$ are quite small).

Table 2: Full, symbolic expressions for the ideal values of I_{OUT} , i_{cap} & V_{Cap} of the Log-domain filter of Figure 4.

Ideal Expression of I_{OUT}

$$I_{OUT}^{Ideal} = I_O \frac{\alpha_2 \alpha_4 \Xi}{\alpha_1 \alpha_3 \Theta}$$

Ideal Expression of i_{cap}

$$I_{D2}^{Ideal} = i_{Cap}^{Ideal} + I_d = \frac{A \sin(\omega t) + I_{DC}}{\Xi / \Theta}$$

Ideal Expression of V_{Cap}

$$V_{Cap}^{Ideal} = nV_T \ln \left(\frac{\alpha_2 \Xi}{\alpha_1 \Theta} \right)$$

Where:

- $\Xi = \omega_d^2 A \sin(\omega t) - \omega \omega_d (A \cos(\omega t)) + \omega^2 I_{DC} + \omega_d^2 I_{DC}$
- $\Theta = I_d (\omega^2 + \omega_d^2)$

with: $\omega = 2\pi f$ and $\omega_d = I_d/(nC V_T)$

Based on (20), equality (2) in (19) can be used for the EKV-based symbolic expressions for the output current, the capacitor current and the capacitor voltage, all summarised in Table 3. In contrast to the ideal relations of Table 2: a) Both process parameters (I_{D0}) and device sizes affect the EKV-based relations of Table 3 and, b) the relation between I_{OUT}^{EKV} and I_{IN} does not correspond to a linear filter. The relations of Table 3 are exploited in Section 4 for the study of the dependence of the output current linearity levels upon certain transistor-level design parameters.

4. Mathematical Calculation and Cadence Simulation Results

In this section, simulated results sourcing from mathematical calculations using the analytic, symbolic formulas shown in Section 3 and Cadence simulations (AMS 0.35 μm - MM / 2P4M c35b4 CMOS technology) are presented. The selected simulation values ensure that the basic assumption made in Section 2 regarding the range of quantity X remains valid. The obtained results, aim at evaluating how close the symbolic expressions of Table 1 are to the BSIM3V3-based results provided by Spectre®. Finally, 3D graphs reporting the deviation between

Table 3: Full, symbolic expressions for the EKV-based values of I_{OUT} , i_{Cap} & V_{Cap} of the Log-domain filter of Figure 4.

Process-Parameter-Dependent Expression of I_{OUT}	
$\frac{I_{OUT}^{EKV}}{\alpha_4} \left(1 + \sqrt{I_{OUT}^{EKV}/(I_{D0}\alpha_4)} \right) = \frac{I_O}{\alpha_3} \left(1 + \sqrt{I_O/(I_{D0}\alpha_3)} \right) e^{\frac{V_{Cap}^{EKV}}{nV_T}}$	
Process-Parameter-Dependent Expression of i_{Cap}	
$\frac{I_{D2}^{EKV}}{\alpha_2} \left(1 + \sqrt{I_{D2}^{EKV}/(I_{D0}\alpha_2)} \right) = \frac{I_{IN} \left(1 + \sqrt{I_{IN}/(I_{D0}\alpha_1)} \right)}{\alpha_1} e^{-\frac{V_{Cap}^{EKV}}{nV_T}}, \text{ with } I_{D2}^{EKV} = i_{Cap}^{EKV} + I_d$	
Process-Parameter-Dependent Expression of V_{Cap}	
$V_{Cap}^{EKV} = V_{Cap}^{Ideal} + \ln \left[\frac{1 + \sqrt{I_{IN}/(I_{D0}\alpha_1)}}{1 + \sqrt{(I_{IN}/(I_{D0}\alpha_1))} \sqrt{e^{-V_{Cap}^{Ideal}/nV_T}}} \right]$	

the ideal expressions of Table 1 and the EKV-based ones in a more qualitative manner are also illustrated. The percentage deviation illustrated in the 3D graphs corresponds to the quantities $(I_{OUT}^{Ideal} - I_{OUT}^{EKV})/I_{OUT}^{Ideal}$ and $(I_{OUT}^{Cad.} - I_{OUT}^{EKV})/I_{OUT}^{Cad.}$, which are referred to in Figure 5, Figure 6 and Figure 7 as “*Ideal Eq. - EKV Eq. surface*” and “*Cadence - EKV Eq. surface*”, respectively.

4.1. 4 MOS Multiplier/Divider TL Circuit

Two indicative cases will be examined for this circuit. In both of them the aspect ratios of all devices are kept the same and equal to the randomly picked value 7. The remaining electrical parameters for both cases are summarised in Table 4. Simulation results for the first case are shown in Figure 5a and Figure 5b, while for the second one are shown in Figure 5c and Figure 5d. From Figure 5a and Figure 5c one can observe that the EKV-based approach is very close to Cadence simulated results, verifying the validity of the analysis. The 3D graphs, on the other hand, demonstrate interesting, seemingly counter-intuitive results. Although in both cases, the product of I_{IN} and λ is the same at every point of the surfaces, the deviation between the models is different. In the first case, the range of the I_{IN} and I_2 current is the same (10nA-100nA), while in the second one the range of the current I_2 is always 100 times bigger. Re-expressing (14) in the form:

$$I_{OUT} = \underbrace{\lambda \frac{\alpha_3 \alpha_4}{\alpha_1 \alpha_2} I_{IN}}_{\text{Ideal Output}} \frac{1 + \sqrt{IC_2} + \sqrt{IC_{IN}}}{1 + \sqrt{IC_3} + \sqrt{IC_{OUT}}}, \quad (21)$$

where $IC_j = I_j/(\alpha_j I_{D0})$ is the inversion coefficient of transistor M_j (see Figure 1), the following are observed: Referring to case 1, when $I_2 \rightarrow 100\text{nA}$, then $\lambda \rightarrow 10$ and $I_{OUT} \rightarrow 1\mu\text{A}$, when $I_{IN} \rightarrow 100\text{nA}$; for such values ($\lambda \rightarrow 10$, $I_{IN} \rightarrow 100\text{nA}$, $I_{OUT} \rightarrow 1\mu\text{A}$, $I_2 \rightarrow 100\text{nA}$) $I_3 (= 10\text{nA}) < I_2 (\sim I_{IN}) < I_{OUT} \Rightarrow IC_3 < IC_2 (\sim IC_{IN}) < IC_{OUT}$, which explains why the response deviates ($\approx 15\%$) from ideality (“*Ideal Eq. - EKV Eq surface*”), when $I_{IN} = 100\text{nA}$; the condition $IC_2 \sim IC_{IN}$ results

in these two terms contributing in an additive manner to deviations from ideality since they both appear in the numerator of the fraction in (21). In the denominator, IC_3 is small in comparison to the numerator terms and the IC_{OUT} term. This means that the denominator’s value is dominated by IC_{OUT} and (since IC_2 , $IC_{IN} \sim IC_{OUT}/\sqrt{10}$) that the fraction in (21) becomes smaller than unity and the deviation increases. Considering that $\sqrt{IC_3} + \sqrt{IC_{OUT}} \approx \sqrt{IC_{OUT}}$, the percentile deviation from ideality in this case (case 1) ($\lambda \rightarrow 10$, $I_{IN} \rightarrow 100\text{nA}$, $I_{OUT} \rightarrow 1\mu\text{A}$, $I_2 \approx I_{IN}$) roughly becomes:

$$(\text{deviation } (\%))_{(\text{Ideal-EKV})/\text{Ideal}}^{\lambda \rightarrow 10, I_{IN} \rightarrow 100\text{nA}} \approx \frac{\sqrt{IC_{OUT}} - 2\sqrt{IC_{IN}}}{1 + \sqrt{IC_{OUT}}}. \quad (22)$$

For case 2, when $I_2 \rightarrow 1\mu\text{A}$, then $\lambda \rightarrow 100$ and $I_{OUT} \rightarrow 100\text{nA}$ when $I_{IN} \rightarrow 1\text{nA}$. Consequently (see Table 1 and Figure 1) for such values: $IC_{IN} \leq IC_3 < IC_{OUT} < IC_2$, which explains why the output current deviates from ideality (“*Ideal Eq. - EKV Eq. surface*” in Figure 5d), when I_{IN} takes small values close to 1nA ; when $I_2 \rightarrow 1\mu\text{A}$ and $I_{IN} \rightarrow 1\text{nA}$, $IC_2 \approx 32IC_{IN}$; with $I_3 = 10\text{nA}$ and $I_{OUT} \rightarrow 100\text{nA}$, $IC_{OUT} \approx 3.2IC_3$; thus, the value of the numerator of the fraction in (21) is governed by IC_2 , while the denominator value by IC_{OUT} , which means that the fraction becomes approximately equal to $(1 + \sqrt{IC_2})/(1 + \sqrt{IC_{OUT}})$, with IC_{OUT} always smaller than IC_2 . In this way deviation from ideality is introduced. The rough estimation of the % deviation now (case 2) becomes:

$$(\text{deviation } (\%))_{(\text{Ideal-EKV})/\text{Ideal}}^{\lambda \rightarrow 100, I_{IN} \rightarrow 1\text{nA}} \approx \frac{\sqrt{IC_{OUT}} - \sqrt{IC_2}}{1 + \sqrt{IC_{OUT}}}. \quad (23)$$

Observe from Figure 5b and Figure 5d that for given α_j value, when the gain λ value ranges between 10 and 20 and I_{IN} ranges between 10nA and 20nA , then the deviation from ideality is minimised (almost nullified) with the agreement between Cadence and EKV results also being very good (deviation $\sim 2 - 3\%$).

Table 4: Electrical parameters for the 4 MOS STL shown in Figure 1.

Case	I_{IN} [nA]	$I_2/I_3(\lambda)$	$I_3(=M)$ [nA]
1	10-100	1-10	10
2	1-10	10-100	10

4.2. Squarer TL Circuit

For this circuit, two indicative cases will be examined again. In the first case the aspect ratio of devices M_1 and M_4 is the same and 10 times bigger than the aspect ratio of the devices M_2 and M_3 , while in the second case, all devices have the same aspect ratio. The rest of the electrical parameters for both cases are listed in Table 5. Simulation results for the first case are shown in Figure 6a and Figure 6b, while for the second one in Figure 6c and Figure 6d. Once again, the 2D graphs confirm that the EKV-based results shadow Cadence results. The 3D graphs show that although in case 1 the circuit has two devices (M_2 and M_3) that are x10 smaller than the other two (M_1

and M_4), deviations between the EKV model (and consequently Cadence) and the ideal model are smaller throughout the whole simulation range, compared to the deviations observed when all devices occupy the same area. Re-expressing (16) in the form:

$$I_{OUT} = \frac{\alpha_3 \alpha_4 I_{IN}^2}{\underbrace{\alpha_1 \alpha_2 I_O}_{Ideal\ Output}} \frac{1 + \frac{\sqrt{\alpha_1} + \sqrt{\alpha_2}}{\sqrt{\alpha_1 \alpha_2}} \sqrt{\frac{I_{IN}}{I_{D_0}}}}{1 + \sqrt{\frac{I_O}{\alpha_3 I_{D_0}}} + \sqrt{\frac{I_{OUT}}{\alpha_4 I_{D_0}}}} \quad (24)$$

and considering that for the first case $\alpha_{2,3} = 0.1\alpha_{1,4} = 0.1\alpha$, while for the second case $\alpha_{1,2,3,4} = \alpha$, yields:

$$I_{OUT}^{Case\ 1} = \frac{\overbrace{I_{IN}^2}^{Ideal\ Output}}{I_O} \frac{1 + (4.2) \sqrt{\frac{I_{IN}}{\alpha I_{D_0}}}}{1 + \sqrt{\frac{I_O}{0.1\alpha I_{D_0}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_0}}}} \quad (25)$$

$$I_{OUT}^{Case\ 2} = \frac{\overbrace{I_{IN}^2}^{Ideal\ Output}}{I_O} \frac{1 + (2) \sqrt{\frac{I_{IN}}{\alpha I_{D_0}}}}{1 + \sqrt{\frac{I_O}{\alpha I_{D_0}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_0}}}} \quad (26)$$

Observe that, interestingly, the first case of unequal device sizes results in the IC of the input device (which carries I_{IN} together with M_2 , see Figure 2) appearing to contribute more than

(a) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for the parameters of case 1.

(b) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for the parameters of case 1.

(c) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for the parameters of case 2.

(d) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for the parameters of case 2.

Figure 5: Two dimensional graphs of I_{OUT} current for the EKV-based model and Cadence simulations for both cases shown in Table 4 for the 4 MOS STL shown in Figure 1, accompanied by three dimensional representations of their in between percentile deviations.

twice as much as it contributes in the denominator of (26). Furthermore, the second term in the denominator of (25) is larger (because of the different size) than the second term in the denominator of (26) by $\sqrt{10} \approx 3.2$ times. From (25) and (26), the percentile deviations for both cases become:

Table 5: Electrical parameters for the squarer STL shown in Figure 2.

Case	I_{IN} [nA]	I_O [nA]	$[W/L]_{1,4}$	$[W/L]_{2,3}$
1	5-33	1	10-50	1-5
2	5-33	1	10-50	10-50

Case 1: (deviation(%))_{(Ideal-EKV)/Ideal}

$$= \frac{\sqrt{10} \sqrt{\frac{I_O}{\alpha I_{D_0}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_0}}} - (4.2) \sqrt{\frac{I_{IN}}{\alpha I_{D_0}}}}{1 + \sqrt{10} \sqrt{\frac{I_O}{\alpha I_{D_0}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_0}}}} \quad (27)$$

(a) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for case 1 parameters. The aspect ratios of the devices are set as: $\alpha_{2,3} = 0.1$ $\alpha_{1,4} (= [W/L])$.

(b) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for case 1 parameters. The aspect ratios of the devices are set as: $\alpha_{2,3} = 0.1$ $\alpha_{1,4} (= [W/L])$.

(c) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for case 2 parameters. The aspect ratios of the devices are set as: $\alpha_{1,2,3,4} = [W/L]$.

(d) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for case 2 parameters. The aspect ratios of the devices are set as: $\alpha_{1,2,3,4} = [W/L]$.

Figure 6: Two dimensional graphs of I_{OUT} current for EKV-based model and Cadence simulations for both cases shown in Table 5 for the squarer STL shown in Figure 2, accompanied by three dimensional representations of their in between percentile deviations.

$$\text{Case 2:}(\text{deviation}(\%))_{(\text{Ideal-EKV})/\text{Ideal}} = \frac{\sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}} - (2) \sqrt{\frac{I_{IN}}{\alpha I_{D_o}}}}{1 + \sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}}}. \quad (28)$$

When I_{IN} increases towards the value of 30nA and given that I_O is set to 1nA , the output current I_{OUT} takes larger values (ideally $I_{OUT} \sim I_{IN}^2/I_O$). This means that both the numerators and denominators of (27) and (28) are dominated by I_{OUT} . However, the denominator of (27) is always larger than the denominator of (28), which explains the somewhat reduced deviation from ideality in Figure 6b. The difference between Spectre® and EKV is similar and reduces to $\sim 1 - 2\%$, when I_{IN} reaches its maximum.

4.3. 6 MOS Multiplier/Divider TL Circuit

For the last analysis example of STL circuits, again, two indicative cases will be presented. In the first case the aspect ratio of the devices M_1 and M_6 is kept the same and 10 times bigger than the aspect ratio of the devices M_2 , M_3 , M_4 and M_5 , while in the second case, all transistors have the same aspect ratio. The rest of the electrical parameters are tabulated in Table 6. Simulation results for the first case are shown in Figure 7a and Figure 7b and for the second one in Figure 7c and Figure 7d. The output current range is, again, expected to be the same in both cases based on the ideal approach. Figure 7a and Figure 7b verify that in case 1, the circuit demonstrates smaller deviations from its ideal behaviour throughout the simulations range, while in the second case greater deviations are taking place, in conjunction with larger total area. Re-expressing (18) in the form:

$$I_{OUT} = \underbrace{\frac{\alpha_2 \alpha_4 \alpha_6 I_{IN}^3}{\alpha_1 \alpha_3 \alpha_5 I_O^2}}_{\text{Ideal Output}} \frac{1 + \frac{\sqrt{\alpha_1 \alpha_3} + \sqrt{\alpha_3 \alpha_5} + \sqrt{\alpha_1 \alpha_5}}{\sqrt{\alpha_1 \alpha_3 \alpha_5}} \sqrt{\frac{I_{IN}}{I_{D_o}}}}{1 + \frac{\sqrt{\alpha_2} + \sqrt{\alpha_4}}{\sqrt{\alpha_2 \alpha_4}} \sqrt{\frac{I_O}{I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha_6 I_{D_o}}}} \quad (29)$$

and considering that for the first case $\alpha_{2,3,4,5} = 0.1\alpha_{1,6} = 0.1\alpha$, while for the second case $\alpha_{1,2,3,4,5,6} = \alpha$, yields:

$$I_{OUT}^{\text{Case 1}} = \underbrace{\frac{I_{IN}^3}{I_O^2}}_{\text{Ideal Output}} \frac{1 + (7.32) \sqrt{\frac{I_{IN}}{\alpha I_{D_o}}}}{1 + (6.32) \sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}}} \quad (30)$$

$$I_{OUT}^{\text{Case 2}} = \underbrace{\frac{I_{IN}^3}{I_O^2}}_{\text{Ideal Output}} \frac{1 + (3) \sqrt{\frac{I_{IN}}{\alpha I_{D_o}}}}{1 + (2) \sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}}} \quad (31)$$

From (29), (30) and (31), it becomes clear that the size of each transistor matters; even though the ideal output for both cases

is the same, the two different ratiometric allocations lead to different deviation profiles from ideality. From (30) and (31) the percentile deviations for both cases can be expressed as:

$$\text{Case 1:}(\text{deviation}(\%))_{(\text{Ideal-EKV})/\text{Ideal}} \approx \frac{\sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}} - (7.32) \sqrt{\frac{I_{IN}}{\alpha I_{D_o}}}}{1 + (6.32) \sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}}} \quad (32)$$

$$\text{Case 2:}(\text{deviation}(\%))_{(\text{Ideal-EKV})/\text{Ideal}} \approx \frac{\sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}} - (2) \sqrt{\frac{I_{IN}}{\alpha I_{D_o}}}}{1 + (2) \sqrt{\frac{I_O}{\alpha I_{D_o}}} + \sqrt{\frac{I_{OUT}}{\alpha I_{D_o}}}} \quad (33)$$

When I_{IN} increases towards the value of 10nA and given that I_O is set to 1nA , the output current I_{OUT} takes very large values (ideally $I_{OUT} \sim I_{IN}^3/I_O^2$). This means that both the numerators and denominators of (32) and (33) are dominated by I_{OUT} . However, the denominator of (32) is always larger than the denominator of (33), which explains the somewhat reduced deviations from ideality in Figure 7.

Table 6: Electrical parameters for the 6 MOS-Alt. STL shown in Figure 3.

Case	I_{IN} [nA]	I_O [nA]	$[W/L]_{1,6}$	$[W/L]_{2,3,4,5}$
1	1-10	1	10-50	1-5
2	1-10	1	10-50	10-50

4.4. Accuracy Vs. Device Area

In order to highlight even more the impact of aspect ratios upon the accuracy of TL circuits, an inclusive mathematical simulation is presented, demonstrating the deviation of the EKV model from the ideal TL behaviour, when we experiment with different device sizes. Due to lack of space, only one STL circuit case has been selected to be presented, the 4 MOS multiplier / divider. Again two cases are examined. In the first one, all devices are assumed to have the same area, while in the second one only the areas of the devices M_1 and M_4 , and M_2 and M_3 are the same. The rest of the electrical parameters are summarised in Table 7 for both cases. The mathematical relations that describe cases 1 and 2 are (34) and (35), respectively.

Case 1 - When All Areas Are Equal:

$$I_{OUT} = \underbrace{\lambda I_{IN}}_{\text{Ideal Output}} \frac{\sqrt{I_{D_o}} + \sqrt{I_{IN}} + L \sqrt{\frac{I_2}{A}}}{\sqrt{I_{D_o}} + \sqrt{I_{OUT}} + L \sqrt{\frac{I_3}{A}}} \quad (34)$$

(a) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for case 1 parameters. The aspect ratios of the devices are set as: $\alpha_{2,3,4,5} = 0.1$ $\alpha_{1,6} (= [W/L])$.

(b) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for case 1 parameters. The aspect ratios of the devices are set as: $\alpha_{2,3,4,5} = 0.1$ $\alpha_{1,6} (= [W/L])$.

(c) 2D behaviour of I_{OUT} based on the EKV-model mathematical simulations and Cadence simulations for case 2 parameters. The aspect ratios of the devices are set as: $\alpha_{1,2,3,4,5,6} = [W/L]$.

(d) 3D representation of the deviation of I_{OUT} between the two different mathematical models and Cadence simulations for case 2 parameters. The aspect ratios of the devices are set as: $\alpha_{1,2,3,4,5,6} = [W/L]$.

Figure 7: Two dimensional graphs of I_{OUT} current for EKV-based model and Cadence simulations for both cases shown in Table 6 for the 6 MOS-Alt. STL shown in Figure 3, accompanied by three dimensional representations of their in between percentile deviations.

Case 2 - When Area Of $M_1 = M_4$ & $M_2 = M_3$:

$$I_{OUT} = \widehat{\lambda I_{IN}^{Ideal Output}} \frac{\sqrt{I_{D0}} + L \sqrt{\frac{I_{IN}}{A_1}} + L \sqrt{\frac{I_2}{A_2}}}{\sqrt{I_{D0}} + L \sqrt{\frac{I_{OUT}}{A_1}} + L \sqrt{\frac{I_3}{A_2}}} \quad (35)$$

where $A_j = W_j L_j$ (when $j=1$ and $4 \rightarrow A_1$ and when $j=2$ and $3 \rightarrow A_2$) and L_j is each MOST's channel length. As Figure 8 reveals, for a large gain value, the deviation between EKV and the ideal response is smaller when the devices occupy a large

area. However, for device area larger than ($> 20 - 25 \mu m^2$) the improvement is not significant; an increase in transistor sizes does not result in improved output current accuracy. Such a behaviour can be explained when (34) is considered: when the device area A increases in value, the fraction in (34) reaches asymptotically the value of:

$$I_{OUT} = I_{OUT}^{Ideal} \frac{\sqrt{I_{D0}} + \sqrt{I_{IN}}}{\sqrt{I_{D0}} + \sqrt{I_{OUT}}}$$

which does not depend on A .

For the second case, depicted in Figure 9, a large gain value ($\times 80$) has been selected on purpose. Simulations verify that

Figure 8: Contour and 3D plot of the EKV-based 4 MOS STL circuit's (see Figure 1) output current deviation from the ideal behaviour, when all areas are same.

the deviation becomes smaller when A_2 increases. Considering (35), increasing A_2 values decrease the magnitude of I_2 , I_{OUT} -dependent terms of the fraction (I_2 and I_{OUT} are the large currents of the circuit) with the I_{IN} , I_3 -dependent terms having similar magnitude (since $I_3 = 10nA$ and $I_{IN} = 5nA$). On the other hand, when A_1 takes large values but A_2 decreases towards the $10\mu m^2$ value, then the I_2 , I_{OUT} -dependent terms in the fraction of (35) become dominant and the percentile deviation increases; it is a simple matter to show that in this case:

$$\text{Case 2 } -(\text{deviation}(\%))_{(\text{Ideal-EKV})/\text{Ideal}} \approx \left(\left[\frac{\sqrt{I_{OUT}} - \sqrt{I_2}}{\sqrt{A_2}} \right] L \right) / \left(\sqrt{I_{D0}} + L \sqrt{\frac{I_{OUT}}{A_2}} \right) \quad (36)$$

when the I_2 current values diverges from the I_{OUT} value (which is the case, since $I_2 = 800nA$ and $I_{OUT} \approx 400nA$).

Figure 9: Contour and 3D plot of the EKV-based 4 MOS STL circuit's (see Figure 1) output current deviation from the ideal behaviour, when the areas of M_1 & M_4 (A_1) and M_2 & M_3 (A_2) are equal, respectively.

Table 7: Electrical parameters for the area vs accuracy simulations for the 4 MOS STL shown in Figure 1.

Case	I_{IN} [nA]	λ	M [nA]	Area [μm^2]	L [μm]
1	5	1-100	10	1-50	1
2	5	80	10	1-50	1

4.5. 1st Order Low-Pass Log-Domain Filter

Exploiting the EKV-based, symbolic expression shown in Table 3 for the output current and for the electrical parameters tabulated in Table 8, the HD_2 and HD_3 distortion levels of the filter's output have been investigated. Figure 10 reveals the very good agreement between the mathematical calculations and Cadence simulated results. As it can be verified from the graph, increased deviation between the two approaches takes place for a large value of aspect ratios and modulation index. However, regardless the large modulation index and aspect ratio values, the difference between the simulated circuit and the mathematical approach does not exceed $4dBc$.

With the validity of the symbolic expressions listed in Table 3 verified, the effect of the process-parameter I_{D0} upon the circuit's linearity can be studied; and in particular the effect of the factor $\mu_{eff}C_{ox}$, which varies with technology. From Figure 11 it can be observed that when the product $\mu_{eff}C_{ox}$ increases, the distortion levels of the circuit are falling and vice versa. This means that in technologies, where oxide thickness is very small, the distortion levels of the specific Log-domain filter will be smaller (since $t_{ox} = A\epsilon_{ox}/C_{ox}$ - where A is the gate area of metal), provided that μ_{eff} remains the same. Noticeable differences between μ_{eff} values can be also spotted between NMOS and PMOS devices.

Table 8: Electrical parameters of the Log-domain filter. All devices have the same aspect ratios.

I_{DC} [nA]	f [Hz]	C [pF]	I_d, I_o [nA]	f_c [Hz]
100	1K	5	5,5	4.8K

5. Effect Of The Aspect Ratio Upon The Level of Inversion in Subthreshold CMOS Translinear Circuits

The previous sections aimed at (a) providing sufficient evidence that the proposed EKV-based model is shadowing Cadence simulations closer than the ideal TL model and (b) offering a purely quantitative approach to the calculation of the output current values of each of the previous topologies. All the previous formulas can be used as a first cut approximation for the output current calculation and deviation estimate from the ideal behaviour of the aforementioned TL topologies. In this section, a different approach will be adopted, in order to explore the effect of the various currents and aspect ratios upon the output current ranges of the different TL circuits. For a more qualitative approach to the previous topologies, the IC of the output transistor of each topology will be plotted against key circuit parameters, in an attempt to demonstrate that although

Figure 10: HD_2 and HD_3 distortion levels of the output current of the Log-domain filter shown in Figure 4. The distortion levels are expressed in dBc and are presented versus the filter's modulation index (upper graphs) and also versus the devices' aspect ratio (lower graphs). Very good agreement exists between mathematical calculations and Cadence simulations ($4dBc$ in average). It is reminded that the signal's frequency is set to $1KHz$, the cut-off frequency is $\approx 4.8KHz$, the capacitance is $5pF$ and the biasing currents are being set to $5nA$ each. The dBc values on the graphs demonstrate approximately the deviation between the two methods for the maximum value of modulation index (upper two graphs) and $[W/L]$ ratio (lower two graphs).

Figure 11: The effect of the product $\mu_{eff}C_{ox}$ upon the output harmonic distortion levels of the Log-domain filter. The central value of the distribution is the one shown in Section 2 ($260/2nV_T^2$).

the transistors' current ranges might seem low, it is the $[W/L]$ ratio that defines the level of inversion of the devices and subsequently the integrity of their exponential behaviour.

For the stacked-formation 4 MOS multiplier/divider TL cir-

cuit of Figure 1, the effect of the aspect ratio upon the level of inversion of the transistors is investigated. The devices M_1 , M_2 and M_3 (see Figure 1) are biased by appropriate current sources, therefore, there is no need to calculate the IC of these devices,

(a) Inverse coefficient versus $[W/L]$ for fixed I_{IN} and gain .

(b) Deviation from ideal IC versus I_{IN} for fixed $[W/L]$ and gain .

Figure 12: The dependence of the IC of the output transistor M_4 of the 4 MOS multiplier / divider of Figure 1 upon the aspect ratio and input current of the circuit.

since their IC will be defined by the relation $IC_j = I_j / (I_{D_0} \alpha_j)$ ($j = 1, 2, 3$). Here, the focal point is the current of the output device M_4 , whose current and subsequently IC value is not defined directly by the previous IC formula but from relation (21), stemming from the application of the TLP in the closed loop shown in Figure 1.

From the ideal TLP, the IC of transistor M_4 can be calculated based on relation (13). However, this IC_{OUT}^{Ideal} value is independent of the aspect ratios or current combinations of currents I_2 and I_3 that generate the desired gain value. In Figure 12, two interesting, counter-intuitive results have been generated using the ideal TL equations and the proposed EKV-based model. For a fixed value of I_{IN} and gain, the IC value of M_4 is plotted against the aspect ratio, assuming that all devices have the same $[W/L]$. The gain, defined by the current values of the devices M_2 and M_3 remains constant, however, the current combinations of the transistors M_2 and M_3 are different. Although one would expect the IC_{OUT} value to remain constant, no matter what current combination is selected for I_2 and $I_3 = M$, it seems that since the IC_{OUT}^{EKV} is defined by (21), different biasing combinations lead to different IC_{OUT} values.

Figure 13: The dependence of the IC of the output transistor M_4 of the 4 MOS squarer of Figure 2 upon the aspect ratio of the devices, with $[W/L]_{2,3} = [W/L]$.

Moreover, the deviation from the ideal IC has been plotted against the input current for fixed $[W/L]$ for all devices and constant gain, which again is produced by different current combinations of the transistors M_2 and M_3 . Once again, different percentile deviations are observed for each biasing combinations.

In a similar attempt, for fixed I_{IN} and I_O currents, the ICs of the output transistors M_4 of the 4 MOS squarer of Figure 2 and M_6 of the 6 MOS multiplier/divider of Figure 3 have been plotted against their aspect ratio. Equations (15) and (24) have been employed for the computation of the ideal and EKV-based IC of the 4 MOS squarer, while equations (17) and (29) have been used for the 6 MOS multiplier/divider case. The results obtained for the two circuits can be seen in Figure 13 and Figure 14, respectively.

Figure 14: The dependence of the IC of the output transistor M_6 of the 6 MOS multiplier / divider of Figure 3 upon the aspect ratio of the devices, with $[W/L]_{2,3,4,5} = [W/L]$.

5.1. The “Hidden” Non-Ideality Factor

Based on the detailed analysis of Section 4 and verified by the previous qualitative results, it can be concluded that a “non-ideality factor” is nested within the relations codifying the ideal

operation of each TL circuit; consider for example relations (21), (24) and (29). More specifically: whereas for the ideal case the TL expression takes the well-known form:

$$\frac{\prod_{k,CW} \alpha_k \prod_{j,CCW} I_j}{\prod_{j,CCW} \alpha_j \prod_{k,CW} I_k} = 1. \quad (37)$$

When EKV - related terms are taken into consideration (and under the assumptions been made for X , as shown in Section 2), the circuit will not realise the ideal behaviour shown in (37). The EKV model introduces a “*non-ideality factor*” and the expression codifying the TL circuit’s operation takes now the following form:

$$\underbrace{\frac{\prod_{k,CW} \alpha_k \prod_{j,CCW} I_j}{\prod_{j,CCW} \alpha_j \prod_{k,CW} I_k}}_{\text{ideal factor}} \underbrace{\frac{\left(1 + \sum_{j,CCW} \sqrt{IC_j}\right)}{\left(1 + \sum_{k,CW} \sqrt{IC_k}\right)}}_{\text{non-ideality factor}} = 1. \quad (38)$$

The target function of the TL circuit defines its topology whose ideal behaviour is governed by the ideal factor in (38). However, the realisation of high-performance TL circuits deviating as little as possible from the targeted, ideal response calls for the consideration of the “*non-ideality factor*” of (38). Note that the multiplicative nature of the “*non-ideality factor*” leads to the conclusion that a deviation $\mu\%$ from unity translates directly to $\mu\%$ deviation from the ideal behaviour. Consequently, the non-ideality factor needs to deviate as little as possible from unity for a given topology. In practice, this means that:

$$\sum_{j,CCW} \sqrt{IC_j} \approx \sum_{k,CW} \sqrt{IC_k}. \quad (39)$$

Relation (39) suggests that so long as the summation of the square roots of the IC s of the clockwise MOSTs balances the summation of the square roots of the IC s of the counter-clockwise ones, the topology’s deviation from ideality will be minimal. What is useful to stretch is that the equality (39) refers to summations of IC s and not to equalities of individual device IC s. Intriguingly, (39) bears a resemblance to the MOS TLP relation originating from the quadratic behaviour of strongly-inverted MOSTs in saturation [20].

6. Optimisation Techniques For Translinear Topologies

From equation (38), the reader can realise that the presence of the “*non-ideality factor*” is mainly responsible for deviations from ideality shown in previous results. Therefore, in order to obtain the optimal performance in the aforementioned TL topologies, this “*non-ideality factor*” needs to be minimised, as shown in (39) and implied in (38). A typical approach to this problem would be the increase of the aspect ratios of all devices in a TL loop. However, as it will be shown in the next paragraphs, such an action would lead to sub-optimal solutions.

In addition, such an increase of the geometrical characteristics of the devices would directly translate to bigger chip sizes; a result that is not favoured in VLSI applications.

Exploiting equations (21), (24), (29), (38) and (39), a mathematical system can be created, capable of computing the optimal aspect ratio combinations that nullify the effect of the “*non-ideality factor*” of the EKV-based model. In the following paragraphs, two categories of optimisation results will be shown for each TL topology, each one stemming from the aforementioned optimisation system and targeting a different circuital parameter. In the first category of results, the percentile deviation between the IC of the output transistor of the EKV-based model and the ideal one are displayed versus the aspect ratios of the devices in each TL loop. In the second category of optimisation results, the percentile deviation between the IC of the output transistor of the EKV-based model and the ideal one are displayed against the input current of each TL topology, for different $[W/L]$ combinations.

It is worth mentioning that with respect to the first category of results, the aspect ratios of the devices of each TL circuit have been separated into two groups, where each group contains an equal number of clockwise and anti-clockwise transistors. For the sake of clarity and due to limited space, only one combination of aspect ratios has been selected to be shown for each category of circuits. More specifically, for the 4 MOS multiplier/divider of Figure 1 and the 4 MOS squarer of Figure 2 the pairs M_1 - M_4 and M_2 - M_3 have been selected to be equal, while for the 6 MOS multiplier/divider of Figure 3, the groups M_1 - M_6 and M_2 - M_3 - M_4 - M_5 have the same size. Similar results are obtained for any other aspect ratio combinations between the devices of the TL topology, as long as these combinations comply with the TLP regarding the anti- and clockwise devices’ grouping.

Beginning with the presentation of the optimisation results for the 4 MOS multiplier/divider of Figure 1, Figure 15 provides counter-intuitive quantitative graphs. More specifically, Figure 15a - Figure 15d illustrate the percentile deviation between the ideal and EKV-based IC of the output device M_4 , for four different cases, each one generated by a different I_{IN} current. The deviation is plotted against the aspect ratio parameter, for five device aspect ratio combinations. As it can be seen from the Figures, for a given input current, only one $[W/L]$ combination is nullifying the difference between the ideal and the EKV-based calculated IC. These results are independent of the gain value that has been selected. On the other hand, Figure 15e - Figure 15h reveal the other side of the same coin. Four distinct cases are presented again, only this time the aspect ratio combination of the TL devices is fixed and the input current I_{IN} is being swept. Again, the interested reader can verify that no matter what the value of the $[W/L]$ parameter is, for a given aspect ratio combination, the deviation between the ideal and the EKV-based IC is nullified for a single I_{IN} current value. A qualitative Table that defines the value of the aspect ratios of the devices for the 4 MOS multiplier/divider of Figure 1 for any input current I_{IN} is provided by Table 9. Finally, it needs to be mentioned that for all simulation results shown in Figure 15, the current $I_3 = M$ has been set equal to $10nA$.

(a) Case 1: $I_{IN} = 1\text{nA}$, where $[W/L]_{2,3} = [W/L]$.

(b) Case 2: $I_{IN} = 10\text{nA}$, where $[W/L]_{2,3} = [W/L]$.

(c) Case 3: $I_{IN} = 20\text{nA}$, where $[W/L]_{2,3} = [W/L]$.

(d) Case 4: $I_{IN} = 40\text{nA}$, where $[W/L]_{2,3} = [W/L]$.

(e) Case 5: $[W/L] = [W/L]_{2,3} = 10*[W/L]_{1,4}$.

(f) Case 6: $[W/L] = [W/L]_{2,3} = [W/L]_{1,4}$.

(g) Case 7: $[W/L] = [W/L]_{2,3} = 0.5*[W/L]_{1,4}$.

(h) Case 8: $[W/L] = [W/L]_{2,3} = 0.25*[W/L]_{1,4}$.

Figure 15: Optimisation results for the 4 MOS multiplier/divider of Figure 1. For given I_{IN} current, only one combination of aspect ratios is cancelling the “non-ideality factor”, leading to optimum results. Although the results are independent of the gain value, the value of 10 has been selected for the provided results.

(a) Case 1: $I_{IN} = 1nA$, where $[W/L]_{2,3} = [W/L]$.

(b) Case 2: $I_{IN} = 5nA$, where $[W/L]_{2,3} = [W/L]$.

(c) Case 3: $I_{IN} = 10nA$, where $[W/L]_{2,3} = [W/L]$.

(d) Case 4: $I_{IN} = 20nA$, where $[W/L]_{2,3} = [W/L]$.

(e) Case 5: $[W/L] = [W/L]_{2,3} = 0.2 * [W/L]_{1,4}$.

(f) Case 6: $[W/L] = [W/L]_{2,3} = 0.1 * [W/L]_{1,4}$.

(g) Case 7: $[W/L] = [W/L]_{2,3} = 0.05 * [W/L]_{1,4}$.

(h) Case 8: $[W/L] = [W/L]_{2,3} = 0.033 * [W/L]_{1,4}$.

Figure 16: Optimisation results for the 4 MOS squarer of Figure 2. For given I_{IN} current, only one combination of aspect ratios is cancelling the “non-ideality factor”, leading to optimum results.

(a) Case 1: $I_{IN} = 1nA$, where $[W/L]_{2,3,4,5} = [W/L]$.

(b) Case 2: $I_{IN} = 2.75nA$, where $[W/L]_{2,3,4,5} = [W/L]$.

(c) Case 3: $I_{IN} = 6.5nA$, where $[W/L]_{2,3,4,5} = [W/L]$.

(d) Case 4: $I_{IN} = 9.5nA$, where $[W/L]_{2,3,4,5} = [W/L]$.

(e) Case 5: $[W/L] = [W/L]_{2,3,4,5} = 0.4 * [W/L]_{1,6}$.

(f) Case 6: $[W/L] = [W/L]_{2,3,4,5} = 0.2 * [W/L]_{1,6}$.

(g) Case 7: $[W/L] = [W/L]_{2,3,4,5} = 0.1 * [W/L]_{1,6}$.

(h) Case 8: $[W/L] = [W/L]_{2,3,4,5} = 0.05 * [W/L]_{1,6}$.

Figure 17: Optimisation results for the 6 MOS multiplier/divider of Figure 3. For given I_{IN} current, only one combination of aspect ratios is cancelling the “non-ideality factor”, leading to optimum results.

Table 9: List of indicative optimal $[W/L]$ configurations for the 4-MOS multiplier depending on the input current I_{IN} , when $M = 10nA$.

I_{IN} [nA]	Optimal Configuration $IC_{outEKV} = IC_{outIdeal}$
1	$[W/L]_{1,4} = 0.1 * [W/L]_{2,3}$
10	$[W/L]_{1,4} = 1 * [W/L]_{2,3}$
20	$[W/L]_{1,4} = 2 * [W/L]_{2,3}$
40	$[W/L]_{1,4} = 4 * [W/L]_{2,3}$
80	$[W/L]_{1,4} = 8 * [W/L]_{2,3}$
100	$[W/L]_{1,4} = 10 * [W/L]_{2,3}$

In an attempt to generalise the results of Table 9, the qualitative relation (40) has been derived, which provides a useful design rule concerning the ideal operation of the 4 MOS multiplier/divider for a given input current and gain. The effect of the current $I_3 = M$ in (40) can be seen also in the simulation results shown in Figure 12b of the previous section.

$$[W/L]_{1,4} = \frac{I_{IN}(nA)}{M(nA)} * [W/L]_{2,3}. \quad (40)$$

It is worth noting that as mentioned earlier, the results in Figure 15 quantitatively verify that a significant increase of all the $[W/L]$ values of all transistors in the TL loop will lead to significant deviations of the output device IC from ideality, instead of minimising them.

In a similar attempt, the same procedure has been followed for the optimisation results of the 4 MOS squarer and the 6 MOS multiplier/divider TL circuits. Figure 16 and Figure 17, respectively, display the same two categories of results, as Figure 15. Again, unique combinations of aspect ratios - input currents are observed, thus providing the collective optimisation Tables, Table 10 and Table 11.

Table 10: List of indicative optimal $[W/L]$ configurations for the 4 MOS squarer depending on the input current I_{IN} .

I_{IN} [nA]	Optimal Configuration $IC_{outEKV} = IC_{outIdeal}$
1	Any combination leads to optimum results
5	$[W/L]_{1,4} = 5 * [W/L]_{2,3}$
10	$[W/L]_{1,4} = 10 * [W/L]_{2,3}$
15	$[W/L]_{1,4} = 15 * [W/L]_{2,3}$
20	$[W/L]_{1,4} = 20 * [W/L]_{2,3}$
25	$[W/L]_{1,4} = 25 * [W/L]_{2,3}$

After a careful observation of the results shown in Figure 16, summarised in Table 10, relation (41) has been derived, providing a useful design rule to the user, when it comes to the proper selection of aspect ratios for given input currents for the 4 MOS squarer of Figure 2.

Table 11: List of indicative optimal $[W/L]$ configurations for the 6 MOS multiplier/divider depending on the input current I_{IN} .

I_{IN} [nA]	Optimal Configuration $IC_{outEKV} = IC_{outIdeal}$
1	Any combination leads to optimum results
1.75	$[W/L]_{1,6} = 2.5 * [W/L]_{2,3,4,5}$
2.75	$[W/L]_{1,6} = 5 * [W/L]_{2,3,4,5}$
5.25	$[W/L]_{1,6} = 10 * [W/L]_{2,3,4,5}$
6.5	$[W/L]_{1,6} = 20 * [W/L]_{2,3,4,5}$
9.5	$[W/L]_{1,6} = 40 * [W/L]_{2,3,4,5}$

$$[W/L]_{1,4} = I_{IN}(nA) * [W/L]_{2,3}. \quad (41)$$

The high nonlinearity of the 6 MOS multiplier/divider circuit led to non-integer values of input current - aspect ratio combinations, as it can be seen from Table 11. Nonlinear least squares power fitting of the results, produced the following relation for the optimisation of the specific circuit.

$$[W/L]_{1,6} = \sqrt[0.561]{\frac{I_{IN}(nA)}{1.219}} * [W/L]_{2,3,4,5}. \quad (42)$$

7. Summary

By now it should be clear that the impact of transistor-level design parameters upon performance (e.g. gain, distortion - levels) or upon the ideal behaviour can be such, that can certainly not be predicted by the “conventional” ideal equations. The indeed counter-intuitive simulation results underline the need to consider the effect of the transistor-level design parameters more carefully, when a TL topology (static or dynamic) needs to be realised.

Thanks to the EKV-based model illustrated in this paper, the input current - aspect ratio combinations that have been defined, will allow the engineer to design an optimised TL topology that nullifies the deviation between the ideal and realistic operation of the devices. In other words, a more accurate version of the TLP has been articulated, summarised by (38). This EKV-based TLP, led to the design rules (40), (41) and (42).

When considering (38), it is useful to bear in mind that:

- i) a “small” drain current does not necessarily guarantee a “small” IC value. It depends on the aspect ratio of the device it flows through;
- ii) conversely and similarly, a “large” drain current does not necessarily lead to a “large” IC value;
- iii) WI operation is achieved not because of “small” current values that the devices are called to carry, but thanks to small IC values;

iv) the “*non-ideality factor*” incorporates square roots of IC s and not simply IC s; this means that though the IC of a device might be “*small*”, that device contributes to the “*non-ideality factor*” by the square root of its IC which, when $IC < 1$, will result in a “*larger*” eventual value in the “*non-ideality factor*” expression. This practically means that because the non-ideality factor depends on the square root of the inversion coefficient, a 10% deviation from ideality occurs when one of the transistors reaches an inversion coefficient of 1%, which is a current level that is an order of magnitude smaller than the typical current level taken to be the boundary between weak and moderate inversion;

This paper considered the customary transistor model and analysed the behaviour of several TL circuits in the subthreshold regime. For the static TL circuits category, the paper investigated in detail and discussed three generic TL blocks, while for the dynamic TL case, we investigated the behaviour of the logarithmic integrator and correlated its output distortion levels with low-level process parameters. The symbolic approach adopted in this paper can be expanded to describe more complicated static or dynamic TL circuits since, as discussed, retrospective/symmetric relations are generated with the addition of MOST pairs in a TL loop. The symbolic relations presented in Tables 1, 2 and 3, apart from increasing our understanding as far as deviations from ideality are concerned, they are also process - independent and can be used for assessing performance without resorting to Spectre® simulations.

Finally, the optimisation relations/design rules provided in Section 6 illustrate the optimal aspect ratio value to the designer for given input current and TL topologies, allowing later Spectre® simulations to generate results very close to the ideal ones. The essence of usefulness of these optimisation relations is that they can be expanded and tailored for the description of custom TL topologies (static or dynamic), allowing the designer to provide optimisation rules tailored to given topologies.

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