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ABSTRACT

Euclid is a medium class European Space Agency mission scheduled for launch in 2020. The goal of the survey is to examine the nature of Dark Matter and Dark Energy in the Universe. One of the cosmological probes used to analyze *Euclid*'s data, the weak lensing technique, measures the distortions of galaxy shapes and this requires very accurate knowledge of the system point spread function (PSF). Therefore, to ensure that the galaxy shape is not affected, the detector chain of the telescope's VISible Instrument (VIS) needs to meet specific performance performance requirements. Each of the 12 VIS readout chains consisting of 3 CCDs, readout electronics (ROE) and a power supply unit (RPSU) will undergo a rigorous on-ground testing to ensure that these requirements are met. This paper reports on the current status of the warm and cold testing of the VIS Engineering Model readout chain. Additionally, an early insight to the commissioning of the Flight Model calibration facility and program is provided.

Keywords: CCD, Euclid VIS, CCD readout electronics, astronomy

1. INTRODUCTION

Euclid is a medium class European Space Agency mission designed to examine the nature of Dark Matter in the Universe, and that of the Dark Energy causing its accelerated expansion. The 1.2 m Korsch telescope with two instruments on board – a visual imager VIS and a near-IR spectrometer-photometer (NISP) – will be launched in the late 2020 and placed in the second Lagrange point, L2, for a minimum 6 year mission. The main goal of the imaging provided by VIS is to measure the shapes of galaxies. These are distorted by Weak Gravitational Lensing (WGL): the light from distant galaxies may be weakly distorted by mass concentrations in the Universe, altering their apparent shapes by ~1%. Hence this permits the distribution of the yet unknown Dark Matter to be mapped. The evolution of the Dark Energy equation of state can be constrained by the manner in which this distribution has changed over time by looking at further distances (higher redshift). A more complete description of the *Euclid* mission and its scientific goals can be found in [1, 2, and 3]. The current design and status of the VIS instrument is described in [3].

The core of the VIS instrument is made of a focal plane of 36 CCD273-84 designed to operate in the visible light wavelength range between 550 nm and 900 nm. From the WGL point of view it is clear that the imaging will depend on highly controlled and calibratable performance of the VIS detector chain, including a sufficient sampling of the source photons by the detector pixels, high charge transfer efficiency (CTE) in the CCD detectors and low noise and cross-talk readout electronics. Therefore an on-ground characterization and calibration of the *Euclid* VIS CCDs and the related readout electronics is an important step prior to the integration of the flight equipment into a VIS focal plane assembly

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(FPA). The VIS readout chain (ROC) consists of three CCD273s designed and manufactured by e2v Technologies and a readout electronics (ROE) powered by an ROE power supply unit (RPSU), both designed and manufactured at the Mullard Space Science Laboratory (MSSL). An initial evaluation of the electro-optical parameters of the CCDs is performed by e2v using their internal camera system. The evaluation of the VIS ROC performance using flight-like environmental and operational conditions is carried out at MSSL in the framework of two test programs termed the characterization and the calibration campaigns. The first one, the characterization program, is performed to ensure that the CCDs are thoroughly characterized in a range of extended experimental conditions at all development stages. The second, the calibration campaign, serves to evaluate the mission-specific performance and provide the pre-launch calibration files for all flight model (FM) ROCs prior to their integration into the VIS focal plane. In this paper we present the current status of the characterization and calibration programs at MSSL paying special attention to the testing of the engineering model (EM) equipment.

2. VIS READOUT CHAIN

2.1. Description of the design and operation of the CCD273

The CCD273-84 is a 4k x 4k pixel sensor which has been designed specifically for *Euclid* by e2v Technologies based on the previous model CCD203-82[4]. The CCD273 is a back-illuminated, low-noise and high sensitivity device. It has a split frame architecture with four output amplifiers enabling simultaneous readout from the CCD four corners. The pixel size of 12 µm x 12 µm coupled to the telescope plate scale provides high resolution imaging. The readout register has a gate controlled dump drain which allows for a quick dumping of any unwanted charge and this functionality is used for flushing of the CCD matrix prior to an exposure. The CCD273-84 has been further optimized by narrowing the serial register to improve the charge transfer efficiency (CTE), which is especially helpful at the mission end of life (EoL) when the number of traps generated by the Solar and Galactic particle radiation is highest. In addition, in order to mitigate the effects of the radiation damage, an advanced charge injection structure has also been added in the middle of the CCD, between the two halves of the device. This new structure allows for a controlled injection of rows of charge into the CCD matrix, filling up the traps prior to exposure to improve the CTE. The final enhancements introduced in order to boost detector's red response was to use a thicker (40 µm) silicon and optimize the antireflective (AR) Hafnium Oxide coating. A more detailed description of the design of the CCD273 can be found in [4], while the mission electrical and environmental requirements have been provided in [5].

The characterization of the CCDs starts already at the manufacturer site. Each of the development models undergoes a rigorous qualification and acceptance testing at the silicon wafer level and then at the packaged device level. Broadly, the testing includes positioning and geometrical measurements, wirebond pull and tear tests, electrical tests, temperature cycling, visual inspections and optical tests. During the optical tests the following parameters are measured: pixel response non-uniformity (PRNU), image and register area full well capacity (FWC), dark current, number of defects and traps, readout noise, amplifier responsivity, non-linearity, modulation transfer function (MTF), quantum efficiency (QE) and power consumption.

The family of the *Euclid* VIS CCDs consists of several models ranging from the pre-development demonstration model devices, through engineering model (EM), qualification model (QM) (only internal to e2v) and flight model (FM) devices. After first being tested at e2v, the pre-development and EM devices have been distributed among VIS Team and ESA test sites at MSSL, the Centre of Electronic Imaging at the Open University (OU), European Space Research and Technology Centre (ESTEC) and the Commissariat a l'Energie Atomique (CEA). This ensures that the imaging performance of the CCDs is independently characterized by several research teams in similar but not exactly the same experimental conditions. Examples of the already-performed studies can be found in [6, 7, 8, 9, and 10]. Additionally, the OU runs a comprehensive test program assessing the effects of the radiation damage in the CCDs[11, 12 and 13]. However, only at MSSL are the CCDs tested with the *Euclid* readout electronics and power supply at cold temperature, i.e. in truly flight representative conditions[9, 10].

The findings of the test campaigns performed by the above institutes are triannually presented and discussed at the meetings of the CCD Working Group, an advisory group of experts that overviews the development and calibration of the detectors. The operational parameters which are then agreed by the VIS Team to improve the performance of the CCD become the baseline. For example, to improve the readout noise the register readout rate was reduced to 70 kHz instead of the previously used value of 200 kHz. Another example was to slow down the speed of the readout in the parallel direction to ~20 Hz from the original 11 kHz to improve the CTE[11]. This is especially important for the *Euclid* CCDs which are expected to degrade towards the end of the mission, as a result of the development of electron traps in the silicon structure from radiation damage. Additionally, in order to improve the CTE further, the overlapping waveforms of the image clocks were modified to non-overlapping coincident clocks with a tri-level waveform. This ensured that the trapped charge has a greater probability to return to its original charge packet rather than be captured by the subsequent one and hence this reduces the extent of the charge tails after the sources imaged on the CCD[12].

The *Euclid* CCDs will work in three basic operation modes in flight. Most of the time, a standard science mode will be used, in which the CCDs are first flushed to remove any residual charge, then a 565 s image acquisition takes place, after which the charge is read out. There are variations on the exposure time for bias and dark frames, and for flat fields, as well as a variant for the linearity calibration. Two additional operation modes will become more and more useful as the mission progresses: these are the charge injection mode and the trap pumping mode. The above-mentioned charge injection structure can be used to introduce lines of charge into the image area to study the charge transfer inefficiency (CTI). It can also be used to fill up the electron traps prior to readout. In this way, any image features (like galaxies and stars) transferred over the trap will be preserved with less charge loss. The trap pumping also uses the charge injection lines to fill the traps but instead of reading out the charge, it is shifted backwards and forwards by alternating the sequence of the parallel clocks. This action creates pixel dark-bright pairs at the locations of those traps whose release timescales are resonant with the readout rate. This mode can be used for counting of these traps and for their identification based on the trap release constants[13] which serves to identify the species to which they belong.

2.2. Readout Electronics (ROE)

The ROE has evolved over four stages: the DM (development model), EM (engineering model), QM (qualification model) and FM (flight model). In addition, there were three stages of EVM (evaluation model) breadboards and the STM (structure-thermal model). The ROE consists of three parts: two video boards each containing six detector chains interfacing to one half of each of the three CCDs which process the signals up to a digitized output, and a digital board, controlled by a field programmable gate array (FPGA), containing the clocking and housekeeping activities and the spacewire interface to the rest of the instrument. Each is on a separate printed circuit board.

The VIS ROE has been designed with a gain of 3.1 e^- per analog-digital unit (ADU) to match the nominal CCD full well of 200,000 electrons with the full 16-bit analog/digital converter (ADC) range. The input to the ADC for a full range output is 4.8 V. The amplifiers are operated from a +5.0 V & -5.2 V supplies from the RPSU.

The resistors used to set the gain of the amplifier stages are selected to be with 0.1 % tolerance and 25 ppm/^{0}C stability. The tolerance of the ADC's reference is quoted as -1 %/+0.6 % and the stability +/- 15 ppm/^{0}C. The stability elements are more than 10 times better than the charge to voltage conversion factor (CVF) stability of the CCD which is believed to be ~1000 ppm/^{0}C. The EM ROE video chain gain has been measured during the characterisation and ranges from 3.03 to 3.06 with the target being 3.04.

The analogue video chain bandwidth is chosen as a compromise between settling time and noise. The amplifier chain response chosen has a 3 dB bandwidth of 140 kHz when tested with a low level sinewave signal. A special FPGA mode allows the whole chain, from CCD interface to ADC input, to be tested without the correlated double sampler and DC restoration switches being active. This bandwidth gives rise to a gain loss at 70 kpixels/s of 1 % compared to the gain measured at very low frequencies. The 1 % gain loss is acceptable as it is consistent.

The noise voltage presented to the ADC in the absence of an output signal from a CCD, for example when testing the readout electronics alone, will be an AC voltage centred on 0 V. Therefore, in order to digitise this properly, the most negative excursion of the AC waveform must be within the ADC's input range. This gives rise to the need for an ADC

offset, where a 0 V input to the ADC is converted to an output which is a small fraction of the ADC's full scale range. An ADC offset range of 300-600 ADU is specified. Table 1 provides the nominal operating parameters for the 600 ADU offset.

CCD output voltage for CVF of 7.7 µV/e- and FWC of 200 ke-	200 ke- * 7.7 µV/e- =	1.54 V
Max input range of the ADC	4.8V-4.8V*600 ADU/65536 ADU =	4.756 V
Voltage conversion gain	4.756 V/1.54 V =	3.088
ADC available range	65536 ADU - 600 ADU =	64936 ADU
CCD camera gain	200 ke-/64936 ADU	3.08 e-/ADU

Table 1 Nominal operating parameters for the VIS ROE

Similarly for 300 ADUs the transfer gain is calculated as 3.065 e-/ADU
This gain figure is then increased by 1 % to compensate for the settling time loss. The gain for the EM ROEs has been set to 3.04 as saturation was observed with the gain set to 3.1.

The readout noise for each detection chain is specified to be ≤ 4.5 e-. After the contribution of the CCD readout node, the noise contribution component for the ROE alone is specified to be 2.51 e- which after the gain factor is accounted for results in a maximum noise component of less than or equal to 2.51 e- / 3.08 = 0.81 ADUs. Most of this will be absorbed by the digitisation noise from the selected 16 bit ADC of 0.7 ADU, leaving 0.4 ADU in quadrature. To achieve the noise requirement, the ROE uses linear voltage regulators for the supplies from the RPSU supplying the analogue video stages. This is more effective at reducing supply line noise than passive filtering alone. Along with the filtering, careful grounding techniques are used to ensure that the noise currents shunted by decoupling components do not enter the amplifier chains. The 3.3 V and 1.5 V supplies that operate the ROE digital circuitry are not regulated locally as they are far less susceptible to power line noise.

The ROE contribution to CCD charge measurement non-linearity measured across the full range is specified to be lower than 1 %. The non-linearity of the ROE video electronics has been examined by varying the input voltage to the VIS ROE circuit from 0V to a maximum expected CCD output and the ADC output is measured in ADU units. Results (Figure 1) show that the nonlinearity lies within the requirements.

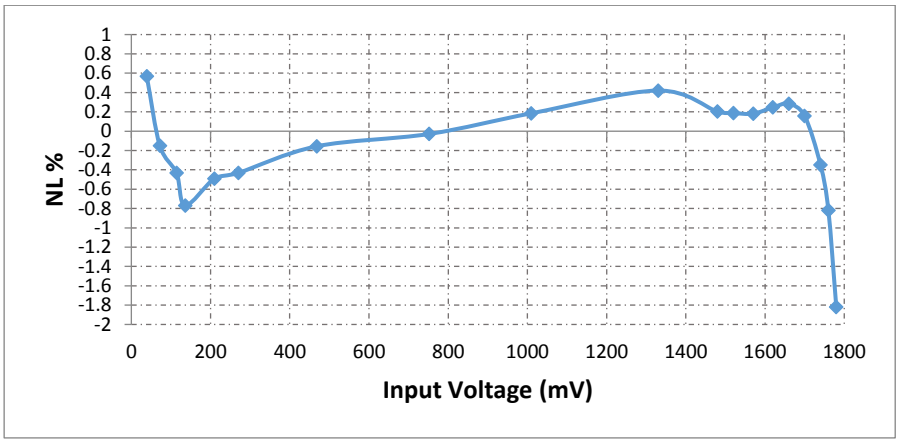

Figure 1: VIS ROE non-linearity

The power consumption for the EM model relies on measurements taken during the EM Full Functional Test within the characterisation programme. Three cases were considered, namely idle (as when an exposure is under way), flushing and readout. The dissipation per ROC (12 CCD outputs) was 6.97, 7.29 and 7.41 W respectively. It is important to note that priority has been given to thermal stability rather than absolute minimum average power consumption. To optimise stability, all ROE circuitry including the ADCs are kept operational all the time. The ADCs dissipate typically 220 mW

each but the option to shut them down during CCD observation was not selected in the interest of maintaining a stable thermal environment.

The other primary function the ROE provides is the ability to drive the required clocks that the CCD demands. The FPGA produces all the necessary clocks for the CCD and the Video PCBs clock drivers. This function is performed primarily on the Video PCB where the CCD drivers are located. These drivers are located as close to the CCD connector as possible to minimise the risk of electromagnetic interference to the ROE CCD input chains and reduce parasitic effects across the circuit boards. The FPGA is also responsible for the housekeeping of the CCD, ROE and RPSU bias voltages. Finally, the FPGA enables communication with the command and data processing unit (CDPU).

2.3. Readout Electronics Power Supply Unit

One readout electronics power supply unit (RPSU) provides power for one ROE and three CCD273s. There are two driving requirements on the RPSU design. The first is the output noise requirement. As the switching power supply is the primary source of noise in the detection chain, a low noise power supply is essential for the entire electronics system to achieve the noise budget. RPSU uses the FORWARD topology rather than the FLYBACK. To achieve sufficient full frequency band noise rejection, the control loop is designed and carefully tuned to work with the output passive filter to cover the entire frequency band.

The other driver is the multiple secondary rails required by ROE. Because the space within the mechanical enclosure is limited, and space is reserved for the filters, there is insufficient room to host multiple converters so the RPSU contains a single converter with multiple outputs. This imposes a technical challenge in cross-regulation between the secondaries as only one secondary can be directly regulated in a single converter. This cross-regulation is achieved by using a planar transformer and inductor. The proximity of each winding within the planar PCB means very low leakage inductance and very good magnetic coupling which results in good cross-regulation. However, the side effect of this good coupling between primary and secondary provides a path for generating common mode (CM) noise, which causes excessive degradation on noise performance inside the ROE. This problem was resolved by enhancing the CM filter inside RPSU and ensuring a symmetric design between the output lines.

The RPSU has evolved over four stages: pre-EM (prototype engineering model), EM (engineering model), QM (qualification model) and FM (flight model). In addition, there was a STM (structure-thermal model),

3. VIS ROC ON-GROUND CHARACTERIZATION AND CALIBRATION PROGRAMS

The characterization is performed on a limited number of devices requested from e2v at different stages of the CCD development. The CCDs are paired with the most recent models of the readout electronics available at MSSL. There are several reasons to run detailed characterization tests before the start of the calibration of the flight devices. Firstly, from the mission point of view, an early testing of a complete readout chain ensures its correct operation and verifies basic mission requirements. At the same time it provides a quick feedback of the performance of the readout electronics. Secondly, it provides a large set of data acquired at extended operational and environmental conditions from which a broad knowledge of the CCD working principles can be withdrawn. This data can then be looked at and discussed by the MSSL scientists and members of the *Euclid* CCD working group to decide what shall be the optimal operation conditions in flight.

The calibration program is realized as a set of measurements performed on all FM readout chains in the flight configuration to confirm the functionality of the ROC operation in all readout modes and to verify the mission requirements.

4. STATUS OF THE VIS EM ROC CHARACTERIZATION PROGRAM AT MSSL

4.1. Description of the Characterization Test Equipment at MSSL

The operational conditions of the VIS CCDs in orbit require that the temperature of the devices is stabilized at ~ 153 K while the ROE and RPSU are at room temperature; the whole readout chain is in vacuum. We have replicated these conditions in the characterization vacuum chamber at MSSL so that the CCDs are kept at a temperature of 153 K by means of a controlled liquid nitrogen cooling while the temperature of the readout electronics is maintained at approximately 300 K. Because of the size limitation of the test chamber, only two CCDs and one ROE can be fitted inside and connected at a

time. The interior of the characterization chamber is shown in Figure 2. The CCDs are mounted one above the other on a metal plate equipped with temperature sensors and heaters. The plate can be moved vertically and horizontally by a set of motors located behind it. The ROE is placed behind the motors at the back of the chamber. The RPSU is replaced by a set of benchtop power supplies. The LN_2 dewar is positioned below the vacuum chamber (not visible in the picture) and is thermally separated from it, with only two metal cold fingers extending through a metal baseplate, one each for cooling of the CCDs and the ROE. The CCDs are illuminated through an optical port in the chamber wall by a set of LEDs mounted in an externally attached optical bench. The flat-field measurements are performed with a diffuser mounted in front of the LED. For the detector PSF measurements, the diffuser is removed and a pinhole is introduced to the optical path at a distance of approximately 30 cm from the CCDs and an objective lens is placed at a distance of ~ 7 mm from the CCD surface. A more detailed description of the experimental setup can also be found in [10].

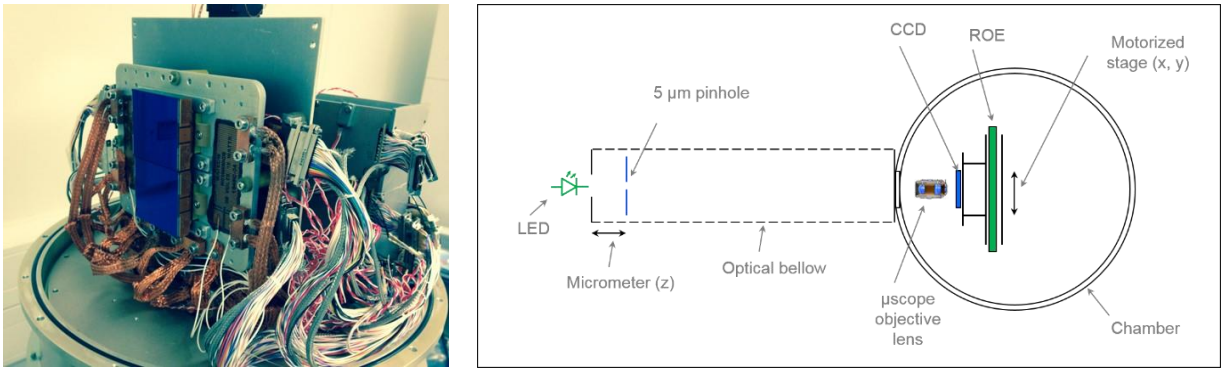

Figure 2 Interior of the CCD273 characterization chamber at MSSL (left) and optical setup for the PSF measurements (right).

The warm testing of the complete EM readout chains is performed on a clean room bench and at ambient temperature and pressure. Two EM ROCs first undergo a set of electrical, functional and EMC testing at MSSL before they are assembled into a VIS EM plane at CEA. Figure 3 shows the EM test setup at MSSL. The CCDs are mounted in a row on a test beam and connected to the ROE via two flexi leads as shown in Figure 3 left. Next, the RPSU is mounted on the side of the ROE box and connected to the ROE via a 37-way MDM connector. The ROE is also connected to a laptop via a SpaceWire interface which enables communication with the FPGA for sending commands and receiving data.

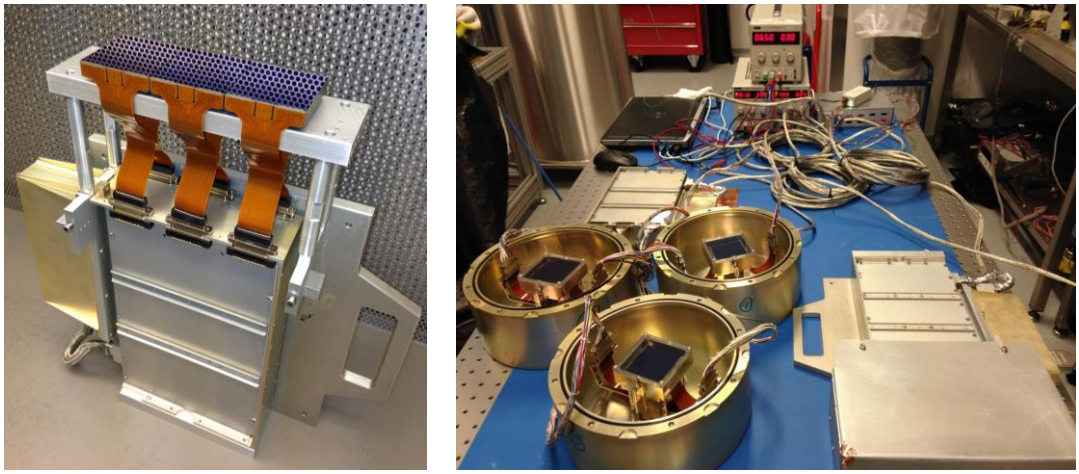

Figure 3 VIS EM readout chain assembly (left) and EM test setup for warm testing (right).

The data acquisition software ELVIS (*Euclid* LabView Imaging Software) has been written specifically for *Euclid* at MSSL using LabView. The software commands are in line with the commands provided by the FPGA registers and allow for a flight-representative operation of the CCDs. While the clock waveforms are hard coded in the FPGA, the speed of the

parallel readout given by a t_{oi} parameter (in the e2v nomenclature known as the image clock pulse edge overlap) is programmable. The number and frequency of the charge injection lines (if any are required) can be set by the user. The trap pumping activity is controlled by the number and speed of the shuffles in the parallel and serial directions. By varying the frequency of the shuffles different trap species can be characterized. The software enables two types of data acquisition – manual and automatic. The later has considerably reduced the amount of time that an operator would need to spend collecting the images one by one. Instead, the test campaign can be scripted in advance and the individual tests can be run in a sequence with minimal supervision. This approach has been adopted with the calibration (as opposed to this characterisation) program in mind, in which each of the twelve FM ROCs will be tested in approximately one week on a 24 hours basis.

We now report on the current status of the warm and cold testing of the engineering model (EM) equipment. The results of the characterization of the previous ROC models can be found in [9, 10]. The EM CCDs, EM ROEs and EM RPSUs are considered to be mechanically, thermally and electrically flight representative.

4.2. Warm testing of the EM ROCs

The detector chain readout noise has been measured by reverse clocking of the CCDs and measuring the standard deviation of the acquired image. The back-clocking of the charge is realized by swapping two serial clocks so that the sequence is RΦ1 – RΦ3 – RΦ2. This allows for a measurement of the entire chain noise including the CCD readout node while avoiding dark current generation in the image at room temperature. The CCDs were also operated in complete darkness to avoid generation of charge in the serial register by the room lights. The noise measured in this way is ~ 4 e^-, which is in line with an overall requirement of 4.5 e^-.

At room temperature some of the useful imaging can be done in a normal forward-clocking mode (despite the generation of the dark current) by reading out small regions of the CCD, while dumping the charge from the others. This functionality is enabled in the FPGA commanding on a line by line basis, allowing the selection of the number of lines to be read out. The limited scan option allows for a sequential checking of the imaging capabilities of all regions of the CCD at room temperature. The charge injection functionality is also verified for the entire area of the CCD in this way. Sample images acquired during the EM functionality testing are shown in Figure 4.

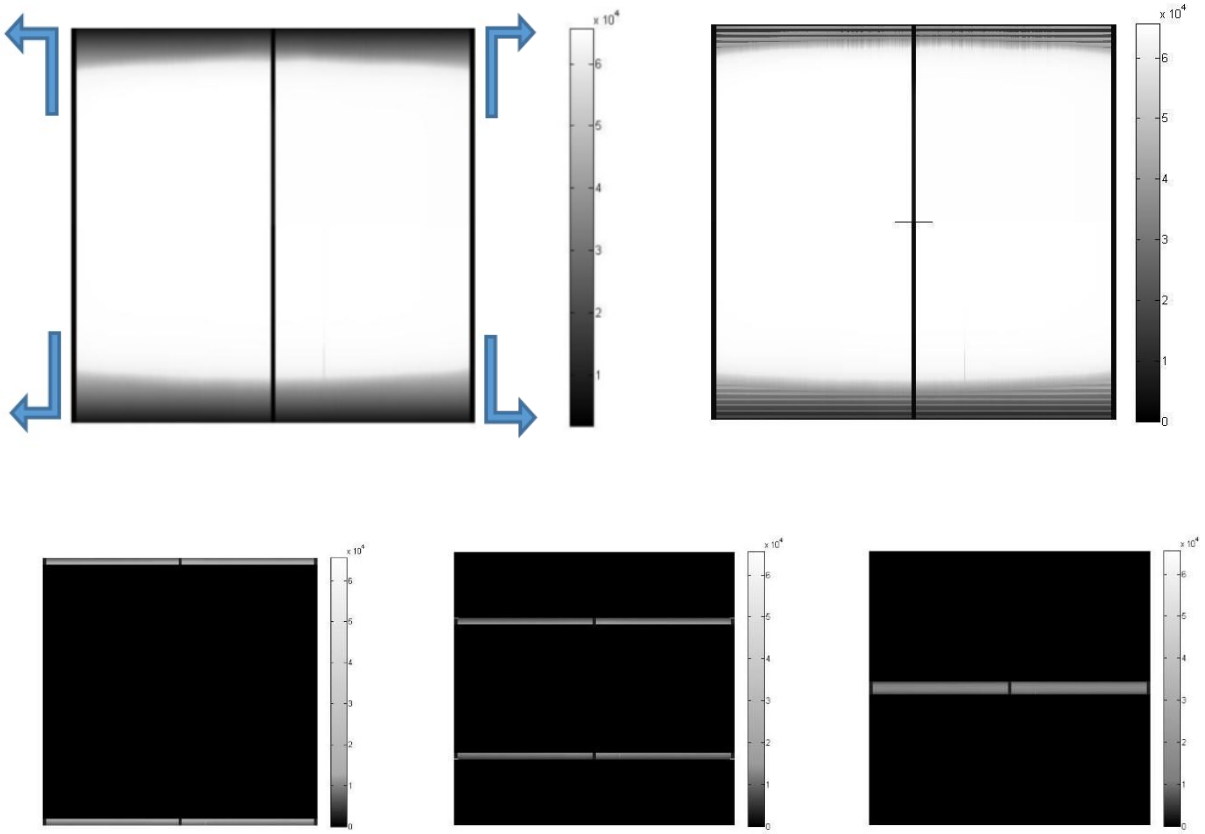

Figure 4 Sample images obtained while performing room temperature functionality checks of the VIS EM ROCs. Upper left – regular warm image (the readout direction is from the middle of the CCD towards the four corners as shown by the arrows). A vertical gradient because of dark current generation during the readout is evident; the dark vertical stripes at the sides and in the middle of the image correspond to the pre-scan and over-scan columns, respectively. Upper right – a typical charge injection image obtained with a pattern of 30 lines with charge followed by 20 lines without charge (visible only in the non-saturated regions of the image). The bottom three images show examples of the limited scan mode, in which a limited number of image rows (from left to right: at the top, middle and bottom of the four quadrants) with low dark current signal.

One of the design challenges related to the DM and EM generations of ROE was the electrical cross-talk between different channels reading different CCD quadrants. As a result, ghost images were seen in some CCD quadrants. An example is shown in Figure 5, in which a bright saturated source has been placed in front of the CCD H quadrant, and a similarly shaped, but much fainter image is seen in the other quadrants, with the G quadrant being the most prominent. After a close inspection of the ROE layout, it was identified that this was caused by magnetic coupling of the inductors on the video board first stage CCD signal filter and two-stage Bessel filter. The physical layout of the components has been changed so that the inductors of the neighboring are now separated and placed at a 90° angle with respect to each other. Also, the tracks between the second stage of the Bessel filter and the ADC that were close to each other in different channels have been separated. To test the effectiveness of the layout changes at room temperature, a test has been performed in which a well-defined CCD-like artificial signal has been injected into one of four OS pins of the ROE channels operating one CCD and the level of the cross-talk in the other 3 channels has been measured. After introducing the modifications, an injection of a signal level corresponding to ~48 kADU the worst cross-talk measured in the neighboring channel was 0.3 ADU, with the other two channels showing a negligible cross-talk. The layout changes have proven effective and will be introduced in the next model of the ROE, the QM.

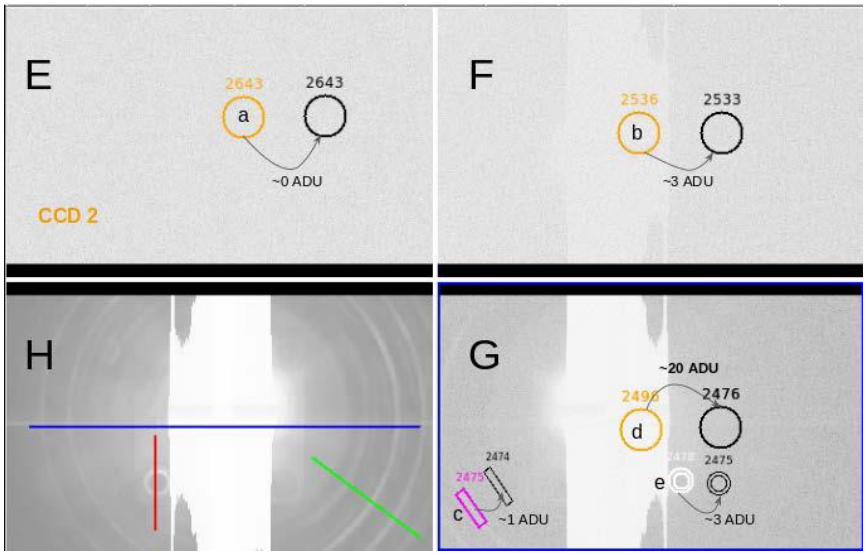

Figure 5 EM image showing an example of the cross-talk. An image of the real light source can be seen in the H quadrant, while a similar mirrored image is also clearly seen in the G and F quadrants. Note that the brightness scale in the G quadrant has been enhanced so that otherwise faint ghost image would be difficult to see.

In order to ensure that the EM ROE and RPSU meet standard and mission regulations in terms of the electromagnetic compatibility (EMC) a complete testing of the conducted and radiated emissions and susceptibility of the EM ROCs was performed by the MSSL and CEA teams. The conducted emission on the power and power return leads was verified for a frequency range between 30Hz and 100MHz. In the susceptibility testing, on the other hand, the electronics is presented to a range of frequencies originated from other S/C equipment which could potentially cause malfunction to the ROC's normal operation. This susceptibility testing has been performed on the integrated EM, which consists of 2 blocks mounted side by side, like in the FM configuration, each block (also mounted like the FM), being made of 3 CCDs read by one ROE and powered by one RPSU. The EMC testing has shown some cases of susceptibility slightly above the requirements for a few CCD quadrants; they were considered as non-critical and to be investigated further when EMC testing will be done at the full instrument integrated level.

4.3. Cold testing of the EM CCD and EM ROE

Although many specific cold tests of the detection chain have been carried out over the last years, the cold testing of the EM CCD and ROE at the formal characterization level has only recently started at MSSL and will take approximately 4-5 weeks, after which time a complete EM test report will be issued for an internal review within the *Euclid* consortium.

Figure 6 shows an example of a "master" flat field obtained by averaging a large number of individual flat fields, as a function of wavelength. The small area features visible in the images are remnants of the CCD manufacturing process. The dark horizontal and vertical lines called stitching edges are caused in the lithography process in which the electrode pattern is projected onto a wafer in small stitching blocks. The diagonal pattern, the amplitude of which decreases with the wavelength, is a result of the CCD back-side laser annealing process. At redder wavelengths, a pattern of concentric rings called "tree rings", starts to be visible. The widely accepted explanation for the appearance of these is because of the silicon resistivity variations during the growth of the silicon crystal. The amplitude of the tree rings was measured by performing a detailed analysis of the master flat-fields in the frequency domain using Fast Fourier Transform (FFT). Typical amplitude (peak-to-peak) of the tree rings is ~5×10^{-4}, with a maximum of up to 10^{-3}. The width of the rings (valley to valley) is approximately 10 pixels. An amplitude of 5×10^{-4}, if resulting from a change in pixel size, leads to a linear distortion of 2×10^{-4}. An amplitude of 10^{-3} would be equivalent to a distortion of 5×10^{-4}. The requirement on average distortion, on scales of 1 arcsec (10 pixels) is 3%, well above these values, but the requirement on residual distortion at scales of 4 arcmin is 3×10^{-5}. To compare with the requirement, it would be necessary to average the (assumed) distortion effect of the tree-rings over those scales. Given that in 4 arcmin there are approximately 240 tree rings, and these are not perfectly regular, their

contribution is probably well below the local distortion figure, and also within requirement, but a detailed assessment of the impact of these tree-rings on the shape measurements is on-going.

The pixel-to-pixel non-uniformity (PRNU) is wavelength dependent and ranges from 0.95 % to 0.6 % for 545 nm and 850 nm, respectively.

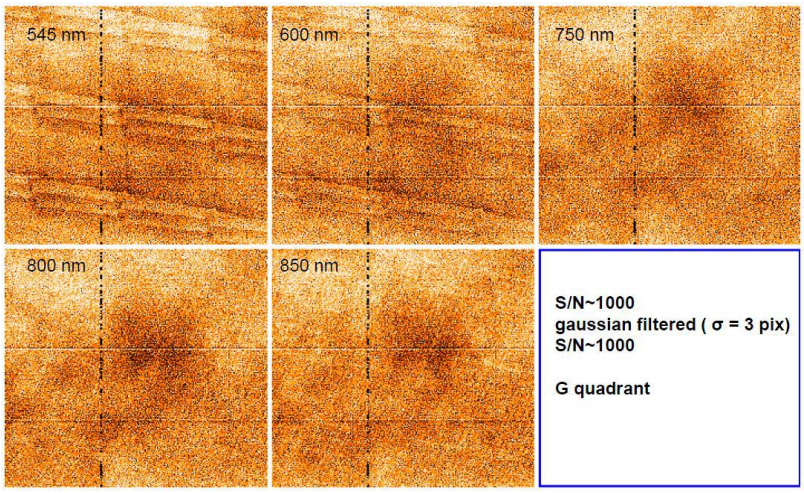

Figure 6 Wavelength dependency of the flatfield

5. CURRENT STATUS OF THE MSSL CALIBRATION PROGRAM

The calibration (as opposed to the characterization discussed above) of the FM readout chains will be performed at MSSL. The facility is currently under construction and commissioning. A large vacuum chamber has been selected to allow for mounting of an entire FM ROC in a flight representative configuration. The cooling is provided by a 17 liter LN_2 dewar allowing for an uninterrupted cold testing of at least 12 hours. Separate LN_2 cooled scavenger plates are to be placed near the CCD mounting plate to attract potential molecular contamination away from the CCD surface. The ROE and RPSU are cooled by a separate weaker thermal link from the LN_2 dewar. The chamber is fitted with a pressure gauge, a pumping set allowing for a high vacuum up to 10^{-6} mbar, and a temperature controlled quartz crystal microbalance (TQCM) device and a residual gas analyzer (RGA) for contamination monitoring. The facility is located in an ISO 8 cleanroom and will additionally be placed within a cleanroom tent to maintain a cleanliness level of ISO 5 during the assembly of the FM readout chains. The thermal and vacuum commissioning of the chamber is currently being performed at MSSL.

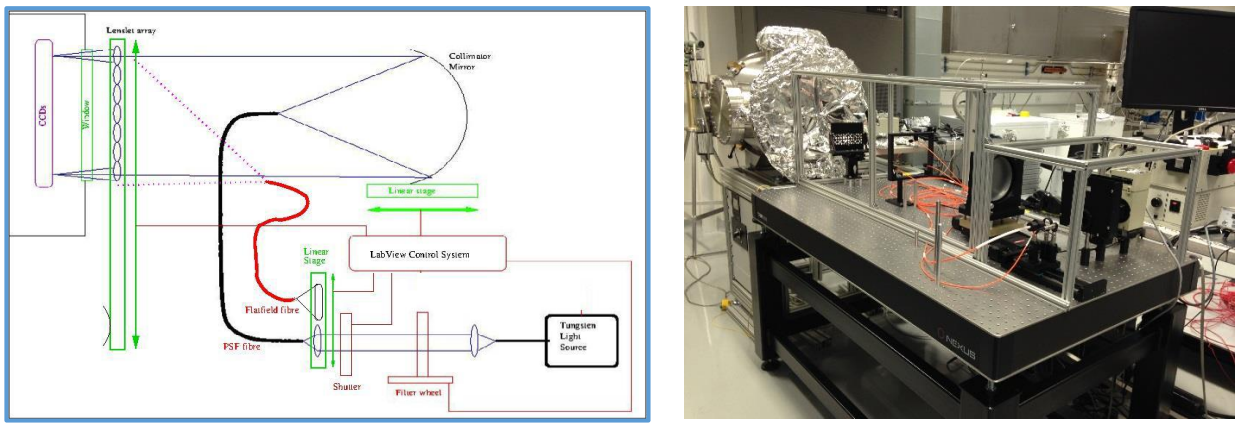

Figure 7 Conceptual schematic of the Euclid PSF and flatfield calibration setups (left) and its practical realization in the cleanroom (right)

The optical setup has been designed in collaboration with the Centre for Advanced Imaging at Durham University (DU). All optical elements were manufactured at DU and commissioned at MSSL at the beginning of March 2016. A schematic layout of the optical setup is shown in Figure 7. The light emitted by a high power stabilized tungsten lamp feeds a collimating lens and a 6-position motorized filter wheel. At this stage the beam is led onto one of two possible paths, one for PSF measurements and one for flatfield measurements. For the PSF measurements, the collimated filtered light is focused onto a 100 µm multi-mode fiber which then illuminates a 150 mm diameter f/4 parabolic collimator mirror. The mirror is mounted in a commercial cell on a linear translation stage to allow refocusing between different filters. The collimated light is incident on a milled support block into which are mounted 60 small achromatic lenses (5 per CCD quadrant) which provide near-diffraction limited spots. The block is mounted in a commercial tip-tilt mount to provide tip and tilt regulation/control about the optical axis of the collimated beam. The optical design has been optimized in Zemax in terms of the chromatic aberrations across the filter bandpass and the effect was negligible. The size of each of the PSF spots expressed in full width at half maximum (FWHM) is expected to be at around 15 µm. An example of a spot measured with a 3 µm pixel CMOS sensor with the setup at DU is shown in Figure 8 - top left, while an image of a slightly defocused (not yet full optimized) spot acquired with the CCD273 at MSSL is shown in Figure 8 – top right. For the flatfield measurements, the lenslet array is removed from the beam and an even illumination across 3 CCDs is provided by 3 ball-lens-ended large diameter fibers mounted on a rectangular frame at a distance of ~ 40 cm from the CCDs. In Figure 8 it is shown how the use of ball lenses improves the flatness of the illumination across the 3 CCDs.

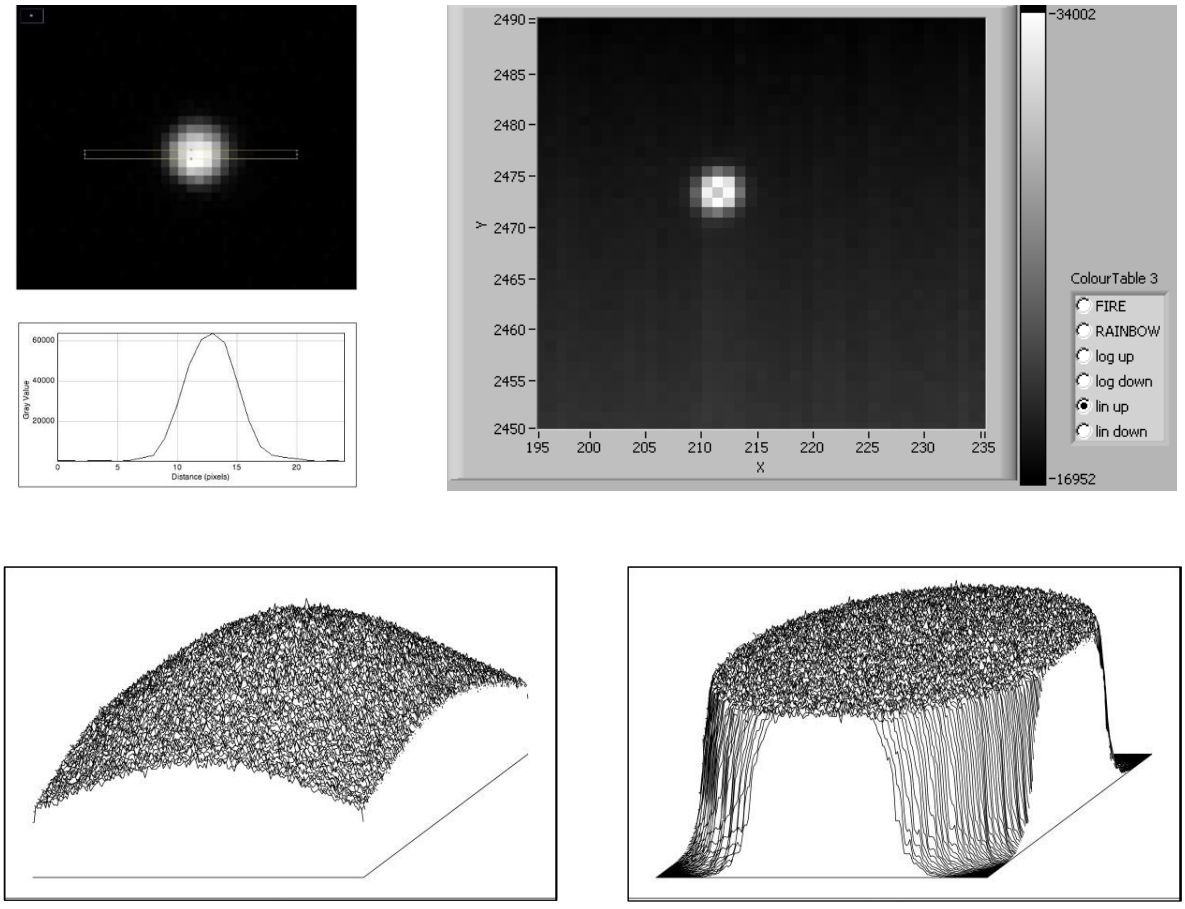

Figure 8 Expected shape and size of the PSF spot (top left), slightly defocused PSF spot obtained with the CCD273 (x, y axes correspond to pixel numbers) and a simulated shape of the flatfield flatness across three CCDs without (bottom left) and with (bottom right) the use of the ball-lensed fibres.

SUMMARY

The on-ground testing of the VIS readout chain is realized at MSSL by means of the characterization and calibration campaigns. A status of the warm and cold characterization of the VIS EM readout chains has been given. The EM devices present functional and imaging capabilities as expected from an EM program with excellent overall performance and some remaining issues. The cross-talk issue identified in the EM ROE has been addressed and the improvements have been introduced in the design of the next QM model. The two EM ROCs have been integrated into a reduced size VIS EM focal plane and are awaiting further testing at instrument level with other VIS EM equipment, including the shutter (RSU), command and data processing unit (CDPU), payload and mechanism control unit (PMCU) and the calibration unit (CU). In parallel with the characterization activities, the calibration facility for the FM readout chains is being constructed and commissioned at MSSL and we have briefly described the calibration setups for the flatfield and PSF measurements.

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