Monolithically integrated heterodyne optical phase-lock loop with RF XOR phase detector

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Abstract: We present results for an heterodyne optical phase-lock loop (OPLL), monolithically integrated on InP with external phase detector and loop filter, which phase locks the integrated laser to an external source, for offset frequencies tuneable between 0.6 GHz and 6.1 GHz. The integrated semiconductor laser emits at 1553 nm with 1.1 MHz linewidth, while the external laser has a linewidth less than 150 kHz. To achieve high quality phase locking with lasers of these linewidths, the loop delay has been made less than 1.8 ns. Monolithic integration reduces the optical path delay between the laser and photodiode to less than 20 ps. The electronic part of the OPLL was implemented using a custom-designed feedback circuit with a propagation delay of ~1 ns and an open-loop bandwidth greater than 1 GHz. The heterodyne signal between the locked slave laser and master laser has phase noise below −90 dBc/Hz for frequency offsets greater than 20 kHz and a phase error variance in 10 GHz bandwidth of 0.04 rad^2.

OCIS codes: (060.2840) Heterodyne; (130.0130) Integrated optics; (060.1660) Coherent communications; (250.5960) Semiconductor lasers; (250.5300) Photonic integrated circuits; (250.0250) Optoelectronics.

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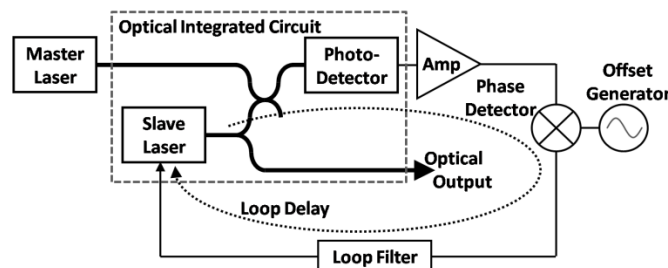
1. Introduction

Fig. 1. A schematic diagram of OPLL implementation (thick lines represent optical paths and thin lines represent electrical paths).

An optical phase-lock loop (OPLL) synchronises the phase of a laser to that of an external, optical signal [1–4]. This is highly desirable for recovery of carrier signals in coherent optical communications [5]. OPLLs also find applications in microwave photonics [3] and in the creation of spectrally pure signals in the mm-wave and THz frequency ranges via photomixing [6,7].

As shown in Fig. 1, an OPLL works by minimising the phase difference between the slave laser and the external signal (master) through a feedback loop. In this variant, the heterodyne between master and slave lasers is detected by a photodetector of bandwidth greater than or equal to the highest required offset frequency. The detected heterodyne is compared with an electrical offset frequency source in an electrical phase detector and the output used to control the slave laser via a loop filter that controls the loop dynamics. This technique is similar to the phase-lock loops found in many electronic systems [8].

It is desirable to use semiconductor diode lasers for OPLLs since they are cheap, compact and can be easily phase controlled using current injection [6, 9]. However, semiconductor lasers generally have linewidths of several megahertz, which places severe constraints upon the loop delay and bandwidth of an OPLL [7, 10]. Hence, narrow linewidth external cavity lasers have frequently been employed in OPLLs [2]. More recently sub-MHz linewidth distributed feedback (DFB) lasers have become available, but these suffer from limitations to their phase control bandwidth in the low megahertz range due to phase reversal, thus limiting their usefulness for OPLLs [6]. Finally, we note that an alternative technique to achieve phase-locking is optical injection of the master signal into the slave laser after which only a slow feedback loop is required in order to keep the slave laser phase locked [11, 12]; however this technique offers no offset frequency tuneability except via an external optical modulator.

The following example demonstrates the difficulties of using wide linewidth lasers. To achieve a phase-error variance of less than 0.03 rad^2 in a bandwidth of 10 GHz using a first-order OPLL, the linewidth–delay product should be ~3 MHz.ns [7]. For a combined slave and master laser linewidth of 1.25 MHz, as in the experiments presented here, the total loop delay must therefore be less than 2.4 ns and the loop noise bandwidth greater than 175 MHz [10]. The short delay time prohibits the use of fibre optic coupled systems since 2.4 ns delay is equivalent to only 0.5 m of optical fibre and the electronic delay of the feedback loop must also be allowed for. Previously, miniaturised free space optics have been utilised to meet

these requirements on the loop delay [6, 13]. More recently, the possibilities of photonic integration have been investigated in order to reduce the delay time of the loop [7, 9]. In [7], hybrid integration has been employed whereby the lasers and photodiodes are separately fabricated and then mounted upon a motherboard containing optical and RF waveguides and electrical connections. This approach allows the performance of the components to be separately optimised, but there can be difficulties in the optical alignment of components. In contrast, with monolithic integration the photonic components are fabricated on a single substrate, allowing the optical elements to be even more tightly packed than using hybrid integration, and presenting fewer alignment issues. However the challenge is then to construct a tuneable laser and a high-bandwidth photodiode on the same substrate, and to achieve high electrical isolation between the components. In the long term, monolithic integration is expected to be a cost effective method of producing integrated optics, since multiple systems could be grown on a single wafer. In [9] an OPLL with monolithic integration of lasers, semiconductor optical amplifiers, optical modulators and photodiodes used as homodyne phase detectors has been demonstrated. The photodiode phase detector approach allows OPLLs to be realised with simple external electrical loop filters and removes the requirement for special, low propagation delay, electronic circuits. The electronic phase detector OPLL design used in the present work offers advantages over the photodiode phase detector approach. First, the technique is insensitive to offset voltages generated in the photodiodes. Second, loop gain can be increased using radio frequency rather than offset-error prone direct current (DC) amplifiers. Third, electrical phase/frequency detectors can be incorporated to give automatic lock acquisition. Integration, both monolithic and hybrid, offers benefits due to improved stability of the system against thermal variations and vibrations. Once constructed, alignment between the integrated components is fixed and the compact size of the photonic integrated circuit (PIC) allows the whole system to be easily temperature controlled. Also, integration allows optical polarisation to be well defined and maintained, making active polarisation control unnecessary.

This paper describes a monolithically integrated OPLL. After discussing the design of the optical components and the RF circuits, results are presented, including measurements of the phase noise on the heterodyne signal between the master and slave lasers.

2. Monolithic integration of photonic components

The photonic elements were defined on the same InP substrate as shown in Fig. 2. These are a laser diode, a photodetector and single-mode optical waveguides, including two Y-junctions. The final chip is only 3.1 mm long and has a 1.4 mm waveguide between the laser and detector with an estimated optical time delay of 16 ps.

The phosphorous quaternary active regions of laser and detector were first grown by metal-organic vapour phase epitaxy (MOVPE) of InGaAsP on the InP substrate. Subsequently, the laser, detector and optical waveguides were defined using photolithography, wet-etch and selective regrowth by MOVPE. Finally the grating sections were defined via electron beam lithography.

The laser is a buried-heterostructure distributed Bragg reflector (DBR) laser with four sections: rear grating, phase, gain and front grating. This allowed the laser to be tuneable by 6 nm (although this was not exploited during the measurements of the phase locking performance). The laser wavelength is centered at around 1553 nm and produces ~4 mW output at 90 mA drive current allowing for waveguide losses. The laser was designed to have
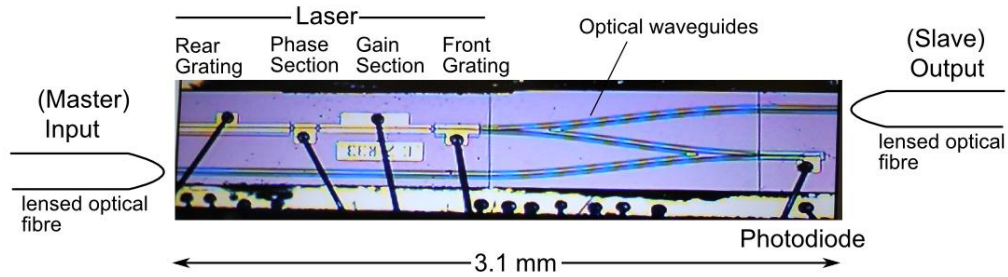
Fig. 2. (color online) Micrograph of photonic integrated circuit, consisting of a monolithically integrated laser and photodiode.

a sub-megahertz linewidth; the sample tested in this paper had a linewidth of 1.1 MHz (full width at half maximum) when all sections except for the gain section were short-circuited, when measured using the delayed self-heterodyne method with a 5 km delay.

In operation, the master and slave laser signals are combined through a Y-junction on the photonic circuit, and the resulting heterodyne signal is detected by the integrated photodiode (Fig. 2). The detector is a 10GHz bandwidth photodiode, fabricated in a ridge waveguide structure. Since the detector is operated in reverse bias and the laser sections are forward biased, it is important for good electrical isolation to be achieved between these components [14]. The electrical resistance between the laser and the photodiode was measured at ~40 kΩ, and the resistance between the different laser sections was ~160 Ω. For 90 mA laser gain section current, the integrated photodiode gave 435 μA photocurrent at 1.5 V reverse bias, whereas the optical power in the output fibre was −11 dBm due to losses in the waveguides/couplers and fibre coupling.

The fabricated PIC was connected with the electronics printed circuit board (PCB) via coplanar waveguide lines designed to carry the high frequency signals (DC-6 GHz) from the photodiode and the control signal back to the laser phase section (Fig. 3). In all of the experiments the chip temperature was stabilised at 21°C using a Peltier cooler. Light was coupled into and out of the PIC using lensed fibres.

3. Design of the OPLL

The OPLL uses an electronic feedback loop to control the phase of the slave laser in order to synchronise it with the master laser, as shown in Fig. 1. A wide bandwidth photodiode is required, since this is an heterodyne system, where the lasers are separated in frequency by up to several GHz, and also since the relative phase noise of the two signals has frequency content up to hundreds of megahertz. The photodiode output is then amplified prior to being compared with an external RF signal in an exclusive-OR (XOR) logic gate phase detector [7]. The resulting baseband error signal is fed through the loop filter, which processes the feedback signal in order to control the slave laser frequency to achieve phase lock [8].

Semiconductor diode laser emission frequency can be adjusted by varying the current to the gain section or through current injection into a dedicated phase or tuning section. The slave laser in this OPLL is tuned by a phase section. This is preferable since the tuning coefficient of the gain section typically displays a sign inversion in the 0.1 MHz to 10 MHz region, due to the opposite signs of the thermal and charge injection tuning mechanisms [6, 9]. This would limit the loop bandwidth and hence the laser phase noise reduction that could be obtained.
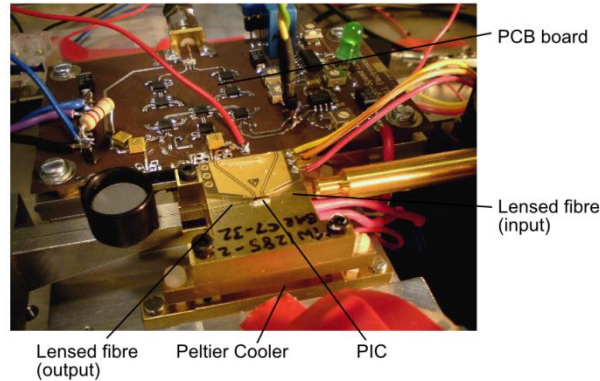
Fig. 3. (color online) The realised OPLL; the complete system occupies 8 cm x 9 cm (not including the lensed fibre positioners, power supplies or RF synthesizer). PIC – photonic integrated circuit.

In order for the loop to operate successfully, it must have a closed-loop bandwidth large enough to track phase variations from the master and slave lasers with low residual error (the offset generator linewidth is negligible by comparison). This bandwidth is determined by the open-loop bandwidth of the loop components, the filter response, the loop gain and the loop delay. The loop delay is a limit on the bandwidth since the loop cannot track changes faster than this time scale.

Photonic integration enables the optical delay to be reduced to less than 20 ps, but it is still a significant challenge to keep the electronic delay close to 1.0 ns, as required for high quality phase-locking when the summed linewidth of the lasers is 2 MHz [7]. This was achieved here by splitting the loop filter into a faster proportional path and a slower integrating path; the first has low delay and high bandwidth to track fast changes, while the second tracks slow changes to the slave or master frequencies, and has correspondingly less restrictive delay requirements. In addition, there is an automatic lock-acquisition circuit. The circuit was implemented using 10 Gb/s emitter coupled logic and current mode logic integrated circuits [7, 15]. The circuit was designed to operate on input signals between 2 and 7 GHz and the proportional path has a 3dB open-loop bandwidth greater than 1 GHz. The overall loop delay is estimated to be less than 1.8 ns, once some additional electrical propagation delays are included.
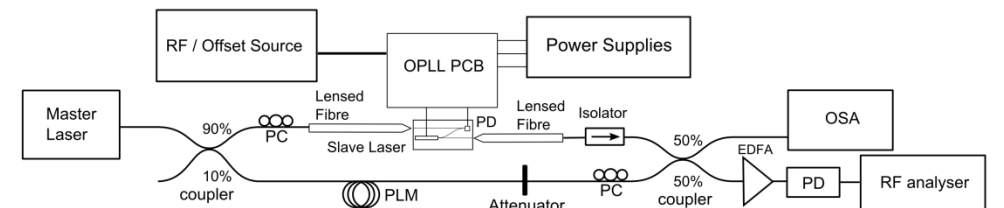

Fig. 4. (color online) Experimental arrangement. PD – photodiode; PC – polarisation controller; OSA – optical spectrum analyser. PLM – path length matching. The paths were matched to better than 1 metre.

4. Testing and results

The OPLL was tested by measuring the heterodyne of the master and slave lasers using an RF spectrum analyser and high bandwidth photodiode (> 20 GHz) as shown in Fig. 4. The polarisation controllers allowed the heterodyne signals to be maximised by aligning the polarisations of the signals. A dramatic narrowing of the heterodyne linewidth occurred when the slave laser was locked to the master laser. The OPLL was able to lock with offset frequencies from 0.6 GHz to 6.1 GHz, limited by the frequency range of the electronic circuit

[7]. Two different master lasers were successfully used during experiments; an external cavity laser (FWHM ~100 kHz) and a narrow linewidth DFB laser (FWHM ~150 kHz). The external cavity laser was frequency stable to within 10 MHz, fluctuating at rates up to 1 kHz. The DFB laser had an unstable absolute frequency that varied by ~1 GHz but fluctuation spectral content was mostly below 100 Hz. Linewidths were measured using a self-heterodyne technique with 5 km fibre-delay.
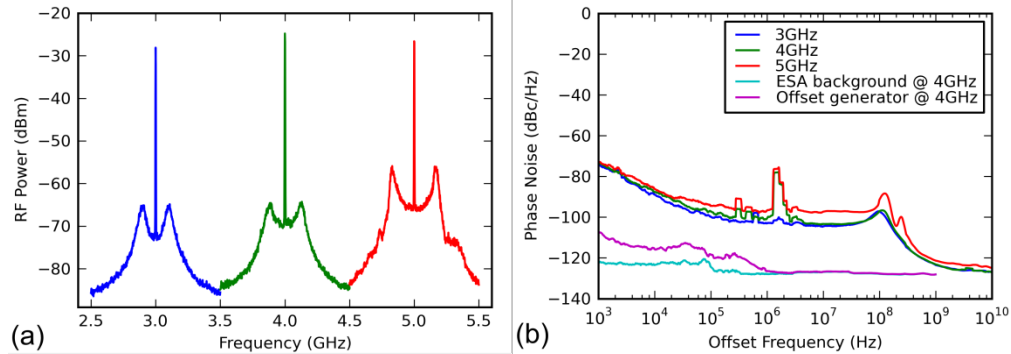

Fig. 5. (color online) (a) The heterodyne signal between the master and slave lasers for OPLL operation at 3 GHz, 4 GHz and 5 GHz offset frequencies (resolution bandwidth 1MHz). (b) Phase noise measurements of the heterodyne signal for the OPLL at offsets 3 GHz, 4 GHz and 5 GHz. Also shown are the noise floor of the spectrum analyzer and the phase noise of the offset generator.

Figure 5(a) shows typical heterodyne spectra for various offset frequencies, using the DFB laser as a master laser. For these measurements the grating sections of the slave laser were shorted in order to minimise the laser linewidth. The OPLL's low-frequency tracking circuit compensated for the DFB laser frequency drift of over 1 GHz and gave stable results, with the OPLL remaining locked for several hours.

Figure 5(b) shows single side-band phase noise spectra for the heterodyne between the DFB master and slave laser signals with the OPLL locked at various offset frequencies. They correspond to the measurements shown in Fig. 5(a) and were recorded using the dedicated phase noise measurement mode of a Rhode & Schwarz FSU26 RF spectrum analyser. Above 20 kHz offset, the phase noise is below −90 dBc/Hz. The phase error variances in bandwidth 1 kHz to 10 GHz are 0.038, 0.058 and 0.22 rad^2 for 3, 4 and 5 GHz respectively. Most of this variance comes from the peak near 100 MHz suggesting that the loop gain was higher than optimum.

5. Conclusion

We have successfully fabricated a monolithically integrated heterodyne OPLL that can be locked to an external master laser at 1553 nm, with a 0.6 GHz to 6 GHz offset between master and slave signals, set by an RF offset input. This is possible due to the very short loop delay allowed by monolithic integration, which has led to an optical delay between the laser and detector of less than 20 ps; and also due to the custom design for the phase detector and loop filter electronics which achieved a propagation delay of less than 1.8 ns.

Such a compact and low noise system is extremely attractive for both coherent optical communications and in photomixing applications for creating mm-wave and THz sources.

Acknowledgements