A Low-Power, Versatile Capacitance Interface ASIC Based on Pulse-Width Modulation with Real-Time Dynamic Range Matching

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***Abstract*—Capacitive sensing is commonly employed to measure a wide range of physical quantities, including displacement, humidity, and pressure. Readout accuracy, speed, and power consumption are among the key performance characteristics during the design process for meeting the specific demands of the sensor application. Minimum parasitic effects in capacitance-to-time converters offer high suitability in precise, high-resolution applications that demand low sensitivity to environmental effects, such as in biomedical sensing devices. However, the design trade-offs in the measurement range, resolution, and speed often limit device performance and require manual adjustment of the sensing front-end. This paper describes a low-power readout circuit for high-resolution capacitance sensing across a wide input range of up to 200 pF. A pulse-width-modulation-based, capacitance-to-time (C-T) converter is presented in 65-nm CMOS technology for miniaturised applications. Real-time monitoring of the output enables automatic adjustment of the sensing parameters that determine range, resolution, and speed, providing a flexible solution to the application needs. The system provides rapid conversion of single- and differential-mode capacitors with a 50-μs readout time while consuming 25 μW from a 1-V supply.**

***Index Terms*—capacitive sensing, low-power measurement system, pulse-width modulation (PWM), real-time monitoring, self-adjusting sensor, time-based capacitor interface**

I. Introduction

The rising demand for biosensing and internet of things (IoT) interfaces has been a driving force in advancing micro-electromechanical (MEMS) readout systems, maximising sensor accuracy, reliability, and versatility at minimum cost, area, and power consumption [1]. Capacitive sensors formed of parallel-plate or coplanar, comb-like structures have been implemented for measuring physical parameters including pressure, strain, proximity, temperature, and humidity using varying forms of rigid and flexible platforms [2], [3]. Due to the passive nature of capacitive sensors, the readout structure defines the overall power consumption of the system. Therefore, low-power implementation of the sensor interface is an important design aspect. Furthermore, the diverse requirements of capacitive sensors used for health monitoring and IoT applications demand a versatile system that can maintain a high performance in real time. Capacitance-to-voltage or current are among the most commonly implemented techniques in sensor interfaces [4], [5]. These rely on analog detection of capacitance inputs via a charge-sensitive amplifier, lock-in detector, or current conveyor [6]–[8], to be later digitised using analog-to-digital converters (ADC). Semi-digital techniques include frequency, time, and phase-based signals that can be more easily converted to the digital domain with minimal analog processing. This can save considerable area and power while achieving a low sensitivity to parasitic capacitances [9], [10]. This allows a wide input range at a low voltage with greater resilience to noise sources in the digital output signals [11], [12]. Time-based architectures typically rely on period modulation using simple relaxation oscillators [13], or pulse-width modulation (PWM) that enables faster readout [11], [14].

A reliability configurable dynamic range is a further advantage of a capacitance-to-time converter, enabling the sensing range and resolution to be fine-tuned to the device under test [15]. Fig. 1 shows a top-level block diagram of the proposed PWM-based readout circuit, where two RC modules are measured through a voltage-to-time converter (VTC) followed by a time-to-digital converter (TDC). The resulting digital signal (D_{in}) is then monitored via a digital signal processing unit (DSP) to alter the input dynamic range, if necessary. In this paper, an ultra-low-power sensing interface ASIC is presented in 65-nm CMOS technology for capacitance-to-time conversion based on a PWM readout structure. The aim of this work is to collect high-resolution and high-speed

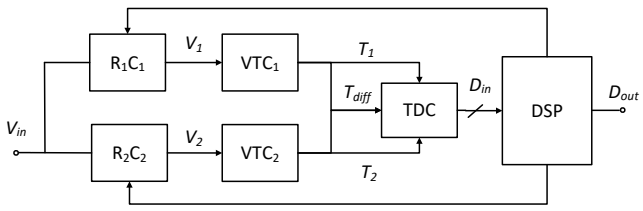

Fig. 1: Schematic block diagram of the sensor interface.

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capacitive measurements at low power and a varying sensor range, suitable for differential and single-mode readout. An overview of the circuit architecture is provided in Section II, describing the principles of the PWM-based capacitance-to-time conversion method and the digital controls implementing automatic matching of the dynamic range to the application needs. Section III reports the simulated results of the full system, followed by concluding remarks in Section IV.

II. Interface Design

A. Theory of operation

The capacitive readout module is formed of two sensing RC networks that can be measured in a stand-alone, single-ended fashion [11], or differentially by combining the VTC outputs of each branch [14]. Adjustments in each node's resistor value enables appropriate matching of the dynamic range [15], which is digitally controlled for automatic tuning. As shown in Fig. 2(a), each VTC comprises inverter-based comparators used to digitise the output voltage of each RC network ($V_{1,2}$), followed by XOR gates that determine the relevant pulse width for each capacitor ($T_{1,2}$) and their difference (T_{diff}). A high-frequency input clock (V_{clk}) used as an excitation signal propagates through each RC network and provides the inputs to the comparators. Each XOR gate is used to determine the PWM output based on the digital outputs of each comparator ($D_{1,2}$). The individual measurements of each branch help determine the baseline capacitance values and calibrate any variations caused by environmental factors that may impact the resulting differential outputs. Local digital control of the variable resistors in the RC networks and the input signal pulse width help adjust the range and precision of measurements. The sensing pulse width (T_{pw}) is linearly proportional to the RC time constant τ. According to the step response presented in (1), T_{pw} can be extracted from the capacitor charge voltage, which is limited by the comparator threshold defined at a percentage (α) of the final voltage (V_f).

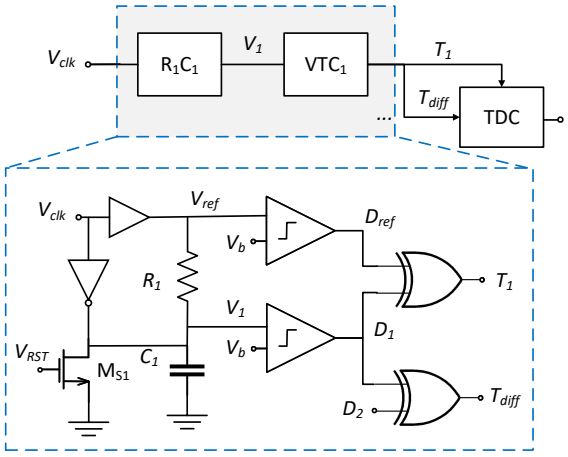
$$V_{charge} = V_f \cdot \left(1 - e^{-t/\tau}\right) \tag{1}$$

Considering the final voltage reaching the supply as $V_f = V_{DD}$, the charging voltage limited by the comparator threshold as $V_{charge} = \alpha V_{DD}$, and the timing parameters $t = T_{pw}$ and $\tau = RC$, the step response in (1) can be solved for the individual (single-mode) sensing time, $T_{pw,single}$, as directly proportional to RC [11], as outlined in (2). For differential sensing, the output PWM signal is linearly proportional to the difference in the time constant of either branch ($R_1C_1 - R_2C_2$). Assuming equal resistance values that are digitally defined ($R_1 = R_2 = R$), the differential output ($T_{pw,diff}$) presented in (3) can be obtained using the same expression and taking the capacitive difference between the two branched (ΔC) as $C_1 - C_2$ into account [14].

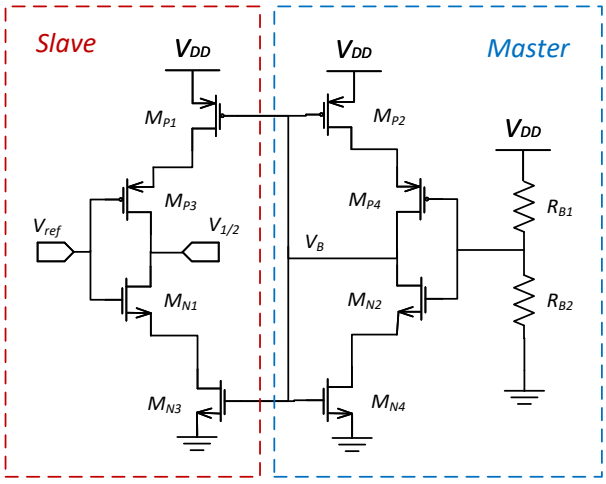
$$T_{pw,single} = RC \cdot ln\left(\frac{1}{1-\alpha}\right) \tag{2}$$

$$T_{pw,diff} = R \cdot \Delta C \cdot ln\left(\frac{1}{1-\alpha}\right) \tag{3}$$

To facilitate rapid and reliable function, each RC block is accompanied by a buffer at the resistor input and a fast reset switch (M_{S1}) across the capacitor to ensure complete discharge between clock cycles, while closely matching the inverter delay with the input excitation signal [11]. The single-RC branches are expected to provide a similar response, with the reference points V_{ref} overlapping the V_{in} signal and measured through the XOR gate with respect to $V_{1,2}$ to determine the $T_{pw,single}$ on each branch. A typical implementation of the capacitor-to-PWM converter involves self-tuning inverter-based comparators, which enable low-power operation that is insensitive to process and temperature variations at a low complexity [16]. The design shown in Fig 2(b) comprises a single master branch that determines the bias voltage for each slave branch. Since measurements are collected in single- or differential-mode settings, only the selected slave branches are active to minimise power consumption.



(a)



(b)

Fig. 2: Capacitance-to-time conversion circuit based on pulse-width modulation: (a) top-level circuit, and (b) comparator schematic.

B. Dynamic Range Control

The maximum sensing capacitance can be found by re-arranging (2) and considering the available pulse width as a product of the excitation clock period (T_{CLK}) and duty cycle (D), or the signal "on time" available for conversion. The expression outlined in (4) shows a direct relationship between C_{max} and the parameter D, which can be optimised to maximise the sensing range, while ensuring full capacitor discharge during the "off time".

$$C_{max} = \frac{T_{CLK} \,.\, D}{R \,.\, ln\left(\frac{1}{1-\alpha}\right)} \tag{4}$$

In addition to the comparator jitter, which has a small impact on the overall system noise, the minimum sensing capacitance (C_{min}) is affected by the dead zone or delay of the XOR gate performing phase detection using the expression below. The delay is expected to measure at approximately five times the output time constant, defined by the gate resistance R_{XOR} and load capacitance C_L [11], [14]. To minimise the $R_{XOR}C_L$, the XOR gate is implemented with the minimum gate dimensions.

$$C_{min} = \frac{5 \,.\, R_{XOR} \,.\, C_L}{R \,.\, ln\left(\frac{1}{1-\alpha}\right)} \tag{5}$$

Therefore, according to (4) and (5), implementing a variable resistor R in each branch enables adjustment of both the sensing range and resolution, while further control over the excitation signal frequency helps achieve the necessary balance between the readout time and the maximum range for the capacitors under test. For rapid measurements within 50 μs cycles, a 20-kHz excitation signal is required for the minimum duty of 50%. Considering a typical baseline capacitance ranging up to tens of pF in flexible structures [2] and a comparator threshold ratio (α) of 0.5, each RC network requires a resistance in the range of several MΩ. Likewise, capacitance values with a resolution in the fF range can be detected using a high-frequency counter at the TDC stage within the bounds of (5).

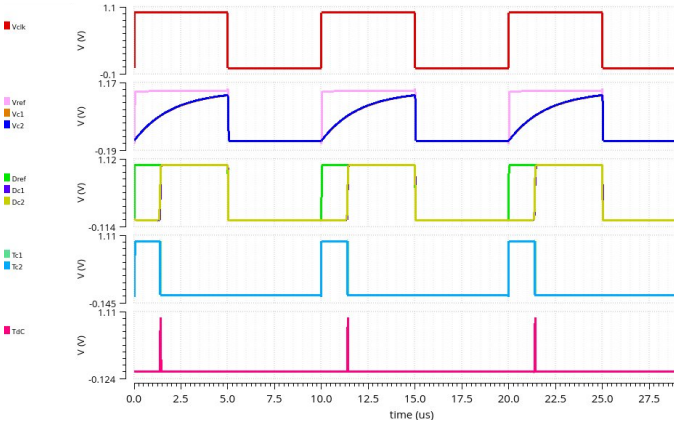
Real-time pulse width monitoring and adjustment of the input dynamic range is implemented at the DSP stage using a self-calibrating algorithm. The control module performs periodic measurements of each capacitor between differential sensing cycles to maintain an up-to-date capacitor baseline with two goals: 1) track individual capacitor variation and calibrate any offsets impacting the differential output; 2) carry out a "zoom-in" function appropriate to the detected range to maximise the sensing resolution by adjusting the reference resistors and the excitation on time ($T_{CLK}.D$). Each resistor value is determined by an independent, multi-bit control signal that changes incrementally at cycle $n+1$ according to the measurement of cycle n, as described below. Any changes in $R_{(n+1)}$ reflect the allowable range of pulse widths with respect to the input clock frequency.

$$R_{(n+1)} = \frac{T_{CLK} \,.\, D}{T_{pw(n)}} \,.\, R_{(n)} \tag{6}$$

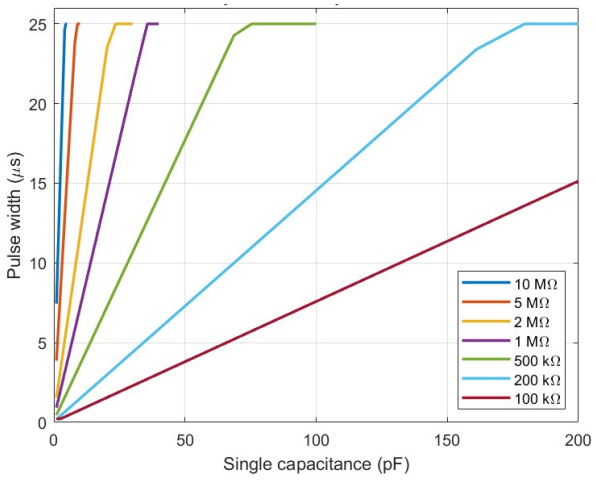
III. Results

The proposed PWM-based capacitive readout circuit is designed in a standard 65 nm CMOS technology under a 1 V supply voltage. Top-level simulations of the sensor were performed with capacitive inputs from femto- to pico-Farad range using on-chip capacitors. Fig. 3 shows transient and parametric analyses of the output pulse width for the sensing capacitors using resistor settings. The transient waveforms of Fig. 3(a) highlights the difference between the pulse width of each RC branch for a baseline capacitance of 1 pF and a differential variation of 100 fF with a 2 MΩ resistor. The parametric results shown in Fig. 3(b) demonstrate the varying readout sensitivity for capacitor values ranging up to 200 pF during single-mode measurement.

Digital analyses of the control module were performed to verify the self-calibration algorithm. As shown in Fig. 4, the output pulse width from the analog front-end is used to dictate the resulting reference resistor value for the next sensing cycle. The testbench presents the on-chip logic with varying pulse



(a)



(b)

Fig. 3: Analyses of the capacitance to PWM converter showing (a) the transient response, and (b) parametric results for varying resistor settings.

width settings that correspond to a wide range of capacitor baseline values. Table I outlines the performance summary of the system in comparison with the state-of-the-art capacitance-to-time converters.

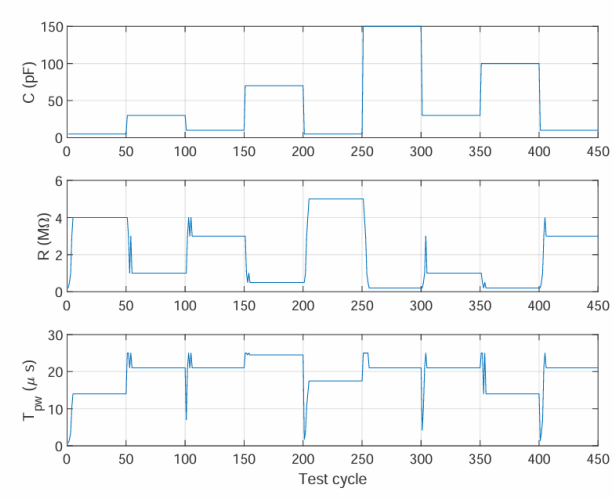


Fig. 4: Digital control of the self-calibrating RC front-end for varying sensing capacitors resulting in resistor adjustments to maintain a high pulse width.

TABLE I: Performance comparison of capacitance sensor interfaces based on pulse-width modulation.

	[11]	[12]	[14]	[17]	This work
Technology	130 nm	350 nm	180 nm	350 nm	**65 nm**
Range	10.7 nF	16 nF	22 pF	320 fF	**200 pF**
Sensitivity (ns/fF)	7	127	3.62	3.88	**5.51**
Conversion time (μs)	31	500	80	40	**50**
Supply (V)	1	3.3	1.8	3	**1**
Power (μW)	60	720	98	54	**25**
Automatic self-calibration	No	No	No	No	**Yes**

IV. Conclusion

A low-power, PWM-based interface ASIC is presented for versatile, high-resolution capacitive measurements. The circuits implemented in 65-nm CMOS technology have been analysed in detail, and their performance has been verified. A 25 μW power consumption was achieved from a 1-V supply voltage. Input capacitances ranging from 0 pF to 200 pF can be measured at the nominal frequency and can be extended beyond this range at lower frequencies. The circuit operates at 20 kHz, resulting in a conversion time of 50 μs. Local digital control enables self-calibration and adjustment of sensing parameters to maximise the input dynamic range without the need for manual intervention. The integrated circuit provides versatile control of single and differential capacitor measurements with automatic matching of dynamic range for a variety of applications in IoT, bioelectronics, and robotics, where rapid and accurate sensing is required.

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