A SoC for an active implantable microsystem for closed-loop optogenetic neuromodulation

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***Abstract*—This paper presents a system-on-chip (SoC) architecture for an active implantable microsystem that combines electrical recording with optogenetic stimulation for closed-loop neuromodulation. The SoC is designed to support a 4-shank optrode (opto-electrode) fork with 8 differential recording channels (0.1-5000 Hz bandwidth, 10 mVpp range, 12-bit resolution) to observe neural signals on electrodes and 32 driver circuits (2 mA range, 6-bit current resolution with µs timing resolution) for microLED optical stimulation. Each SoC additionally integrates diagnostic instrumentation to measure electrical resistance across any of its I/O lines. The SoC features a custom 4-wire interface that provides power and data communication across multiple chips using a shared bus allowing for multiple forks to be stacked to form two dimensional optrode arrays. Each chip has an independent controller that receives, interprets and executes commands, and can transmit neural data while simultaneously controlling LED outputs. The circuit is implemented in a 180 nm CMOS process, with each chip occupying a 5 mm×2.45 mm silicon footprint, designed specifically to mount on the base of the silicon optrode fork.**

***Index Terms*—Implantable microsystem, neural recording, optogenetic stimulation, closed-loop neuromodulation.**

I. Introduction

Neuromodulation, the ability to modify neural activity, is an established bioelectronic intervention for Parkinson's disease, essential tremor and epilepsy, providing therapeutic control over abnormal neural oscillations [1]–[3]. Optogenetics has transformed neuroscience by enabling precise control of neural activity through genetic manipulation and optical stimulation [4], [5]. By introducing light-sensitive opsins into neuron membranes, neural tissue becomes responsive to optical stimuli. This allows for the activation or suppression of specific neurons using light without generating electrical artifacts that interfere with neural recordings [6], making optogenetics particularly beneficial in closed-loop neuromodulation [7], [8]. Furthermore, as highlighted by recent efforts towards clinical translation, its precision and selectivity hold significant potential for treating neurological and psychiatric disorders [9].

Recent advancements in optoelectronic systems have shifted from using external light sources [10], [11] to on-site generation via micro-scale LEDs [12] in integrated neural implants, addressing challenges posed by tissue light scattering [13], [14]. To achieve on- or near-probe light generation, three general approaches exist: (1) integrating LEDs within a custom semiconductor substrate to circumvent silicon's indirect bandgap limitations [15]; (2) directly mounting microLEDs onto CMOS integrated circuits [16]; and (3) engineering waveguides into the chip to modulate and switch light supplied by an off-chip source typically situated at the end of the probe [17]. In this work, we follow the second approach [18], providing the flexibility to combine highly efficient microLEDs implemented in optimal technology with highly integrated microelectronics using CMOS technology.

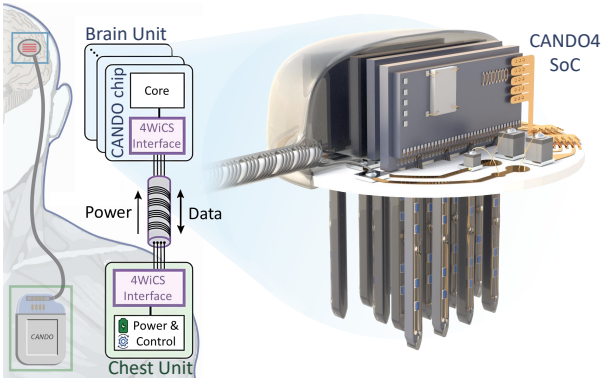

Fig. 1. CANDO implantable system concept showing the brain and chest units connected via a subcutaneous lead.

Several system integrations for optogenetic neuromodulation have been proposed [19]–[23], with some addressing multichannel recording and stimulation [19]–[21]. However, they typically rely on off-the-shelf components [20], [23], require tethering [22], or use headstages [19]. To overcome the limited robustness and stability, a fully implantable system offering complete integration and long-term durability is needed for clinical applications. This work presents a system-on-chip (SoC) integration for a neural interface which is part of the CANDO (Controlling Abnormal Network Dynamics with Optogenetics) project, aiming to develop a novel intervention for drug-resistant focal epilepsy.

II. System Overview

The implantable device concept is shown in Fig.1. Building on previous work in [16], [24]–[26], which has been validated through in vitro and in vivo studies, this paper presents the 4th generation (CANDO4) SoC in the brain unit of the implantable system. This latest iteration enhances the performance and functionality reported in earlier designs [16]. It allows the observation of local field potentials (LFPs) and extracellular action potentials (EAPs) via microelectrodes and the application of optical stimulation via microLEDs. It connects to a chest unit via a subcutaneous lead [27] using a custom 4-Wire Communication System (4WiCS) for power and full-

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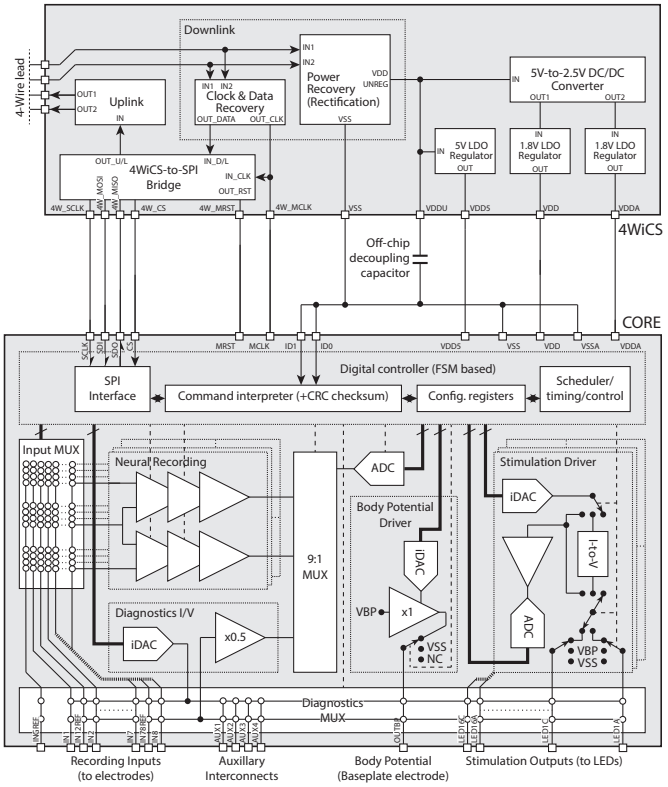

Fig. 2. Top-level system architecture of the CANDO4 SoC.

duplex data communication [28], [29]. The chest unit contains the power source (rechargeable battery), system controller, processor, power management, and data telemetry [29], [30].

The brain unit features a 4×4 array of 5 mm optrode shanks, each with a cross-section of $300\,\mu m^2$, containing 8 microLEDs and 3 electrode sites distributed along the shank length. This unit is assembled from four subsystems, each consisting of an optrode fork with four optrodes and a CANDO4 SoC. The four CANDO4 SoCs connect in parallel via the custom 4-wire interface, which also links to the chest unit. The CANDO4 SoC (outlined in Fig. 2) is arranged in two subsystems: the 4WiCS and the core neural interface. This modular organisation provides versatility for use under two configurations: as a research tool, where the core system functions as a peripheral device connected to a microcontroller via SPI and powered by a DC supply, or as a medical device, where bondwire links connect the core system with the 4WiCS for integration within the multi-fork optrode array. The complete system contains eight key blocks: data uplink, data and power downlink, power management, digital controller, neural recording, optical stimulation, diagnostics, and body potential driver.

The 4WiCS interface enables power transmission and bidirectional data communication across a shared AC-coupled wireline, supporting up to four addressable devices. It translates bidirectional data to a standard SPI bus, which interfaces with the digital controller. The controller implements error checking/correction, co-ordinates the various peripheral functions, and manages internal timers that allow to group stimulation channels together and assign groups to the timers. The neural recording block includes eight differential low-noise amplifier cascades and an ADC. The optical stimulation block contains 32 current-controlled driver circuits with balanced voltage bias for enhanced encapsulation durability [31], [32]. Additional subsystems include a diagnostics interface for source-measure testing across the multi-shank fork connections and a body potential driver to maintain a constant bias between the neural tissue and the internal power supply.

III. System Implementation

A. 4-Wire Communication System (4WiCS)

Building on our previous work, validated in [28]–[30], the 4WiCS subsystem in the CANDO4 SoC enables simultaneous power transfer and bidirectional data communication between the external controller (chest unit) and internal peripheral devices (brain unit) via a single 4-wire lead [28] (Fig. 3). A key feature is the use of AC signalling with DC-blocking capacitors, ensuring safety in the event of damaged leads and improving long-term encapsulation reliability by maintaining zero net DC voltage during normal operation. Two wires handle power and downlink data, while the other two manage uplink communication. The system's full-duplex capability allows real-time closed-loop neuromodulation. Noise immunity is achieved through differential signalling, reducing common-mode noise interference essential for stable implant operations.

The Power Management Unit (PMU) converts AC signals received into stable 5 V and 1.8 V supplies. A full-wave active rectifier maximises the power conversion efficiency (PCE) by reducing the voltage drop, while a switched-capacitor DC/DC converter reduces the ripple to under 5%, supporting a power transfer efficiency of up to 85% at 1 mA. The Data Communication Unit (DCU) supports data and 200 kHz clock recovery in the downlink path. This is used to generate a stable 3.2 MHz system clock via a phase-locked loop (PLL), providing precise timing and synchronization for implant operations. Uplink data employs Manchester encoding, achieving a bit-error rate (BER) below 10^{-6} even in noisy environments.

Full-duplex communication enables real-time monitoring and adjustment of stimulation parameters for effective closed-loop neuromodulation. The core digital controller, part of the 4WiCS interface, manages all SPI communication and system operations, including command execution, configuration, and subsystem monitoring. Implemented using RTL and a standard-cell design flow, it translates SPI data into control signals for stimulation, recording, and diagnostics. A 32-bit word format with 24 data bits and an 8-bit CRC ensures data integrity before command execution.

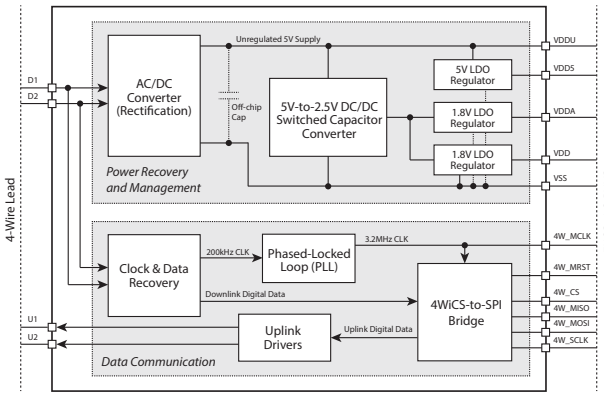

Fig. 3. Top-level architecture of the CANDO4 4WiCS interface.

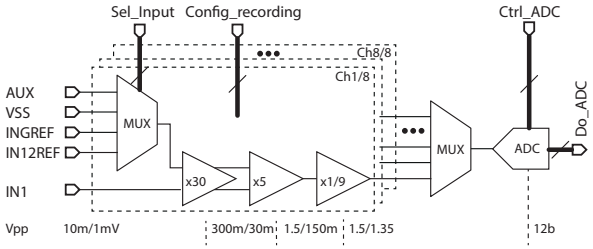

Fig. 4. Architecture of the neural recording subsystem with 8 differential low-noise amplification channels, input and output MUXs and a shared ADC. Gain and filter configuration, as well as ADC timing, is provided by the controller.

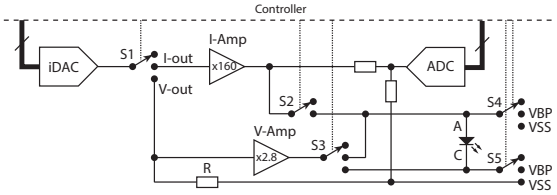

Fig. 5. Simulation driver circuit for different stimulation profiles.

B. Neural Recording

To effectively observe neural network dynamics for closed-loop neuromodulation, the neural recording circuit is designed to acquire both LFPs (<100 Hz) and EAPs (∼200 Hz-5 kHz). The analogue front-end (AFE) is shown in Fig. 4, consisting of 8 differential channels (two per optrode), providing a total of 32 channels across the brain unit. The reference inputs are multiplexed to provide a configurable scheme with local (per shank), global (per chip), and single-ended (VSS) referenced recordings [33]. The AFE implementation is based on our previous designs [34] with parameters adjusted to the CANDO application and specific CMOS technology. It features a programmable overall gain between 44 dB and 63 dB, 0.1-200 Hz high-pass filter corner and 400 Hz-7 kHz low-pass corner. A 9:1 multiplexer is used to interface the 8 channels and impedance/diagnostic measurement (Fig. 2) to a shared 12-bit SAR ADC with a sampling rate of 100 kHz.

C. Stimulation Driver

The stimulation driver circuit (Fig. 5) delivers programmable current pulses to modulate the illumination of 32 individual LEDs (CREE TR2227, 470 nm), arranged as 8 LEDs per shank across four shanks. Each driver provides a precise, configurable current stimulus up to 2.016 mA with 32 µA resolution and operates in both monophasic and biphasic stimulation modes. A biphasic mode is included based on our previous work [35] to ensure balanced, symmetric stimulation, minimising electric field-induced encapsulation degradation [31]. The asymmetric biphasic scheme, validated for its effectiveness in maintaining long-term device viability [36], provides voltage compensation around the body potential during both stimulation and compensation phases.

The stimulation driver architecture consists of a current DAC (iDAC), ADC, current and voltage amplifiers, and multiple analogue multiplexers (MUXs). The iDAC, operating in the 1.8 V domain, generates the reference current during the stimulation phase, which is then amplified by a factor of 160× and directed through the anode of the selected LED. Voltage compliance is maintained within a 4.5 V range to ensure reliable operation. In the compensation phase, the polarity of the stimulation profile is reversed, and the output is sampled by the ADC to achieve symmetric compensation through a proportional current.

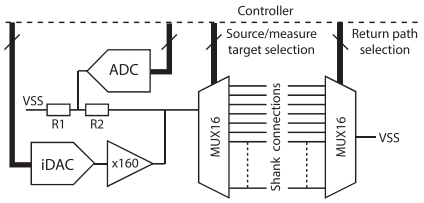

Fig. 6. Architecture of the diagnostics subsystem including current source generation, voltage measurement, and current return path routing.

D. Diagnostics Instrumentation

A diagnostic instrumentation circuit was designed to provide comprehensive testing capabilities, and following LED-optrode thermal and optical modelling [37]. Shown in Fig. 6, it is capable of sourcing test currents and measuring voltage across any two of the 50 system connections. Each shank has 12 connections—8 for LEDs, 3 for recording electrodes, and 1 auxiliary—plus a body potential electrode and a global reference. It can test LED I-V characteristics, including temperature sensing via reverse biasing as demonstrated in [38], [39], verify the mechanical integrity of silicon shanks [40], [41], and detect leakage currents through encapsulation.

The test current is generated with the same 6-bit programmable iDAC and current amplifier used in the stimulation driver circuit. For voltage measurement, the observed potential is scaled down from the 5 V to the 1.8 V domain to match the input range of the recording ADC. This scaled voltage is then digitised via the recording MUX as shown in Fig. 4. The diagnostics current amplitude and 4-bit programmable pulse duration (32-504 ms) are configured within the controller.

E. Body Potential Driver

The body potential driver (BPD) [33] connects to a ring-shaped electrode on the underside of the brain unit, contacting the brain surface, to maintain a constant bias between the body and the system's power supply. This setup establishes a local ground, minimising common-mode noise and interference. To prevent DC current flowing into the body, current monitoring and overcurrent protection circuits are implemented, complying with the BS EN 45502-1:2015 standard [42].

IV. System Integration & Packaging

The proposed CANDO4 SoC has been implemented in a 180 nm CMOS technology with dimensions of 5 mm×2.45 mm. The annotated layout is shown in Fig. 7.

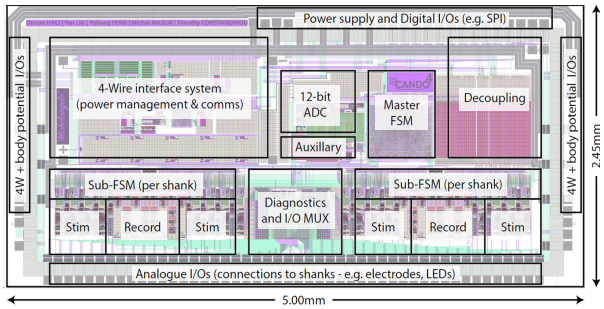

Fig. 7. Annotated layout of the complete CANDO4 SoC.

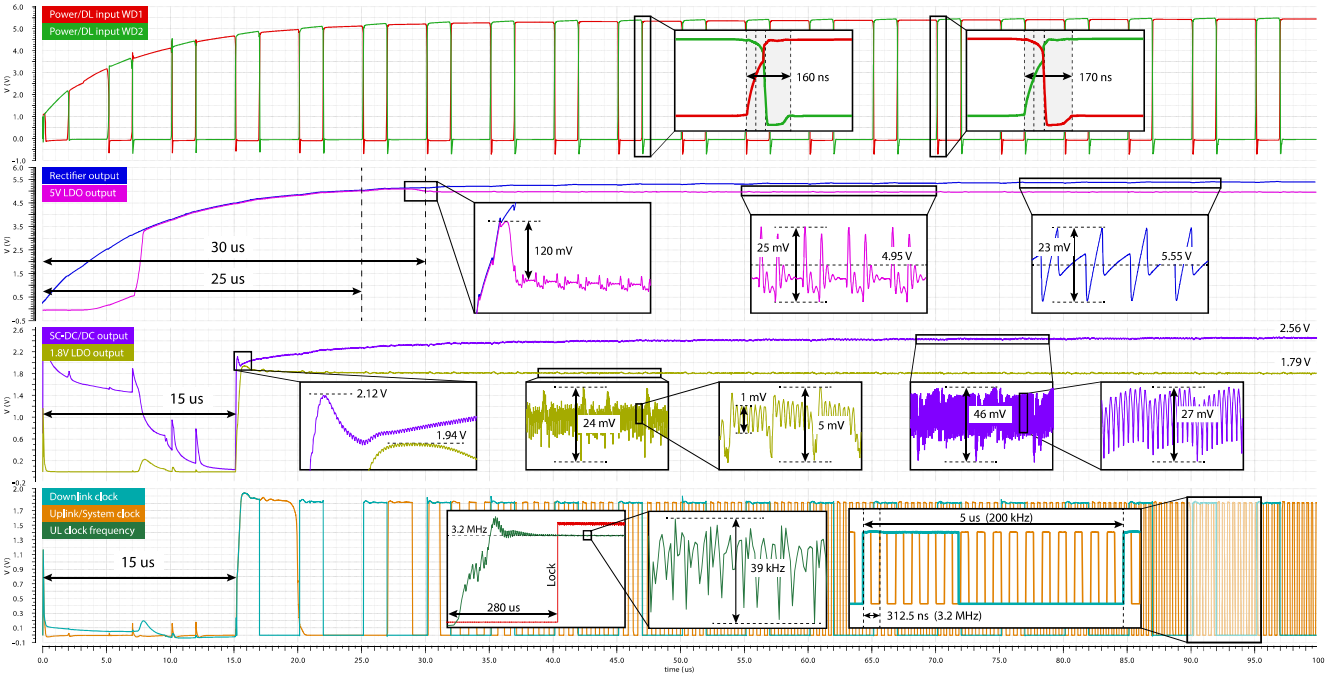

Fig. 8. Post-layout transient simulation results of the 4WiCS interface.

The four optrode forks are integrated into the device on a ceramic baseplate. The baseplate consists of alumina with metal tracks of Au paste, solder pads of Pt/Au and dielectric glass layers, screen-printed using standard thick-film techniques. Post-printing, the plate is micromachined into a baseplate with a Nd:Yag laser into a circle with four slots for each optrode fork. The fork-baseplate interconnection is achieved with a custom ribbon cable made of Au between polyimide. On both the optrode side and the baseplate side, thermosonic gold bumping is used as interconnection [43]. The 4-wire helical cable [27] along with the off-chip DC-blocking capacitors are soldered to the baseplate. The whole structure would then be washed [36], air plasma activated, and encapsulated in silicone rubber (NuSil MED-6015). This allows to protect the implant from corrosion due to body fluids and electric fields induced by the biphasic stimulation, as demonstrated in accelerated in vitro and in vivo studies in [32].

V. Simulation Results

The neural recording circuit achieves an input range of up to 10 mV_{pp}, an input-referred noise (IRN) of 5 μV_{rms} in the LFP and EAP bands, with a power consumption of approximately 32 µW per channel. The AC-coupled amplifier topology enables a high input impedance of 50 MΩ at 1 kHz, minimising signal attenuation when interfacing with intracortical electrodes [44].

Fig. 8 shows the key signals of the novel 4WiCS interface during transient simulation. Power signals of 6 V_{pp} are transmitted through the chest unit and received at the WD1/WD2 inputs, with transition times averaging 165 ±5 ns. Due to loading effects from the cable and capacitors, the signals ramp up to their peak voltage. The rectifier reaches 5 V after 25 µs, stabilising at 5.55 V with a 23 mV ripple. The 5 V LDO begins regulating at 30 µs, outputting 4.95 V with a 25 mV ripple, caused by interference of the downlink signal. The switched-capacitor DC/DC converter activates at 15 µs, with a ripple of 46 mV, mainly due to the 60 MHz interleaving switching, resulting in a 27 mV ripple. The 1.8 V LDOs activates at 1.9 V, providing an output of 1.79 V with a 24 mV ripple due to noise from the downlink and DC/DC converter. Finally, the clock signal is recovered, and the PLL locks after 280 µs, enabling uplink communication for recorded and diagnostic data.

TABLE I
Comparison of Optogenetic Neural Interface Systems

Parameter	[45]	[22]	[19]	This work
Technology [µm]	0.35	0.18	0.13	**0.18**
No. of Ch. (Rec./Stim.)	4/6	1/1	10/4	**8/32**
Neural signal	LFP	EAP	LFP, EAP	**LFP, EAP**
Total area [mm²]	1.96	4.64	1.2	**12.25**
IRN [μV_{rms}]	N/A	4.57	3.2	**5**
Noise bandwidth [Hz]	N/A	300-5k	10-7k	**0.1-3k**
ADC resolution	10-bit	N/A	9.75 ENOB	**12-bit**
Additional features	Diagnostics, controller	In-vivo tests	In-vivo tests	**Diagnostics, controller, BPD**

Simulation results of additional subcircuits and overall system specifications are illustrated in Table I along with a comparison to other existing optogenetic systems.

VI. Conclusion

The CANDO4 SoC introduces significant advancements in precise closed-loop optogenetic neuromodulation as part of a complete implant system. It includes an AC-coupled wireline interface for safe operation, combining power transmission with full-duplex communication. The optical stimulation driver implements a novel asymmetric biphasic waveform that reduces degradation of encapsulation, enhancing device longevity, while its neural recording front-end captures both LFPs and EAPs with configurable gain and flexible referencing. Additionally, the integrated diagnostics ensures real-time testability and device integrity. Future work will focus on silicon verification of the fabricated circuit and microsystem integration of the CANDO4 SoC to realise the brain unit.

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