Design and Optimization of a High Linearity On-Chip Sinusoidal Current Generator for Bioimpedance Measurements Using Direct Digital Synthesis

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***Abstract*—This paper presents an optimization methodology to enhance the linearity of direct digital synthesis (DDS)-based on-chip sinusoidal current generators (SCGs) for bioimpedance measurements. After a detailed analysis of the origin of harmonics and their impact on measurement accuracy in conventional DDS-based SCGs, three different harmonic cancellation schemes are proposed. These are designed to decrease the harmonics in various applications with differing hardware requirements, significantly improving the precision and efficiency of DDS-based SCGs. The approach was implemented in DDS-based SCG in 65 nm CMOS technology. Both simulations and measurements demonstrate a marked improvement in linearity with a figure-of-merit at least 9.4 times better than prior work. Although tailored for bioimpedance applications, the approach is also suitable for other low power, high linearity sinusoidal signal generators.**

***Index Terms*—Bioimpedance, direct digital synthesis, sinusoidal current generator harmonic cancellation, total harmonic distortion.**

I. INTRODUCTION

BIOIMPEDANCE analysis is a method of measuring the electrical properties of biological tissues in the human body. It has been widely used in different applications including body composition analysis, cardiovascular health and respiratory function assessment [1]-[3]. Bioimpedance measurements are usually performed by injecting a known ac current and measuring the induced voltage, whose magnitude and phase are used to calculate the tissue impedance.

State-of-the-art bioimpedance measurement systems are typically characterized by their precision and low power consumption. Enhanced precision improves the system's capability to accurately capture vital bio-information, crucial for reliable health monitoring. In addition, energy efficiency ensures extended system operation, a critical factor for wearable or implantable devices designed for continuous health monitoring. Fig. 1 shows the block diagram of a typical bioimpedance measurement system, comprising three primary components: (i) a sinusoidal current generator (SCG) composed of a sine wave generator (SG) and a current driver (CD), the latter converts the sinusoidal voltage into a current and injects it into the target tissue (represented by load Z_L in Fig. 1), (ii) a recording amplifier for capturing the induced voltage, and (iii) an in-phase and quadrature (I-Q) demodulator to determine the real and imaginary parts of Z_L. In I-Q demodulation, the most common method of bioimpedance measurements, the recorded voltage is multiplied with in-phase and quadrature reference signals, followed by dc conversion using low-pass filters (LPFs) [3]-[7]. The accuracy of I-Q demodulation is strongly affected by the spectral purity of the excitation and reference sinusoidal signals, as discussed in Section II. The SCG is the most power-consuming component of a bioimpedance measurement system when achieving high spectral purity, and accounts for over 80% of the overall power consumption [6], [8]-[9]. This highlights the critical need for a SCG that not only exhibits high power efficiency but also maintains high linearity.

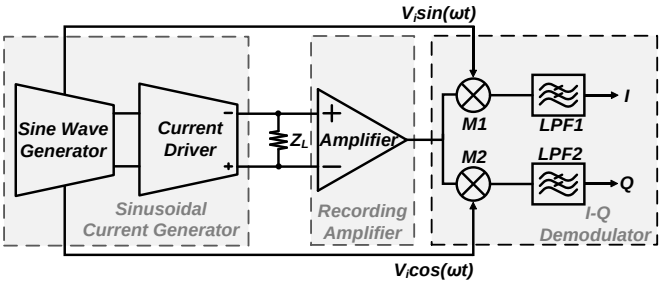

Fig. 1. Block diagram of a common bioimpedance system.

Various on-chip SCG architectures have been proposed. The majority adopt a configuration comprising a SG to provide a sinusoidal voltage and a CD to convert this voltage into current. As shown in Figs 2(a) and 2(b), SGC topologies can be broadly categorized based on their sinusoidal voltage generation approaches into: (i) closed-loop oscillator-based SCGs, and (ii) direct digital synthesis (DDS) based SCGs. Closed-loop oscillator-based SCGs typically feature a non-linear feedback mechanism paired with a loop filter, facilitating the generation of highly linear sinusoidal voltages with total harmonic

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distortion (THD) below 0.1% [10]-[12]. However, this approach tends to be power-intensive, with consumption ranging from hundreds of microwatts to milliwatts, and the frequency and magnitude of the output sinusoidal voltages are sensitive to process variations. Hence, DDS-based SCGs are often favored in contemporary bioimpedance measurement systems due to their low power consumption, usually below 100 μW, and precision in frequency and magnitude [13]-16].

The architecture of DDS-based SCGs, as shown in Fig. 2(a), usually comprises a lookup table (LUT) that stores pseudo-sinusoidal wave patterns, a digital-to-analog converter (DAC) that transforms these digital patterns into an analog signal, and a LPF that eliminates high order harmonics from the pseudo-sinusoidal wave. During operation, an oversampling clock (OSC) triggers the LUT to cycle through the prestored pseudo-sinusoidal sequence, directing the DAC to produce the desired sinusoidal signal. The frequency of the resultant sinusoidal voltage is determined by the OSC frequency and the oversampling rate (OSR), where the OSR denotes the patterns within the LUT corresponding to a single sinusoidal wave period.

To enhance the linearity of DDS-based SCGs, several approaches are typically considered: (i) increasing the OSR, (ii) increasing the resolution of digitization and DAC quantization, and (iii) increasing the order of the LPF. However, increasing these parameters invariably leads to increased power consumption and expanded chip area. In addition, the errors introduced by low order harmonics due to limited digitization and quantization resolution in bioimpedance measurements are much more significant than those introduced by high order harmonics. In-band low order harmonics are not removed by the LPF due to their proximity to the fundamental frequency.

To address these challenges, an optimization methodology with three different harmonic cancellation schemes is proposed in this paper to improve the intrinsic linearity within the LUT dataset. Measurements show that the proposed LUT dataset generated by harmonic cancellation effectively suppresses low order harmonics within the quantized waveform in the conventional approach, reducing the requirement for high OSR, DAC resolution, and LPF order. Detailed circuit level analysis of the tradeoff between the power consumption and linearity of the DAC, LPF and CD is also provided to further increase performance. A prototype SCG was designed and fabricated in a 65 nm CMOS technology to validate the efficacy of the proposed harmonic cancellation schemes. The rest of this paper is organized as follows. Section II analyses the impact of low order and high order harmonics on measurement accuracy and presents the principle of the proposed harmonic cancellation optimization method with simulated verifications in MATLAB. Section III provides the detailed hardware implementation of the SCG. Section IV presents measured results. Section V concludes the paper.

II. Optimization with Harmonic Cancellation

A. Impact of Harmonics on Measurement Accuracy

In I-Q demodulation, the recorded signal is multiplied with an in-phase (I_m) and a quadrature (Q_m) reference. Conventional demodulator circuitry implements multiplication with sinusoidal references in the digital [6], [9] or analog [12] domains. The latest integrated I-Q demodulation circuitry often employs square wave-based instead of sinusoidal-based references to lower power consumption [13], [15]. The square wave-based references I_m and Q_m can be written as:

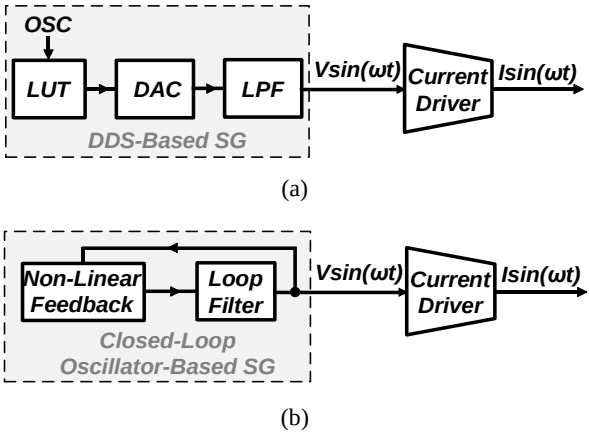


Fig. 2. Block diagram of (a) DDS-based SCG and (b) closed-loop oscillator-based SCG.

$$I_m = \frac{4}{\pi}\sum_{n=1,3,5,\dots}^{\infty}\frac{1}{n}\sin(n\omega t) \quad (1)$$

$$Q_m = \frac{4}{\pi}\sum_{n=1,3,5,\dots}^{\infty}\frac{1}{n}\sin(n\omega t + \frac{\pi}{4}) \quad (2)$$

where ω is the angular frequency of the signal. Assuming the recorded voltage V_m is:

$$V_m = \sum_{n=1,2,3,\dots}^{\infty} a_n \sin(n\omega t - \theta) \quad (3)$$

where a_n is the magnitude of the fundamental and harmonic components, and θ is the phase shift. The outputs of I-Q demodulation, I and Q, as a result of multiplying V_m with I_m and Q_m, and after removing the high frequency components, are:

$$I = \sum_{n=1,3,5,\dots}^{\infty}\frac{a_n}{n}cos(\theta) \quad (4)$$

$$Q = \sum_{n=1,3,5,\dots}^{\infty}\frac{a_n}{n}sin(\theta) \quad (5)$$

In (4) and (5), the desired demodulation outputs are obtained only when $n = 1$, and the rest is error due to the harmonics in V_m. These equations show that low order harmonics have higher contributions to the total error. In addition, these low order harmonics are less effectively removed by the LPF due to their proximity to the fundamental frequency, which further

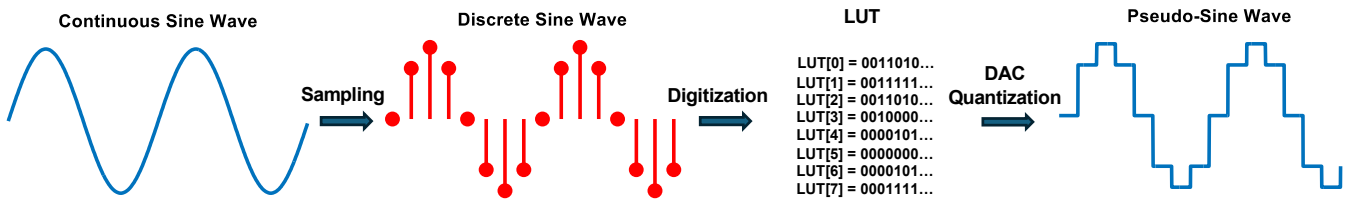


Fig. 3. Signal transfer process from an ideal sine wave to pseudo-sine wave in conventional DDS based SCG.

decreases the measurement accuracy.

B. Impact of Limited DAC Resolution and Conventional Method

In a conventional DDS-based SGC, the digital pattern controlling the DAC is created by sampling a discrete sequence from an ideal continuous sine wave. Each sample is then digitized and stored in a LUT. The DAC subsequently quantizes the digitized values in the LUT to produce a pseudo-sine wave. This signal transfer process is illustrated in Fig. 3. During digitization and quantization, the lowest value in the discrete sine wave is converted to 0 in binary code, and the highest value is converted to the DAC's maximum value.

Theoretically, for an infinite digitization and quantization resolution, with a given OSR, the harmonic components with orders lower than $\mathrm{OSR}-2$ can be completely eliminated in the generated pseudo-sine wave. However, in a practical realization, quantization noise will be introduced as most of the values of the points in the discrete sine wave are irrational values and cannot be precisely represented by a finite DAC resolution. Consequently, harmonic components with orders lower than $\mathrm{OSR}-2$ will inevitably be introduced into the generated pseudo-sine wave. To reduce quantization noise, many designs used thermal-coding DACs with resolution higher than 10-bit [17]-[18]. The high-resolution DAC effectively reduces the quantization noise, while the thermal-coding method reduces the glitches during switching and meets the matching requirement of high-resolution DACs. Although such an approach can achieve an overall THD lower than 0.5 %, it significantly increases the design complexity and chip area due to the increased size of the DAC, LUT, switches, and the routing between the LUT and DAC.

To mitigate this issue, different approaches have been suggested. One approach is to implement noise shaping together with a LUT to reduce the required DAC resolution [19]. However, it inevitably increases the noise floor, logic latency and power consumption. In addition, the low order harmonics are still limited by the intrinsic quantization noise within the LUT dataset. In another approach, a sinusoidally tapped resistive DAC is used in [20], [21]. In this approach, a sequence of resistors is dedicatedly sized for different resistance values representing each pseudo-sine step. Although it can reduce the total number of cells required to synthesize the pseudo-sine wave, it suffers from mismatch among the resistors, high quiescent power consumption and speed limitation due to charging and discharging of the capacitance at the output node. For unified DAC cell values, the optimization technique in [22] exhausts all different maximum DAC values

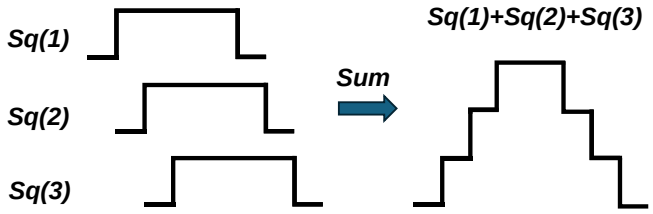


Fig. 4. Working principle of harmonic cancellation.

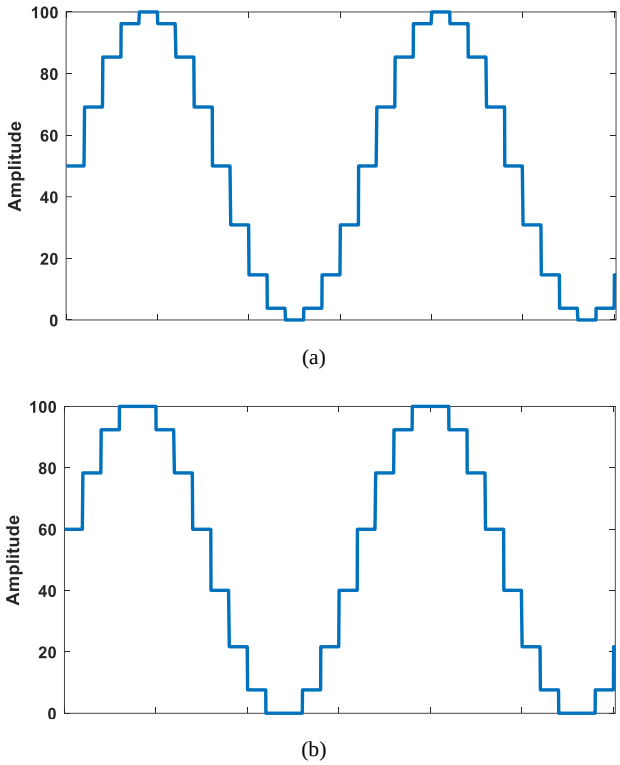
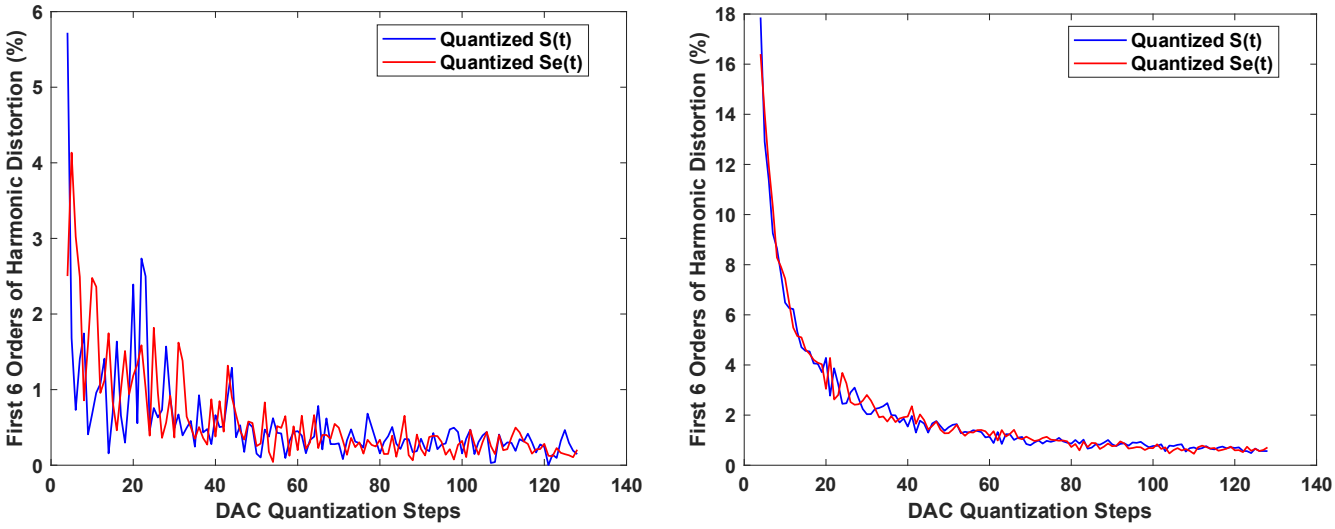


Fig. 5. Generated waveforms from (a) $Se(t)$ and (b) $S(t)$ at OSR of 16.

to represent the full scale of the pseudo-sine wave under a given DAC resolution and finds the optimized values resulting in the lowest THD. However, it requires a relatively high DAC resolution to reduce the quantization error when representing irrational values.

C. Proposed Optimization With Harmonic Cancellation

For both methods above, the principal aim is to reduce the quantization noise due to irrational values during the transfer from discrete sine wave to pseudo-sine wave. Consequently, the performance is limited by the irrational values in the discrete sine wave. Hence, it is highly desirable to find a waveform other



(a) (b)

Fig. 6 Harmonics of $S(t)$ and $Se(t)$ with OSR $= 64$: (a) first 6 orders and (b) first OSR $-$ 2 orders.

TABLE I
DETAILED COMPARISON OF THE HARMONIC DISTORTION WITH OPTIMIZED DAC STEPS

OSR $= 64$ and first 6 orders of harmonics						
DAC Resolution (bit)	4	5	6	7	8	9
Optimized DAC Step of $S(t)$	14	14	57	121	121	121
Harmonic Distortion of $S(t)$	0.157%	0.157%	0.095%	0.002%	0.002%	0.002%
Optimized DAC Step of $Se(t)$	15	30	54	54	54	328
Harmonic Distortion of $Se(t)$	0.841%	0.362%	0.043%	0.043%	0.043%	0.008%
OSR $= 64$ and first OSR $-$ 2 orders of harmonics						
DAC Resolution (bit)	4	5	6	7	8	9
Optimized Steps of $S(t)$	15	30	63	124	214	420
Harmonic Distortion of $S(t)$	4.562%	2.036%	0.850%	0.485%	0.202%	0.107%
Optimized Steps of $Se(t)$	15	27	62	110	239	477
Harmonic Distortion of $Se(t)$	4.620%	2.414%	0.987%	0.457%	0.243%	0.110%

TABLE II
DETAILED COMPARISON OF THE MEASUREMENT ERROR WITH OPTIMIZED DAC STEPS

OSR $= 64$ and without filter						
DAC Resolution (bit)	4	5	6	7	8	9
Optimized DAC Step of $S(t)$	14	30	63	108	214	441
Measurement Error of $S(t)$	1.006%	0.633%	0.298%	0.168%	0.105%	0.075%
Optimized DAC Step of $Se(t)$	15	27	54	110	234	496
Measurement Error of $Se(t)$	1.297%	0.737%	0.270%	0.185%	0.116%	0.078%
OSR $= 64$ and with filter						
DAC Resolution (bit)	4	5	6	7	8	9
Optimized DAC Step of $S(t)$	14	30	51	108	248	457
Measurement Error of $S(t)$	0.030%	0.030%	0.016%	0.006%	0.0026%	0.0015%
Optimized DAC Step of $Se(t)$	15	27	54	54	234	472
Measurement Error of $Se(t)$	0.116%	0.053%	0.007%	0.007%	0.0033%	0.0017%

than the ideal discrete sine wave which can eliminate harmonic components below a certain order while requiring fewer irrational values. To address this, an optimization method based on harmonic cancellation is proposed in this section.

Harmonic cancellation is a method that sums a group of square waves with the same frequency but with different magnitudes and carefully designed phase shifts so that their harmonics cancel each other [23], as shown in Fig. 4. As the conventional pseudo sinewave can cancel harmonics with orders lower than OSR $-$ 2, it can be considered as a sum of different square waves, where all harmonic components below OSR $-$ 2 have been cancelled by each other. For conventional pseudo-sine waves generated from a sampled discrete sine wave, although most of the sampled points vary with different OSR, the points with phases 0, $\pi/2$, π and $3\pi/2$ are always sampled regardless of different OSR [18]-[22]. As a result, it must consist of even numbers of square waves, and the generated waveform, $Se(t)$, is a sum of an even number of different square waves which can be expressed as the sum of different square waves:

$$Se(t) = \sum_{i=1}^{p} s_i[Sq(t + t_i) + Sq(t - t_i)]$$

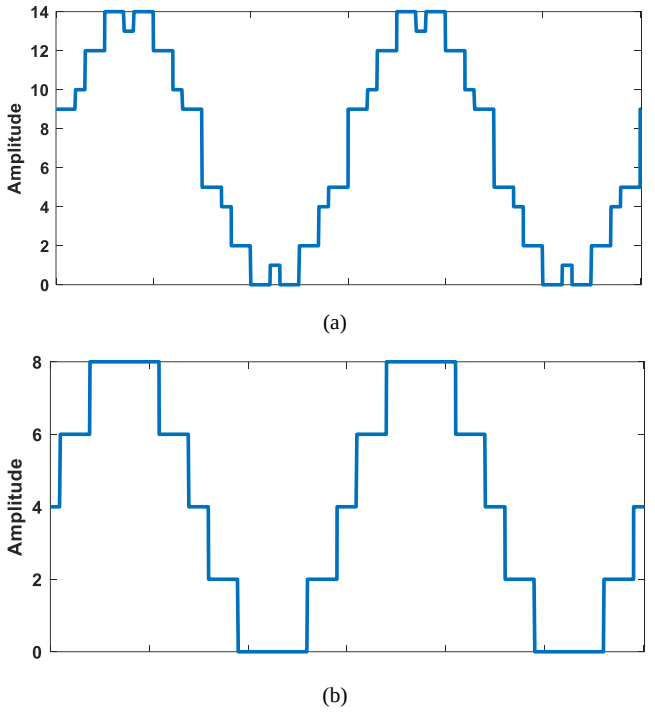


Fig. 7. Generated waveforms from (a) $y(t)$ at ORS = 30 and DAC quantization step of 14 and (b) $ye(t)$ at ORS = 30 and DAC quantization step of 8.

$$= \frac{4}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}[2\sum_{i=1}^{p} s_i \cos(n\theta_i)]\sin(n\omega t) \quad (6)$$

where Sq represents the function of a square wave, t_i is the time shift of each pair of square waves, ω is the angular frequency, θ_i and s_i are respectively the corresponding phase shift and magnitude of each pair of square waves, and p is the total pairs of square waves. For a given OSR, to cancel all the harmonic components below $\mathrm{OSR}-2$, the solutions to (6) are:

$$\begin{cases} \theta_i = i\frac{2\pi}{\mathrm{OSR}} - \frac{2\pi}{2\cdot\mathrm{OSR}} \\ s_i = \cos\left(i\frac{2\pi}{\mathrm{OSR}} - \frac{2\pi}{2\cdot\mathrm{OSR}}\right) \\ p = \frac{\mathrm{OSR}}{4} \end{cases} \quad (7)$$

By utilizing (6) and (7), the ideal pseudo-sine wave is now represented by the sum of different groups of square waves, whose harmonic components below $\mathrm{OSR}-2$, or $2(2p-1)$ can be cancelled with a total p group of square waves at OSR of $4p$.

According to (7), most of the magnitudes of the square waves, s_i, are irrational values. They are hard to fit into a DAC with limited resolution, causing quantization errors. To reduce the quantization errors without increasing the DAC resolution, one approach is to reduce the total number of square waves required for cancelling a given number of harmonic components, and thus reduce the number of irrational values. Both the difficulties of fitting DACs with finite resolution to irrational values and the quantization noise will decrease.

For the waveform $Se(t)$, the total number of steps within one signal period equals the OSR. Consider another waveform $S(t)$ with the same OSR as $Se(t)$ that can cancel all harmonic components lower than $\mathrm{OSR}-2$ but requires fewer square waves and thus, fewer step changes in one signal period compared with $Se(t)$. This indicates that at least a pair of adjacent sample points in $S(t)$ must have the same value to reduce the total number of steps. This is only possible when the two adjacent sample points are located symmetrically on each side of the peak point. With this arrangement, the number of steps within one signal period will change to $\mathrm{OSR}-2$ and a total of $2p-1$ square waves are required by this waveform. As the total square waves required is an odd number, this waveform $S(t)$ is given by:

$$S(t) = Sq(t) + \sum_{i=1}^{p} s_i[Sq(t+t_i) + Sq(t-t_i)]$$

$$= \frac{4}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}[1 + 2\sum_{i=1}^{p} s_i \cos(n\theta_i)]\sin(n\omega t) \quad (8)$$

where the variables have the same definition in (6). For a given OSR, the solutions for each variable are given by:

$$\begin{cases} \theta_i = i\frac{2\pi}{OSR} \\ s_i = \cos\left(i\frac{2\pi}{OSR}\right) \\ p = \frac{OSR-1}{4} \end{cases} \quad (9)$$

An example of the waveforms generated from $S(t)$ and $Se(t)$ at an OSR of 16 is shown in Fig. 5. Similarly to $Se(t)$, $S(t)$ can cancel the harmonic orders below $\mathrm{OSR}-2$. Since the adjacent points around the upper and lower peak point value share the same value, $S(t)$ has fewer step changes compared with $Se(t)$. This indicates that $S(t)$ can be more easily fitted to a DAC with limited resolution compared with $Se(t)$ due to the reduced number of irrational values required. To verify this, Fig. 6 shows the simulated plots using MATLAB of the % error for both the first 6 harmonic orders and the first $\mathrm{OSR}-2$ orders of harmonic distortions across varying DAC quantization levels, with $\mathrm{OSR} = 64$.

Table I shows a detailed comparison between $S(t)$ and $Se(t)$, of the optimal DAC quantization steps required to minimize the harmonic distortion for a predetermined DAC resolution with $\mathrm{OSR} = 64$. $S(t)$ demonstrates enhanced linearity, particularly in the suppression of low order harmonics. This advantage translates to greater accuracy in bioimpedance measurements. Table II compares the simulated measurement accuracy of $S(t)$ and $Se(t)$ according to (4) and (5). Cases both with and without a second-order LPF are presented. The cutoff frequency of the LPF was set to twice the fundamental frequency of the signal. $S(t)$ achieves a better performance compared to the conventional pseudo-sine wave $Se(t)$ in both THD and measurement error especially with a low DAC resolution. The measurement error is defined as the difference between the calculated I/Q values and the ideal I/Q values. With only 4-bit DAC resolution, $S(t)$ provides an overall measurement error of 0.03% with second-order filters and $\mathrm{OSR} = 64$, which is sufficient for most bioimpedance measurement applications [22]. To achieve a similar level of performance, a 6-bit DAC is required by the conventional pseudo-sine wave $Se(t)$. Implementing the LUT according to $S(t)$ significantly reduces

TABLE III
DETAILED COMPARISON OF $y(t)$ AND $ye(t)$ AT OSR = 30

OSR = 30				
Harmonic order	7^{th}	11^{th}	13^{th}	Total
$y(t)$	5.4567	9.09%	2.94%	10.60%
$ye(t)$	8.83%	9.09%	4.75%	12.67%

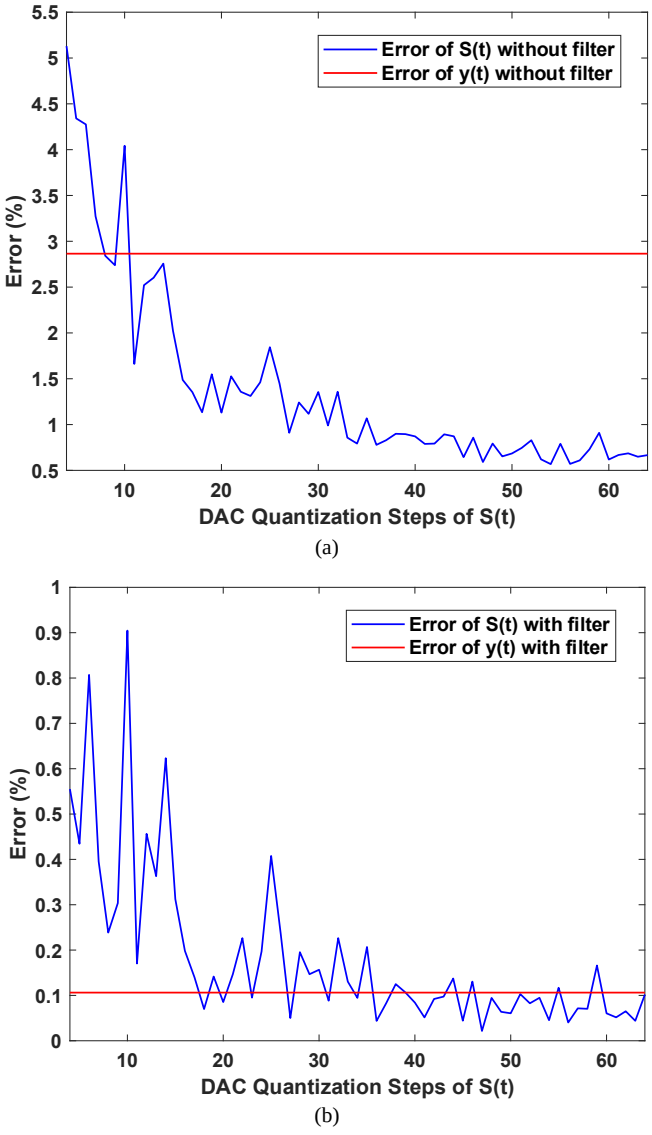


Fig. 8. The error of $y(t)$ and $S(t)$; (a) without LPF and (b) with LPF. OSR = 64, $y(t)$ quantization step fixed at 14.

chip area, design complexity and power consumption of the DAC and LUT.

D. Waveform With All Rational Steps

Although for limited DAC resolution, $S(t)$ shows a better performance compared to the conventional pseudo-sine wave $Se(t)$ after quantization, the low order harmonics due to quantization noise still exist. There would be further improvement if the waveform could fit all the magnitudes of the square waves to rational values. One of the possible approaches to solve this is to find a certain pattern with rational s_i which can cancel one order of harmonics and iterate such pattern to cancel all the orders of harmonic components required [24]. For waveforms combined by odd numbers of square waves as depicted in (8), one of the patterns is $p = 1$, $s_1 = 1/2$ and $\theta_i = \pi/3$, which can cancel the first, second and third harmonics. Extending this approach to the fifth order harmonic involves combining three signals, each already clean of the third harmonic, with phase shifts of 0, $\pi/5$, $-\pi/5$, and respective weights of 1, 1/2 and 1/2. Following this method, a general equation for cancelling any harmonic orders lower than p is:

$$y(t) = \sum_{n=1,3,5\ldots}^{p} \left(\frac{1}{2}\right)^{\frac{n-1}{2}} Sq\left(\omega t \pm \frac{\pi}{3} \pm \frac{\pi}{5} \pm \cdots \pm \frac{\pi}{n-2} \pm \frac{\pi}{n}\right) \quad (10)$$

According to (10), to cancel harmonic orders lower than p, an OSR of $2 \times 3 \times 5 \times \ldots \times (p-2) \times p$ is required. A DAC resolution of $(p-1)$ bit is required to fit all these quantization steps into an integer value. For signals based on the sum of even numbers of square waves as depicted in (6), a solution can also be derived by the same approach. It is given by:

$$ye(t) = \sum_{n=3,5\ldots}^{p} Sq\left(\omega t \pm \frac{\pi}{6} \pm \frac{\pi}{10} \pm \cdots \pm \frac{\pi}{2(n-2)} \pm \frac{\pi}{2n}\right) \quad (11)$$

Comparing $y(t)$ and $ye(t)$, an obvious difference is that $ye(t)$ only requires a total DAC step of $(p-2)$ instead of $(p-1)$ in $y(t)$. However, this is at the expense of increasing high order harmonic distortion. Table III compares $y(t)$ and $ye(t)$ with an OSR = 30, whose third and fifth order harmonics have been completely removed. As shown in the table, the total harmonic of $y(t)$ is much smaller than that of $ye(t)$, with better accuracy. Compared with $S(t)$, the advantage of $y(t)$ is that it can completely cancel a given number of harmonics due to the rational values of the quantization steps, but at the expense of much higher OSR. Fig. 7 shows the generated waveform of $y(t)$ and $ye(t)$ at OSR of 30.

To further explore the optimal design parameters, a testbench indicating the measurement error of $S(t)$ and $y(t)$ according to (4) and (5) was generated in MATLAB. To have a fair comparison, the OSR for $S(t)$ and $y(t)$ were set to 32 and 30, respectively. For this condition, only 14 DAC quantization steps are enough to quantize $y(t)$ without any quantization noise. Fig. 8 shows the simulated measurement error of $S(t)$ and $y(t)$. $y(t)$ has a fixed DAC quantization step of 14, while the DAC quantization step of $S(t)$ changes from 4 to 64 (2 to 6 bit). In Fig. 8(a), $S(t)$ provides higher accuracy from a DAC quantization step of 9 if no LPF is applied. Fig. 8(b) shows the error after applying a second-order LPF with a cutoff frequency twice the fundamental frequency. At a DAC quantization step of 18 (and over), $S(t)$ provides higher accuracy than $y(t)$. These simulation results reveal that without a LPF, $S(t)$ is more effective in providing a high accuracy measurement, while with a LPF, $y(t)$ can provide better performance when the DAC resolution is limited.

In conclusion, the equations for $S(t)$, $Se(t)$, $y(t)$, and $ye(t)$ demonstrate their efficacy in harmonic cancellation up to a specified order, underscoring their significance for high accuracy bioimpedance measurements. Notably, the harmonic

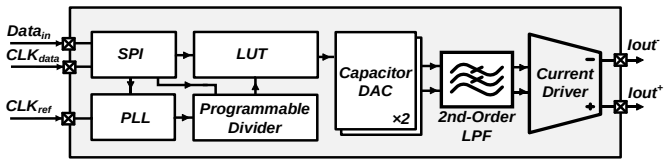


Fig. 9. The block diagram of the DDS-based SCG.

cancellation of $S(t)$ and $Se(t)$ exhibits a requirement for ideal quantization steps that include irrational values, necessitating judicious selection of DAC quantization steps to mitigate the presence of low order harmonics effectively. Of these two equations, $S(t)$ outperforms the conventional pseudo-sine wave $Se(t)$ in terms of linearity and measurement accuracy when the DAC quantization steps are optimally chosen. Conversely, $y(t)$ and $ye(t)$ present approaches that achieve perfect waveform quantization within the constraints of limited DAC resolution, thereby avoiding the production of additional low order harmonics. This advantage, however, comes at the expense of increased OSR requirement. While $y(t)$ is characterized by reduced high order harmonic content relative to $ye(t)$, the latter benefits from requiring fewer DAC bits. The analyses highlight the nuanced tradeoffs between harmonic suppression, DAC resolution, and OSR, guiding the selection of the most appropriate strategy based on specific application requirements and system constraints.

III. Hardware Implementation

A. Architecture Overview

The architecture of the proposed DDS-based SCG is shown in Fig. 9. It has a serial peripheral interface (SPI) for data communication, a phase-locked loop (PLL) and a programmable frequency divider to generate the required OSR, a LUT for generating the control pattern for the DAC, a capacitor DAC for converting the digital pattern into analog, a second-order LPF for removing high order harmonics and a CD for converting the sine wave voltage into current. For a high-performance on-chip DDS-based SCG, there are many design considerations in addition to the pattern of the LUT. These usually include: (i) minimizing the power consumption while maintaining the linearity of the LPF, (ii) ensuring current efficiency and preserving the linearity of the CD, and (iii) addressing the effects of DAC non-idealities on the overall linearity. This section examines these factors, providing an optimized design solution.

B. DAC Design

The performance of a DDS-based SCG is affected by the settling speed, linearity, and power consumption of the DAC design. The three principal DAC topologies for on-chip integration are the resistor DAC, utilizing resistors and switches, the capacitor DAC, comprising capacitors and switches, and the current DAC, based on MOSFETs and switches. The resistor DAC, constrained by the RC time constant from its resistive elements and load capacitance, requires a substantial quiescent current to attain rapid settling to ensure sufficient linearity, demanding significant chip area and careful layout for linearity

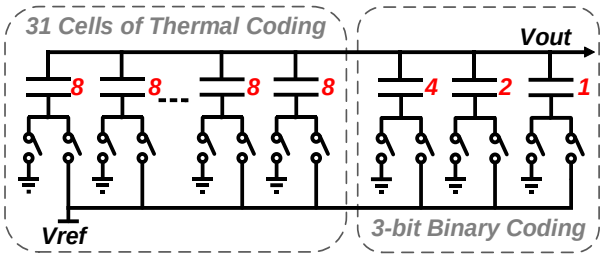


Fig. 10. Schematic of the 8-bit capacitor DAC.

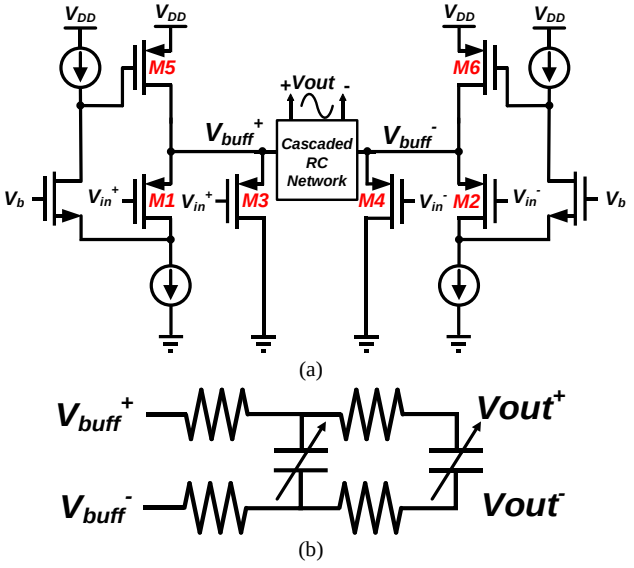


Fig. 11. Schematic of (a) the second-order LPF and (b) the cascaded RC network.

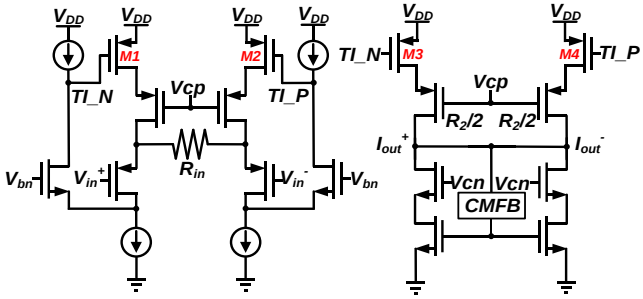


Fig. 12. Schematic of the current driver.

requirement, thus rendering it suboptimal for DDS-based SCG applications. On the other hand, MOSFET-based current DACs, although compact, have mismatch issues, necessitating dynamic element matching and added design intricacy to achieve pure sine wave generation. Additionally, in a MOSFET-based current DAC its settling speed directly correlates with power consumption.

Capacitor DACs are increasingly favored for high-linearity DDS-based SCG designs, with their fast-settling capabilities and no quiescent current needed. In addition, the utilization of on-chip metal-oxide-metal (MOM) capacitors offer exceptional matching performance, which significantly reduces the total capacitance value required and results in much smaller switching power consumption and chip area [25]. Consequently, an 8-bit MOM capacitor DAC has been selected for this design,

as shown in Fig. 10. To further minimize mismatches, the top 5 for most significant bits employ thermal coding, while the remaining three least significant bits utilize binary coding, providing a refined approach to enhance signal integrity and SCG performance.

C. LPF Design

In DDS-based SCGs the power efficiency and linearity of the LPF design are of paramount importance. Given the inherent lack of driving capability in capacitor DACs, the deployment of an active filter becomes necessary. The two prevalent methodologies for active filter realization are the gm-C filter and RC filter.

An active gm-C filter operates on the principle of capacitor charging and discharging via currents proportional to input voltage variations and the transconductance (*gm*). Nonetheless, this approach encounters challenges on the linearity of the *gm*, particularly under conditions when the input voltage has a large magnitude. As a result, the active RC filter, known for its superior linearity, is more frequently adopted. A widely utilized active RC filter configuration employs an operational transconductance amplifier (OTA) with resistor feedback, integrating a capacitor in parallel to the feedback resistor to establish the desired cutoff frequency [15]. However, the OTA usually requires a large current consumption to maintain a large open loop gain while driving the resistors and capacitors, which inevitably increases power consumption.

To circumvent these limitations, a filter architecture using a class-AB flipped voltage follower (FVF), as shown in Fig. 11 (a), was employed. This design provides enhanced linearity attributable to the FVF's intrinsic high linearity characteristics, functioning as a voltage buffer to efficiently drive the passive RC filter component. Notably, this configuration mitigates the need for excessive quiescent current to actuate the passive RC filter due to two key design features. Firstly, the source current, facilitated by transistors M5 and M6, is dynamically regulated by a feedback loop, enabling a substantial amplification of current levels by more than two orders of magnitude with minimal effort. Secondly, transistors M3 and M4 increase the current sinking capability, where their gate-to-source voltages equal the voltage differential across the FVF buffer's input and output. Consequently, as this voltage difference increases, current through M3 and M4 will also increase, which effectively increases the current sinking ability. The LPF uses a cascaded RC differential low pass network, as shown in Fig. 11(b). The passive network provides very high linearity. Programmable capacitors adjust the corner frequency of the LPF. Through these strategic design enhancements, the LPF achieves good linearity while substantially reducing power consumption. This LPF shows a THD less than 0.02% in simulation.

D. Current Driver Design

In contemporary on-chip SCG designs, the CD emerges as a power-intensive component, particularly in applications requiring substantial current delivery. It is, therefore, imperative to develop CDs that not only exhibit high efficiency but also maintain high linearity. Various CD architectures have been introduced, broadly categorized into open-loop and closed-loop configurations.

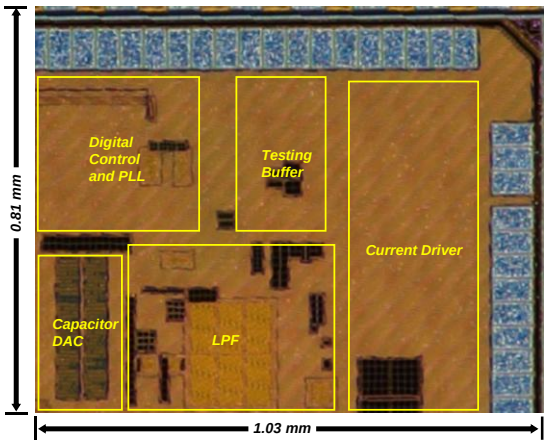


Fig. 13. Chip micrograph of the DDS-based SCG.

Closed-loop topologies often employ differential difference transconductance amplifiers (DDTAs), featuring a feedback resistor within the current injection loop. This design samples the voltage drop across the feedback resistor, with the DDTA adjusting the current to align this voltage drop with the input voltage, effectively setting the current to the ratio of the input voltage to the feedback resistor's resistance. This configuration tends to consume significant power to achieve accurate closed-loop gain, compromising current efficiency. Conversely, open-loop CDs benefit from their superior current efficiency but typically fall short in terms of accuracy. A CD based on current feedback was used in this design, which can provide high current efficiency, accurate current injection and high linearity [26-27]. The CD schematic is shown in Fig. 12. The output current is determined by the ratio between the current mirrors M1/M2 and M3/M4 times the input voltage divided by the input resistor R_{in}. Consequently, the output current level is well-defined. The CD has high linearity due to the intrinsic high linearity of the FVF structures, and high current efficiency due to its open-loop output stage. The current driver exhibits a THD less than 0.07% at 500 kHz and 1 mA load current in post layout simulation.

IV. Measured Results

A. Chip Overview

The DDS-based SCG for bioimpedance measurements was designed and fabricated in a 65 nm CMOS technology, with an area of 0.81 mm × 1.03 mm. The chip micrograph and the identification of each functional block is shown in Fig. 13. The DAC, PLL, LPF, digital logic and testing buffers use a 1.2 V supply, while the CD uses a 3.3 V supply to account for the output voltage needed due to the large variation of contact impedance between electrodes and human tissues. The 1.2 V power supply consumption of all the blocks working excluding the testing buffers is 84 μW at the maximum oversampling clock frequency of 64 MHz, where the PLL consumes 23 μW, the LUT consumes 39 μW, the LPF consumes 17 μW and the

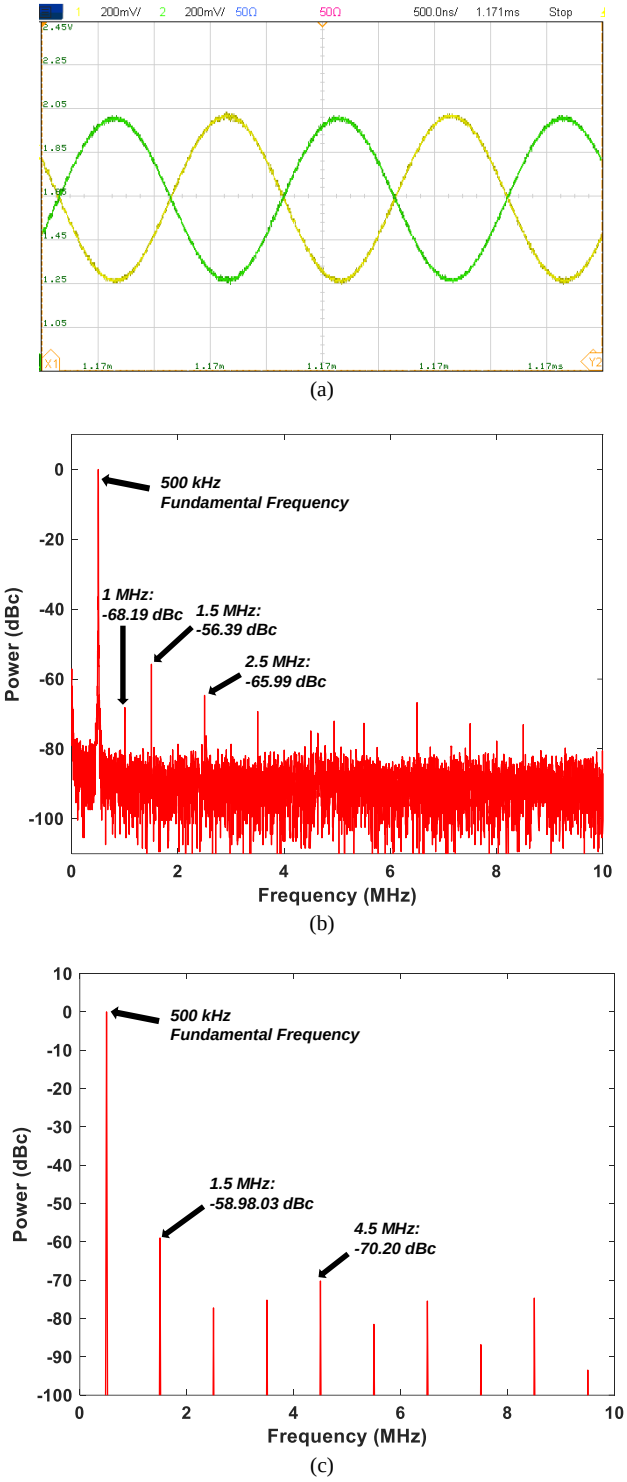


Fig. 14. Measured waveform of the SCG output with a 1.5 kΩ resistor load and (b) corresponding measured FFT spectrum and (c) spectrum from the ideal waveform.

DAC consumes 5 μW. The CD consumes 1.41 mA current with a maximum output current of 1.2 mA. The output signals were measured on a KEYSIGHT MSOX3024T mixed signal oscilloscope. A CMOD-A7 35T FPGA was used to control the chip and write in the LUT data to verify the performance with different patterns.

Fig. 14 shows the output current waveform of the SCG and the corresponding FFT spectrum when the full scale of the 8-bit DAC was used with no optimization at $OSR = 64$, output

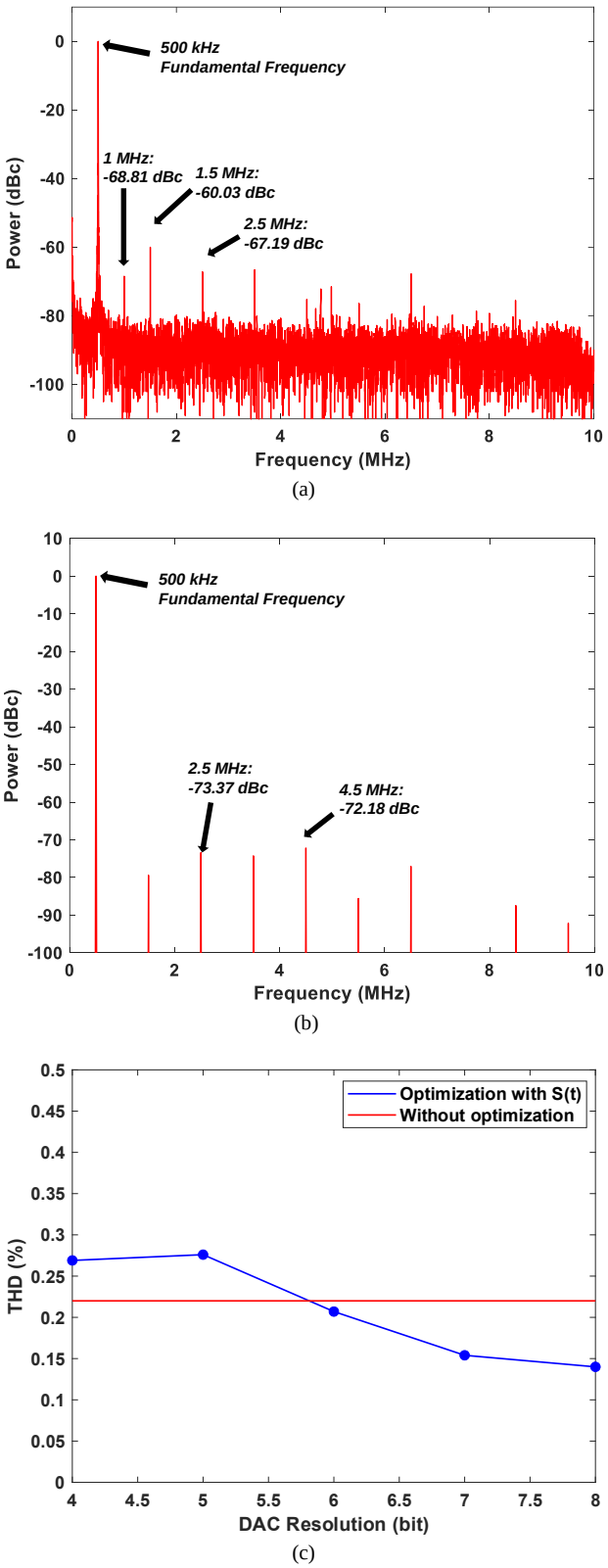


Fig. 15. (a) Measured spectrum of the waveform generated from $S(t)$ with 214 quantization steps, (b) spectrum from the ideal waveform and (c) measured THD with optimized DAC quantization steps under different DAC resolutions in comparison with the THD using full DAC scale without optimization at $OSR = 64$.

current of 1 mA, frequency of 500 kHz and 1.5 kΩ load resistor. It shows an overall THD of 0.22%. The simulated spectrum from an ideal wave is also presented in Fig. 14 (c) for

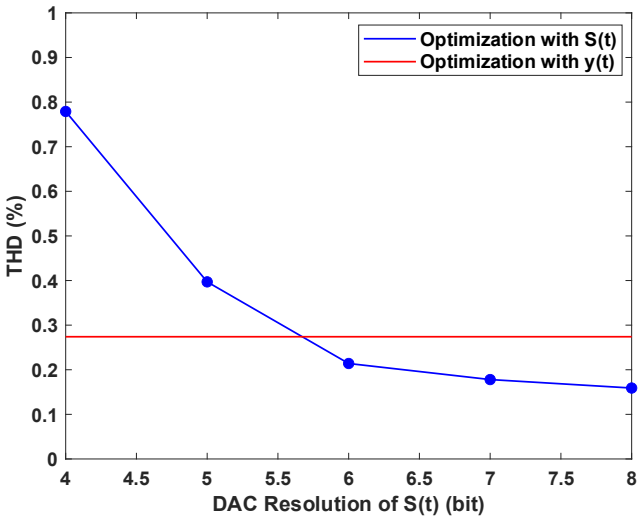


Fig. 16. Comparison between measured THD of $S(t)$ and $y(t)$. $y(t)$ quantization step fixed at 14.

comparison, which is based on the full scale of an 8-bit DAC with a second-order LPF It has a THD of 0.12%.

B. Optimized Results With Harmonic Cancellation

To verify the effectiveness of the derived waveform $S(t)$ by the proposed harmonic cancellation method, the LUT patterns were implemented according to the optimized DAC quantization steps in Table II with DAC resolutions from 4 to 8 bits at OSR $= 64$. For a fair comparison, the output current amplitudes were adjusted to be equal by changing the reference voltage of the capacitor DAC. Fig. 15(a) shows the measured spectrum of the waveform generated from an optimized (214 quantization steps) $S(t)$ pattern at OSR $= 64$. A significant improvement on third-order harmonic and fifth-order hormonic is observed, resulting in a THD of 0.13 %. The spectrum generated from an ideal waveform based on the same condition is also presented in Fig. 15 (b). It has an overall THD of 0.039%. Fig.15(c) compares the measured THD with optimized DAC quantization steps under different DAC resolutions and the THD measured directly using a full 8-bit DAC scale without optimization at OSR $= 64$. At $\geq$ 6-bit DAC resolution, the THD of the optimized design is lower than that without optimization. At 8-bit DAC resolution the THD decreases from 0.22% to 0.13% with the proposed optimization method. Fig. 15(c) suggests that with optimization, the SCG with a 6-bit DAC can achieve better linearity than an 8-bit DAC, while a 6-bit capacitor DAC has an area and power consumption four times lower than an 8-bit full scale capacitor DAC. The reason why the THD of the optimized design is slightly higher at 5-bit than 4-bit DAC resolution is because the optimized quantized steps in Table I were obtained without an LPF.

C. Comparison Between $S(t)$ and $y(t)$

Fig. 16 compares the measured THD performance between $S(t)$ and $y(t)$. $S(t)$ used an OSR $= 32$ and optimized DAC quantization step at each DAC resolution. $y(t)$ used an OSR $=$ 30 and a DAC quantization step of 14. The measured THD of the waveform generated with $y(t)$ is 0.27 %. $y(t)$ provides better performance than $S(t)$ when the DAC resolution is less than 6-bit. $y(t)$ is suitable for those applications where the DAC resolution and total power consumption are limited.

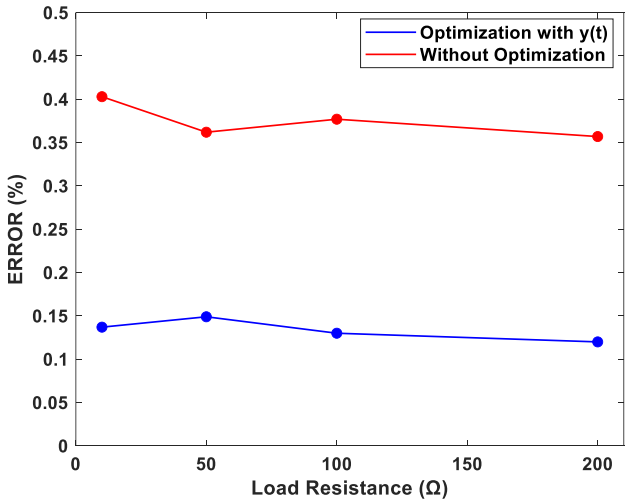


Fig. 17. Measured error of different resistive loads.

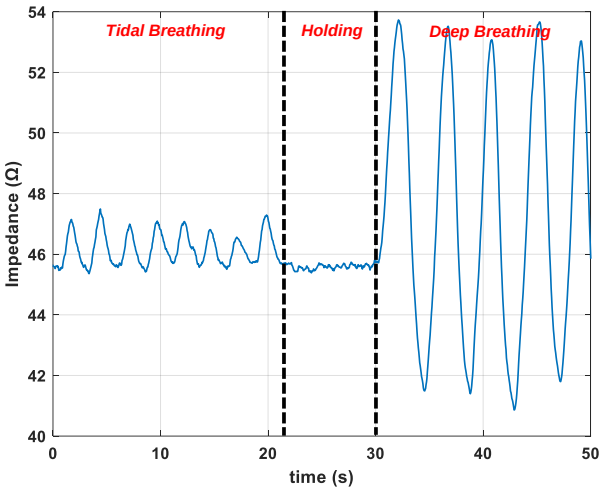


Fig. 18. Measured bioimpedance variation with breathing.

D. Validation with Impedance Measurement

To further verify the effectiveness of the proposed optimization method, resistive loads ranging from 10 Ω to 200 Ω were measured utilizing the two types of waveform: one optimized by $y(t)$ at OSR $= 30$ and a DAC quantization step of 14, and the other from a full scale 4-bit DAC (quantization step = 16) and OSR $= 32$.

A printed circuit board (PCB) was designed and fabricated using commercial off-the-shelf components to read out the impedances using digital I/Q demodulation. The regenerated voltage across the resistive load was recorded and amplified by two cascaded instrumentation amplifiers (AD8253 and LTC6373). The amplified voltage signal was then digitized by an analog-to-digital converter (AD9237). The digital I/Q demodulation was processed on a Xilinx Artix-7 FPGA (CMOD-A7-35T). To identify the measurement error due to the sinusoidal signal generator, the same impedance readout circuit was used to measure the same set of resistors with a KEYSIGHT 33600A Waveform Generator, used to generate a differential high quality sinusoidal input from the current driver. Results from this measurement were used as the reference for error calculations. The measured resistive errors are presented

TABLE IV
COMPARISON WITH PRIOR WORK

Parameter	JSSC'11 [28]	ASSCC'17 [29]	TCAS2'19 [30]	ISSCC'19 [15]	JSSC'21 [31]	**This work**	
CMOS Process	180 nm	65 nm	180 nm	130 nm	65 nm	65 nm	
Supply Voltage	1.5 V	1.2 V	1.2 V	1 V	0.5 V	1.2 V, 3.3 V	
SCG Type	Oscillator	DDS	DDS	DDS	DDS	DDS	
On-Chip Frequency Synthesizer	No	No	No	No	Yes	Yes	
Frequency	90 kHz	10 kHz–5 MHz	1 kHz–100 kHz	15 kHz–125 kHz	20 kHz	15 kHz–4 MHz	
Max. Output Current	350 $\mu A_{p\text{-}p}$	400 $\mu A_{p\text{-}p}$	160 $\mu A_{p\text{-}p}$	200 $\mu A_{p\text{-}p}$	2 $\mu A_{p\text{-}p}$	1.2 $mA_{p\text{-}p}$	
Current Efficiency	26.2%	17.2%	64.0%	37.1%	14.9%	81.0%	
LPF Order	N/A	N/A	1	2	2	2	
Digitization Resolution	N/A	N/A	12-bit DSM	8-bit	9-bit DSM	8-bit [c]	4-bit [d]
OSR	N/A	N/A	100	192 [a]	128	64 [c]	30 [d]
THD	<1%	0.5%	<0.4%	0.12%	0.088%	0.13% [c]	0.27% [d]
FoM [b]	N/A	N/A	13.3	10.1	7.6	62.5 [c]	125.0 [d]

[a] Calculated from the paper.

[b] $\text{FOM} = \frac{\text{Current Efficency}}{\text{Digitization Resolution} \times \text{LPF Order} \times \text{OSR} \times \text{THD}} \times 100.$

[c] Value of $S(t)$.

[d] Value of $y(t)$.

in Fig. 17. As shown in the figure, the proposed optimization method with $y(t)$ achieves an average of 2.6 times error reduction compared with conventional method without optimization. This reveals an effective method to increase the measurement accuracy when DAC resolution is limited.

The proposed SCG and the impedance readout PCB were also used in impedance pneumography measurement to record the bioimpedance variation during respiration [28]. A four-electrode arrangement was adopted on a test subject performing around 20 seconds of normal tidal breathing, followed by 7-8 seconds of holding breath, then five deep breathing. The measured impedance is shown in Fig. 18. The three different regions clearly show the impedance variations between tidal, holding, and deep breathing.

V. CONCLUSION

This paper has presented an optimization methodology based on harmonic cancellation for DDS-based SCGs. It provides a more efficient way to improve the linearity and reduce the measurement error in bioimpedance measurements. A DDS-based SCG for bioimpedance measurements has been designed and fabricated to prove the optimization methodology. The design shows significant improvement on linearity with reduced power consumption and hardware resources. Table IV compares the measured performance of the SCG with prior work. Optimization results for both $S(t)$ and $y(t)$ are presented. The optimization with $S(t)$ achieves four times reduction on DAC area and power consumption, while providing higher linearity. The optimization with $y(t)$ achieves 2.6 times improvement on the measurement accuracy when DAC resolution is limited. A figure-of-merit (FoM) related to OSR, digitization resolution, LPF order, THD and current efficiency is used to evaluate the overall performance of the state-of-art DDS-based SCGs. The SCG in this work shows at least 9.4 times improvement in FoM compared with other work. In addition to bioimpedance applications, the proposed techniques could also be used in the design of sinusoidal signal generators for other applications where high linearity and low power consumption are crucial. The detailed optimization code LUT data can be found in [32].

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