35.3 A 30MHz Wideband 92.7dB SNR 99.6% Accuracy Bioimpedance Spectroscopy IC Using Time-to-Digital Demodulation with Co-Prime Delay Locked Sampling

The permittivity and conductivity of bioimpedance in tissues are governed by α, β, and γ dispersions, with biological features detectable in the tens of MHz range. Wideband spectroscopy is required in many applications including body fluid volume assessment [1], cancer diagnosis [2], anatomical characterization [3], and plant content estimation [4]. However, state-of-the-art bioimpedance ICs are limited to frequencies up to 10MHz, which hampers biological research. For example, estimating starch content in cassavas requires wideband spectroscopy with frequencies up to 30 MHz [4]. In a wideband system using analog I-Q demodulation, accuracy is limited by the large distortion from its multiplication process; a phase error of 4.32° at 10 MHz was reported in [2]. In a wideband system using digital I-Q demodulation, a phase error of 0.15 % at 10 MHz was reported in [5] but at the expense of a large power consumption (12.2 mW for the amplifier and ADC alone) and a mediocre SNR of 65 dB. This paper presents a wideband (30 MHz) bioimpedance spectroscopy IC achieving both high SNR (92.7 dB) and high accuracy (99.6%) with low power consumption (3.18 mW). The IC employs time-to-digital (T-D) demodulation and features: 1) a novel co-prime delay-locked (CDL) sampling approach achieving an equivalent sampling rate of 21.6 GHz with a 240 MHz sampling clock; 2) a new delay-locked loop (DLL) architecture utilizing a compact phase comparator for high accuracy delay generation; 3) optimized wideband design for the current generator and readout front end to further reduce power consumption. The IC has only 0.39% magnitude error and 0.57° phase error at 30 MHz bioimpedance spectroscopy measurements.

Fig. 1 shows the block diagram of the IC. It consists of (1) a sinusoidal current generator, (2) a readout front end, (3) a clock generator and (4) digital modules. By injecting a current into the bioimpedance load, the induced voltage, V_m, can be measured. A resistor is connected in series with one of the recording electrodes for calibration. Based on the T-D demodulation principle in [6], dynamic comparators controlled by a known clock CLK_{comp} detect the crossing point between V_m and the known differential dc reference voltages $\pm V_{dc}$. The magnitude $|V_m|$ and phase θ of the measured sinusoidal voltage is extracted by counting 3 periods of pulses, $N_{0\text{-}2}$. Then the bioimpedance is calculated using the two equations shown in Fig. 1.

In all T-D demodulation methods, the IC's bandwidth and sensitivity depend heavily on the frequency of the CLK_{comp}; tens of GHz are required for 30 MHz bioimpedance spectroscopy. A normal GHz clock would significantly increase power consumption and design complexity. To overcome this, a CDL sampling approach is proposed, featuring a programmable pico-second-precision delay-locked clock generator for the dynamic comparators. As shown in Fig.2, the clock generator consists of two cascaded blocks, a 9-phase phase locked loop (PLL) and a 10-phase

DLL. The PLL generates a 9-phase 240 MHz clock with a step delay of T/9 where T (4.167 ns) is the period of the clock, and each phase is further delayed by the DLL at a step of T/10. Since 9 and 10 are co-prime numbers, the least significant delay (LSD) step is *T*/90 (46.3 ps or 21.6 GHz). The total delay at the DLL output is, $\tau_{total} = \left(\frac{pT}{9} + \frac{(q-1)T}{10}\right)$, where $p \leq 9$ and $q \leq 10$. The CDL sampling takes two steps as shown in the 30 MHz example in Fig 2. Firstly, for coarse comparison a 240 MHz CLK_{comp} is used, dividing the signal into coarse slots (8 slots for a 30 MHz signal) where two slots contain the cross points. Secondly, for fine cross point detection CDL sampling in the two slots is used. By controlling *p* and *q*, the CDL CLK_{comp} delay changes each cycle by one LSD until it covers the entire slot with a 46.3 ps temporal resolution, taking 3 μs (90 cycles).

The total delay of the DLL is first initialized to *T* (4.167 ns) in closed-loop operation before measurement, and then the DLL works as an open loop delay generator. To overcome the current mismatch in the charge pump (CP) and the dead zone of the phase-frequency-detector (PFD) in conventional DLLs, a new DLL architecture is proposed for generating an accurate 4.167 ns delay with 10 phases, as shown in Fig. 2 and Fig. 3. It has a phase comparator and a 10-bit resistive DAC (R-DAC) for defining the control voltage, *Vctrl*, for a voltage-controlled delay chain (VCDC). The VCDC is a 20-cell delay chain, from which 10 phases are selected by a dynamic element matching (DEM) module to randomize accumulated phase errors from single delay cells. Dummy delay cells are also used to isolate input and output offset from phase comparison. The measured VCDC delay versus *Vctrl* is shown in Fig. 3. A slope of 6.5 ps/mV was measured around the target delay time, where a 10-bit R-DAC with 1.2 V supply provides sufficient resolution. During closed-loop initialization, two pulses clipped from a 120 MHz clock (there are 20 delay cells), divided from a PLL output, are used as the input of the VCDC. The delay is defined by the time difference between the first rising edge of CLK_{ref} (input of delay cell 1) and CLK_{delay} (output of delay cell 20). The phase comparator has 3 D-flip-flops (DFFs) and a few logic gates. After *Reset*, DFF1 is triggered by the first rising edge of CLK_{ref} to release the reset pins of DFF2 and DFF3. The first arriving rising edge between CLK_{ref} and CLK_{delay} sets output *Q* of either DFF2 or DFF3 to logic 1, which in turn resets the other DFF. The difference between *Out1* and *Out2* determines whether the input of the R-DAC decreases or increases by one LSB. This procedure repeats until the rising edges CLK_{ref} and CLK_{delay} align, indicating an 8.333 ns delay (1/120MHz) has been achieved and the initialization is completed. The dead zone or resolution of the phase comparator is determined by the transmission delay difference between the complementary outputs of the DFF, *Q* and $\overline{Q}$ (a few ps), rather than the time required to switch on/off the CP in a conventional FPD (hundreds of ps). Within the dead zone, *Out1* and *Out2* are both either 0 or 1, depending on which one in *Q* and $\overline{Q}$ has a shorter transmission delay, as

shown in Fig. 3. The simulated dead zone was less than 5 ps, far smaller than 46.3 ps temporal resolution. A long enough time is allocated to the initialization process and the averaged value determines the final value of the R-DAC in the last 32 comparisons for noise integration. An 8.337 ns delay was measured after initialization, as shown in Fig. 3, with only 4 ps offset compared with the target 8.333 ns delay. The measurement was repeated 50 times to remove the impact of clock jitter. After initialization, the DLL operates in open-loop. The 240 MHz clock, CLK_{DLL}, is injected into one of the delay cells through the multiplexer (MUX) and the required delay is selected by another MUX, according to the values of p and q.

The block diagram of the current generator and readout front end are shown in Fig. 4. An optimized look-up-table (LUT) with 24 oversampling rates and 77 unit steps is used for high efficacy and linear sinewave generation [7]. The 720 MHz clock is multiplied from the 9-phase 240 MHz PLL to further reduce power. The trans-impedance (TI) filter after the current DAC exhibits high current efficiency and linearity since the transfer function only depends on passive components. A current feedback current driver is used due to its high efficiency and linearity [8]. The current generator can deliver a current from 15.6 µA to 500 µA, with a frequency from 10 kHz to 30 MHz. It achieves a measured THD of 0.39% at 3 MHz and 0.82% at 10 MHz. An instrumentation amplifier (IA) and a programmable gain amplifier (PGA) are used to amplify the voltage, providing a gain from 30 V/V to 150 V/V in 4 steps. Two dummy comparators with a complementary clock are used to compensate the kickback noise and reduce the value of load capacitors, which reduces power in the PGA. Resistors are connected in series before V_m and ± V_{dc} to balance the output impedance of the PGA and buffers for accurate measurements.

The IC was fabricated in a 65 nm CMOS process. High-frequency resistors from 10 Ω to 1 kΩ were measured at 30 MHz with pre-set current excitation level, ± V_{dc} voltage and PGA gain. A 3 ms measurement window was allocated to single impedance data for sufficient DEM and noise integration. The measured resistance at dc were considered to be the theoretical values and were used in error calculations. An overall magnitude error of 0.39% and phase error of 0.57° was achieved after calibration, as shown in Fig. 5. The accuracy decreases with increasing load resistance due to parasitic capacitances. The SNR was calculated from the mean values and standard deviation in continuously measured 3 s dataset (1000 data). R_{rms} is the corresponding standard deviation. An overall SNR of 92.7 dB was obtained and the R_{rms} varies from 0.24 mΩ to 23.3 mΩ with different loads. A spectroscopy measurement with various concentrations of cassava flour solutions is shown in Fig. 5, showing high accuracy bioimpedance data. A comparison with prior work is presented in Fig. 6. The chip micrograph is shown in Fig. 7. It occupies an area of 1.6 mm^2.

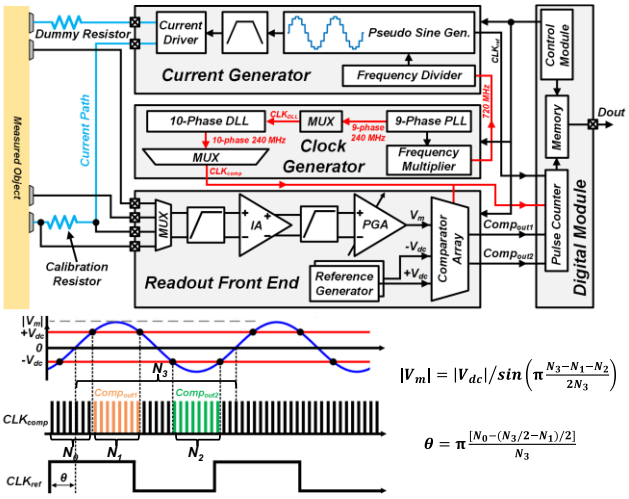

Fig. 1: Simplified block diagram of the proposed wide-band bio-impedance readout IC and the principle of the T-D method.

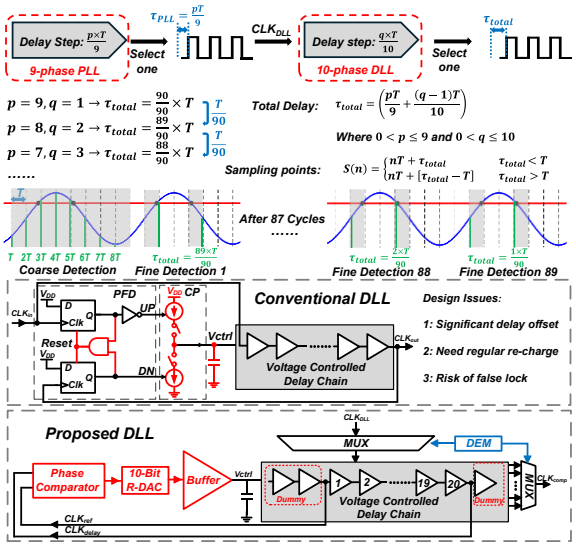

Fig. 2: Principle of the proposed co-prime delay locked sampling and the proposed DLL architecture.

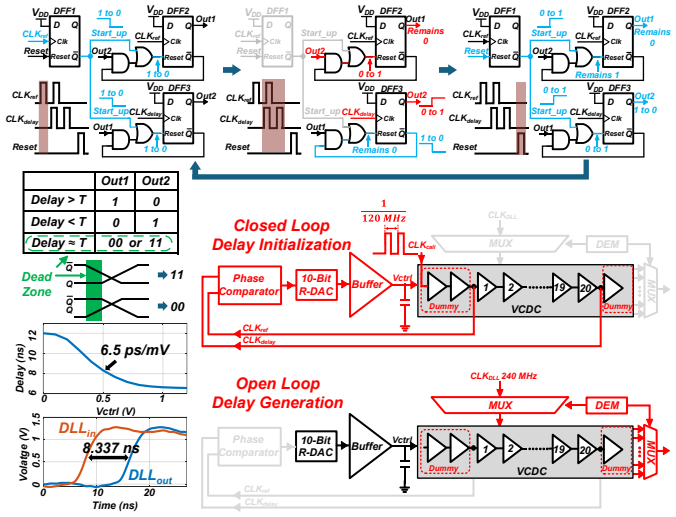

Fig. 3: Working principle of the proposed DLL and phase comparator, and the measurement results of the delay versus *Vctrl* and the generated delay after calibration.

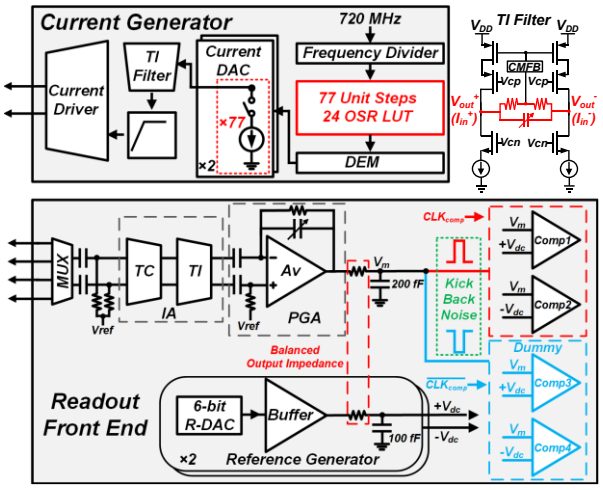

Fig. 4: More detailed diagram of the current generator, readout front end and the schematic of the TI filter.

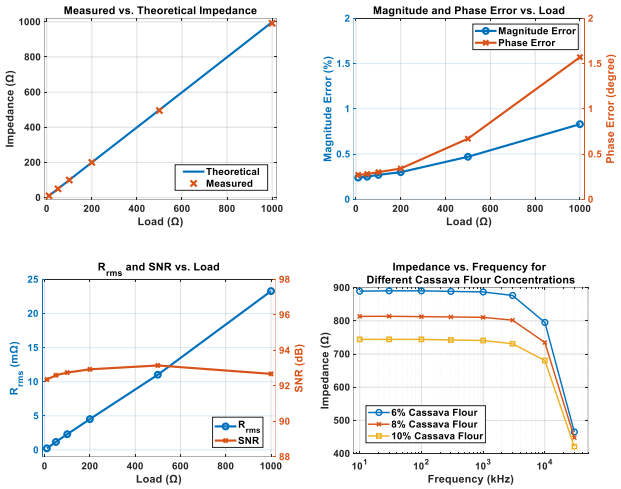

Fig. 5: Measured magnitude error, phase error, SNR and R_{rms} with different loads at 30 MHz and impedance of different cassava flour concentration solutions at different frequencies.

Parameters	TBCAS'19 [5]	JSSC'21 [2]	ISSCC'22 [10]	ISSCC'24 [11]	This Work
Technology (nm)	180	65	180	180	65
Supply (V)	N/A	1.8/3.3	1.8	1.2/0.9	1.2
Readout Method	Digital I/Q	Analog I/Q	Analog I/Q	Analog I/Q	T-D
Excitation Signal	N/A	Sine	Pseudo-sine	Pseudo-sine	Sine
Current Magnitude (μA_{pp})	N/A	Up to 3000	5-200	3-100	15-500
Frequency Range	100 Hz – 10 MHz	10 kHz – 10 MHz	1 kHz – 215 kHz	1 kHz – 200 kHz	10 kHz – 30 MHz
Max Power Consumption (mW)	12.2[a]	9.6[b]	0.27	0.167	3.18
SNR	65 dB at 10 MHz	N/A	103.5	101.5	92.7 dB at 30 MHz[c]
FoM[d]	104.1	N/A	142.5	142.3	142.4

[a]Only includes the power of amplifier and ADC.
[b]Excluding injection current.
[c]SNR = 20×log ($R_{average}/R_{rms}$), where R_{rms} is the standard deviation of the measured impedance and $R_{average}$ is the averaged impedance.
[d]FoM = SNR (dB) + 10×log(Max Frequency (kHz) / Max Power Consumption(mW))

Fig. 6: Comparison with prior work.

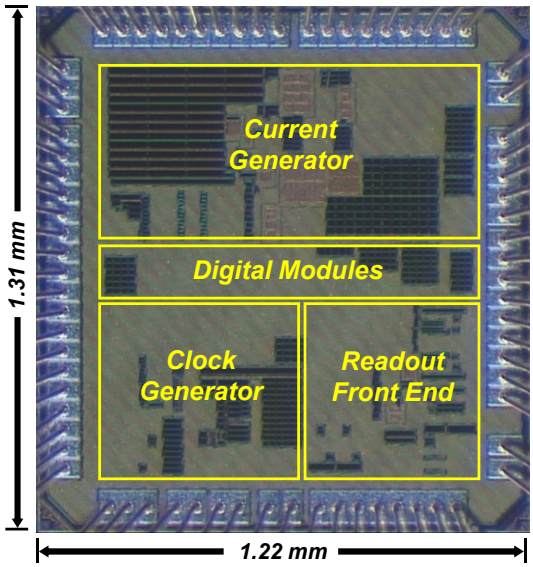

Fig. 7: Chip micrograph and die size.

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