

The Instrument Control Unit of the AIRS Instrument on-board the ARIEL mission: design status after PDR

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ABSTRACT

ARIEL (Atmospheric Remote-sensing InfraRed Large-survey) is the fourth medium-class mission (M4) of the European Space Agency, part of the Cosmic Vision program, whose launch is planned by late 2029. ARIEL aims to study the composition of exoplanet atmospheres,¹ their formation and evolution. The ARIEL's target will be a sample of about 1000 planets observed with one or more of the following methods: transit, eclipse and phase-curve spectroscopy, in both visible and infrared light. The scientific payload² is composed by a reflective telescope having a 1m-class elliptical primary mirror, built in solid Aluminum, and two focal-plane instruments: FGS and AIRS.

FGS (Fine Guidance System)³ has the double purpose of performing photometry (0.50-0.55 μm) and low resolution spectrometry over three bands (from 0.8 to 1.95 μm) and, simultaneously, to provide data to the spacecraft AOCS (Attitude and Orbit Control System).

AIRS (ARIEL InfraRed Spectrometer) instrument will perform IR spectrometry in two wavelength ranges: between 1.95 and 3.9 μm (with a spectral resolution $R > 100$) and between 3.9 and 7.8 μm with a spectral resolution $R > 30$.

This paper provides the status of the ICU (Instrument Control Unit), an electronic box whose purpose is to command and supply power to the AIRS warm front-end (as well as acquire science data from its two channels) and to command and control the TCU (Telescope Control Unit).

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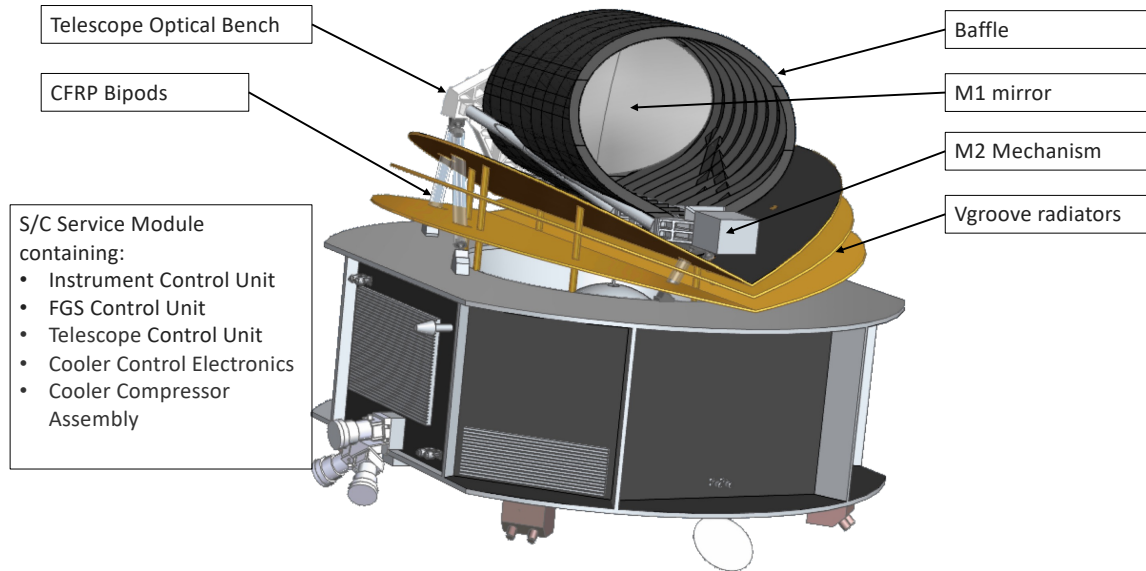


Figure 1: The ARIEL S/C with its main components. The ICU is hosted inside the Service Module (warm side)

Keywords: Exoplanets atmospheres, NIR spectroscopy, Infrared radiation, Infrared telescopes, Remote sensing, Instrument Control Unit

1. INTRODUCTION

ARIEL (Atmospheric Remote-sensing InfraRed Large-survey)⁴⁵ is a medium-class (M4) mission part of the Cosmic Vision program of the European Space Agency. The launch is planned by late 2029 in a twin configuration with Comet Interceptor on an Ariane 6-2 vector from the Kourou Space Centre in French Guiana. The planned mission duration is 4 years, plus 2 years of extended mission. ARIEL's scientific purpose is the study of the composition of exoplanet atmospheres,⁶ their formation and evolution, by performing infrared spectroscopy of a large number of transiting exoplanets with temperatures from $\sim 500\text{ K}$ to $\sim 3000\text{ K}$. During its mission ARIEL will observe about 1000 planets with one or more of the following methods: transit, eclipse and phase-curve spectroscopy.

The ARIEL⁷⁸ spacecraft is based on an off-axis Cassegrain telescope with an elliptic $1\text{ m} \times 0.7\text{ m}$ primary mirror, built in aluminum and feeding, by means of an optic system (dichroics, mirrors and prisms), two instruments:

- AIRS (ARIEL InfraRed Spectrometer) that will perform IR spectrometry in two wavelength ranges: between 1.95 and $3.9\ \mu\text{m}$ and between 3.9 and $7.8\ \mu\text{m}$.
- FGS (Fine Guidance System), an instrument with three narrow-band (from visible to near-infrared) photometric channels (two of these are used as guidance sensors as well as for science) and a low-resolution near-infrared spectrometer.

This paper reports the AIRS Instrument Control Unit (ICU) design status and gives an overview of its development stage after the Instrument PDR (Preliminary Design Review)⁹ representing a milestone for the ICU design definition. The first models foreseen by the model philosophy illustrated in Section 4.1 (MD and EM/AVM) have been realized. In Section 2 we describe the AIRS instrument, in Sections 3.1 and 3.2 we go in detail with the internal architecture of the boards composing the ICU and in Section 4 we illustrate the ICU development plan, including a description of the past, present and future activities.

2. THE INSTRUMENT CONTROL UNIT ROLE

The ARIEL IR Spectrometer (AIRS)⁵ is an instrument performing high stability spectroscopy in two different wavelength bands: from 1.95 to 3.9 μm (channel 0, CH0), and from 3.9 to 7.9 μm (channel 1, CH1). The resolving power is greater than 100 for channel 0 and greater than 30 for channel 1. The scientific data will result in cropped windows of 355×64 pixels for CH0 and 130×64 pixels for CH1. The number of levels (depth) of the H2RG detectors is 16 bits.

2.1 AIRS structure

The light collimated by the telescope is folded by mirrors and split in the various wavelength components by an optic system based on dichroics. The component with larger wavelength ($> 1.95 \mu\text{m}$) is fed to the AIRS box.

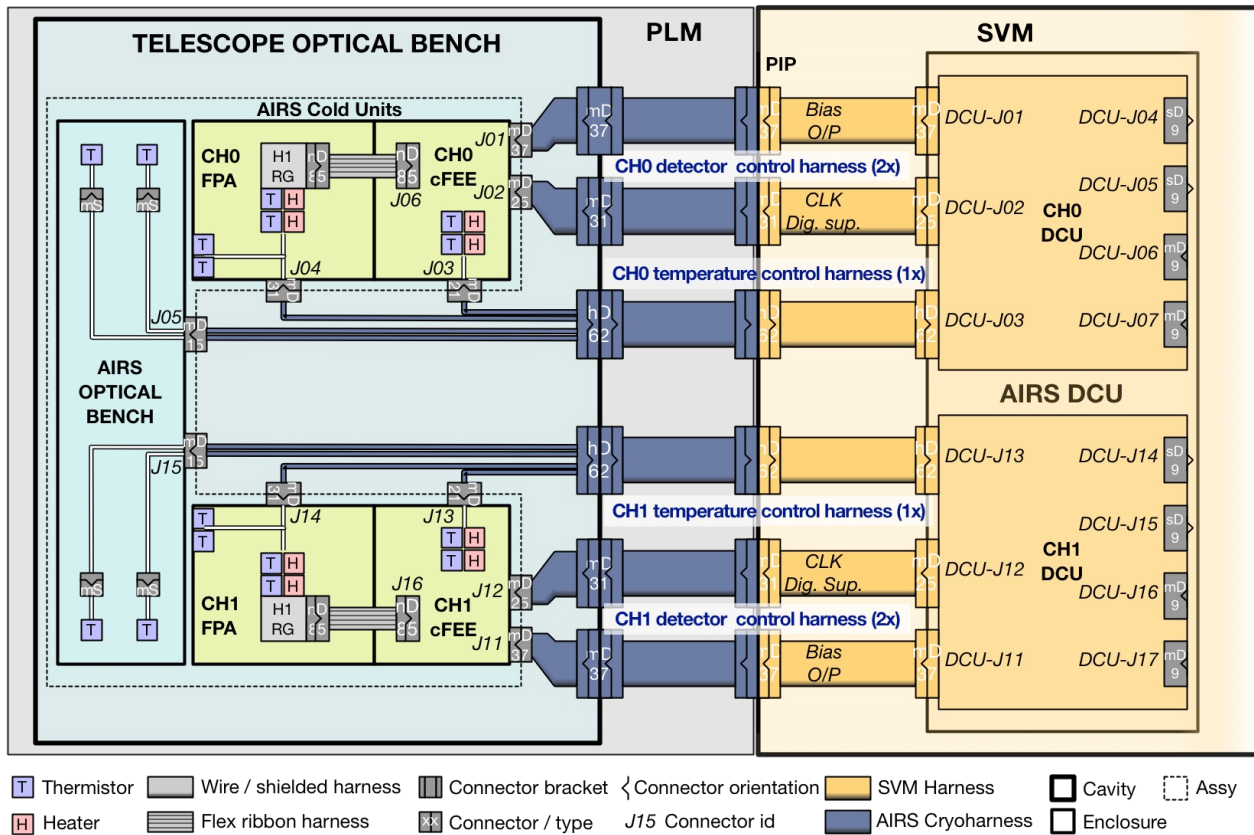


Figure 2: AIRS Electrical Block Diagram (Courtesy CEA).

The AIRS instrument is composed of¹⁰ :

1. A metallic enclosure situated in the cold part of the payload (@ 55 K) in the instrument bay, a cavity carved in the Telescope Optical Bench (TOB) and containing, for each channel:
 - (a) The final parts of the optics: slits, folding mirrors, prisms (the dispersive elements), filters etc.
 - (b) Two H2RG (Teledyne) detectors, cooled down to 42 K by a cold finger
 - (c) The cold Front-End Electronics (cFEE)
2. The A-DCU (warm Front-End Electronics) that is an electronic box accommodated in the “warm” side of the spacecraft,⁷ at a temperature of about 300 K. The two A-DCU modules control and read out the detectors.

Figure 2 shows a scheme of the AIRS system, from the cold part of the Payload Module containing the detectors and the cFEE to the A-DCUs. The ICU connects to the A-DCU on the right of the figure by means of two SpW connectors (MDM9) and two Power connectors (DSub9) for each A-DCU module.

The ICU interfaces the S/C (and Ground) with AIRS, managing the data streams (Science and *Housekeepingings*) coming from the AIRS instrument and commanding the two A-DCU boards, each one committed to process the data of one AIRS channel.

2.2 ARIEL DCU

Into the cFEE it is implemented the preamplifier for the ROIC (ReadOut Integrated Circuit). Others functions, such as the readout clock sequencer and the bias voltages generation, reside into the warm electronics (A-DCU). Figure 3 illustrates the distribution of functions between the A-DCU and the cFEE.

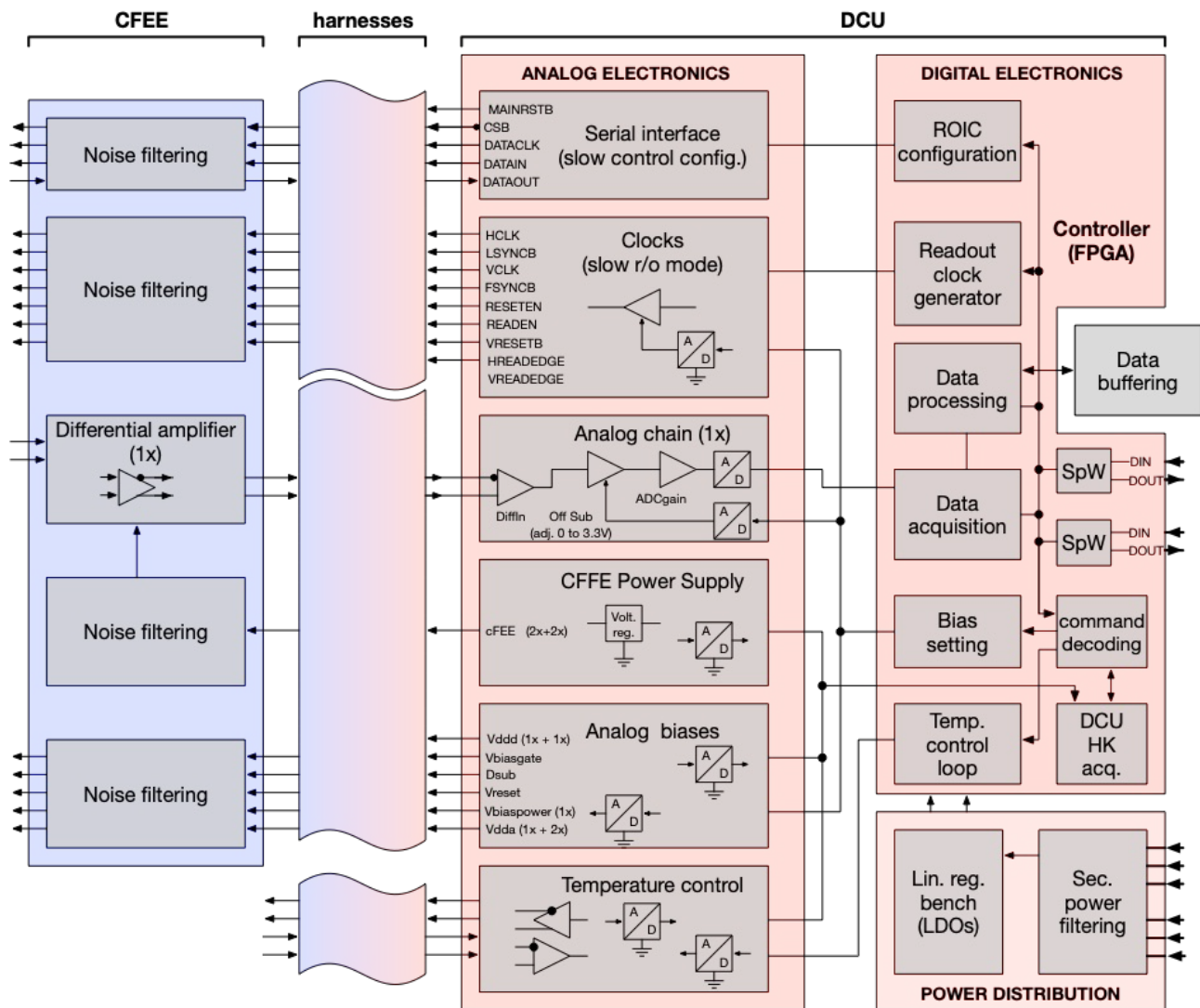


Figure 3: AIRS Detailed Electrical Diagram (1 channel) (Courtesy CEA).

The A-DCU main functions are:

- Send commands and the needed secondary voltages to the cold Front-End Electronics

- Digitize the scientific data from the detector prior the formatting of the Science Data Packets performed by ICU
- Ensure the proper interface with the ICU for Telecommands (TC) reception, Science and HK Data Packet transmission
- Control of the thermal stability of detectors (duplicated to increase reliability)

The ICU is connected to the A-DCUs by means of four cross-strapped SpW (SpaceWire) links. The redundancy is not complete due to the singleness of the A-DCU boards (one board for each channel). The ICU provides also the secondary power to the A-DCUs (analog $\pm 6V$ and digital $+5V$), see Figure 5.

2.3 Telescope Control Unit

Beside the A-DCUs, the ICU manages another warm electronic box, the Telescope Control Unit (TCU), that is in charge of:

- Drive the Mirror#2 Mechanism (M2MD)
- Monitor the thermal state of the Payload (Vgrooves and Telescope);
- Communicate with the ICU CDPU and transmit HK data: internal, thermal sensors readouts and from the M2M

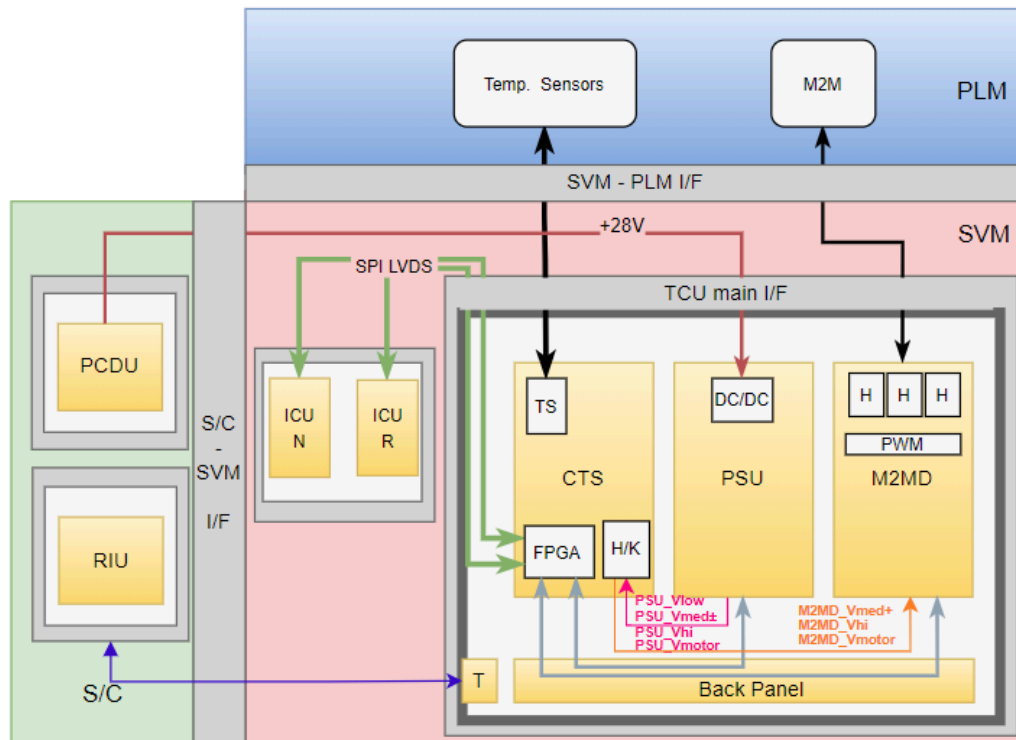


Figure 4: TCU Electrical Block Diagram, the green arrows are the SPI connections with the ICU (Courtesy IEEC)

The TCU digital system is based on a FSM (Finite State Machine) encoded in a FPGA (RT3PE3000L-CQ256). The system's registers are written by the ICU upon reception of telecommands from the Service Vehicle Module (SVM) and are read back to extract housekeeping data that the ICU re-sends as telemetries

(TM). The M2M Driver provides to the M2M motors the switching sequences contained in the telecommands translated by the ICU and acquires the status information that will be provided to the FPGA and forwarded to the ICU to be sent as housekeeping telemetries.

The TCU receives the primary voltage (+28V) directly from the S/C and its PSU (Power Supply Unit) board operates all the necessary conversions to supply the other TCU boards and the M2M motors.

The TCU is fully redundant and is connected to the ICU by means of a fully cross-strapped SPI (Serial Peripheral Interface), based on LVDS signals. The TCU design and realization responsibilities are in charge of IEEC (Spain) and part of the boards are realized by the industry (SENER).

3. ICU DESCRIPTION

The ICU¹¹¹² system is composed by two cold-redundant modules:

1. CDPU (Control and Data Processing Unit) that is, in turn, made up by a motherboard (CPU) and a carrier board hosting the FPGA
2. PSU (Power Supply Unit)

The currently estimated ICU mass is 6.3 kg (7.5 kg including Design Maturity Margin) and the allocated power is 37 W. The ICU is connected to the S/C computer by four cross-strapped SpW links for data transmission, and is powered, with the regulated +28V, by the PCDU (Power Conditioning and Distribution Unit).

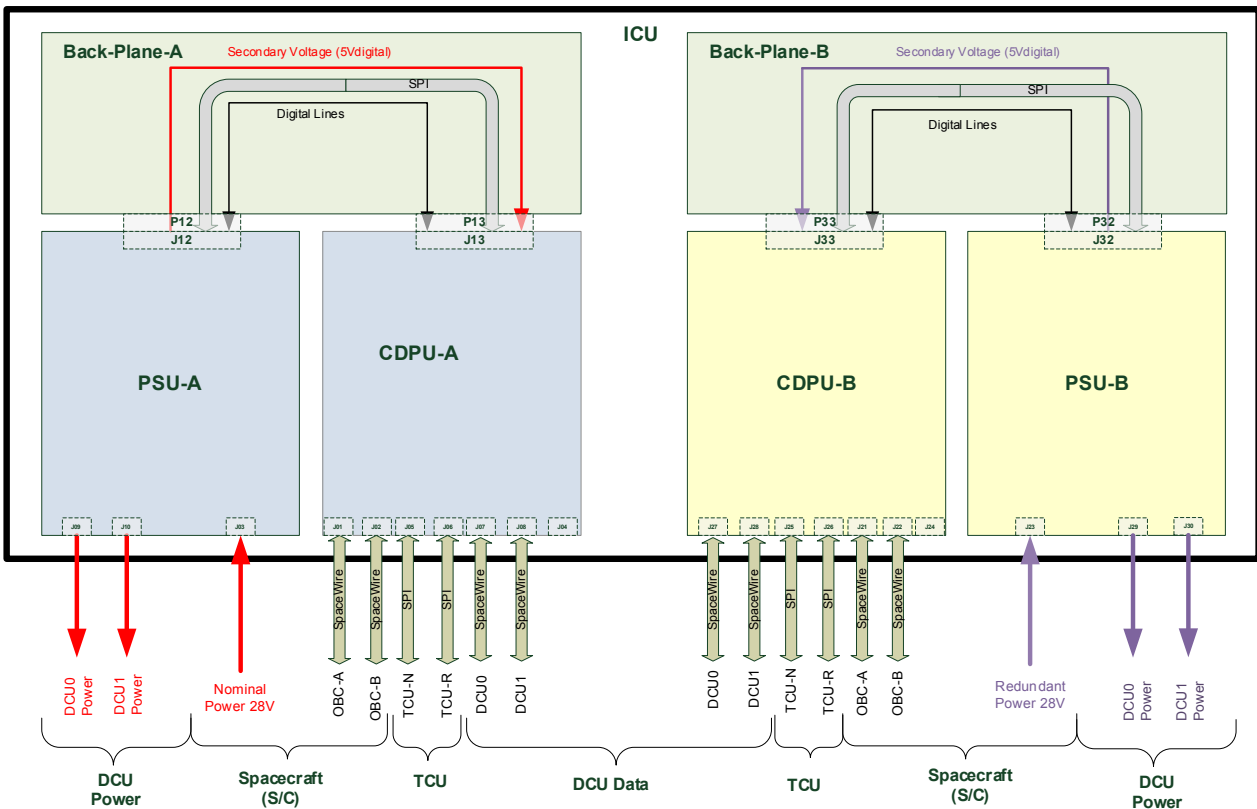


Figure 5: ICU internal architecture and data interfaces (Courtesy Kayser Italia).

3.1 CDPU module boards

Due to space constraints, the components needed to populate the CDPU module have been allocated on two separated boards: the CDPU itself, tied to the mechanical structure of the drawer, and the FPGA daughterboard (or carrier board) that is connected to the previous by means of board-to-board connectors.

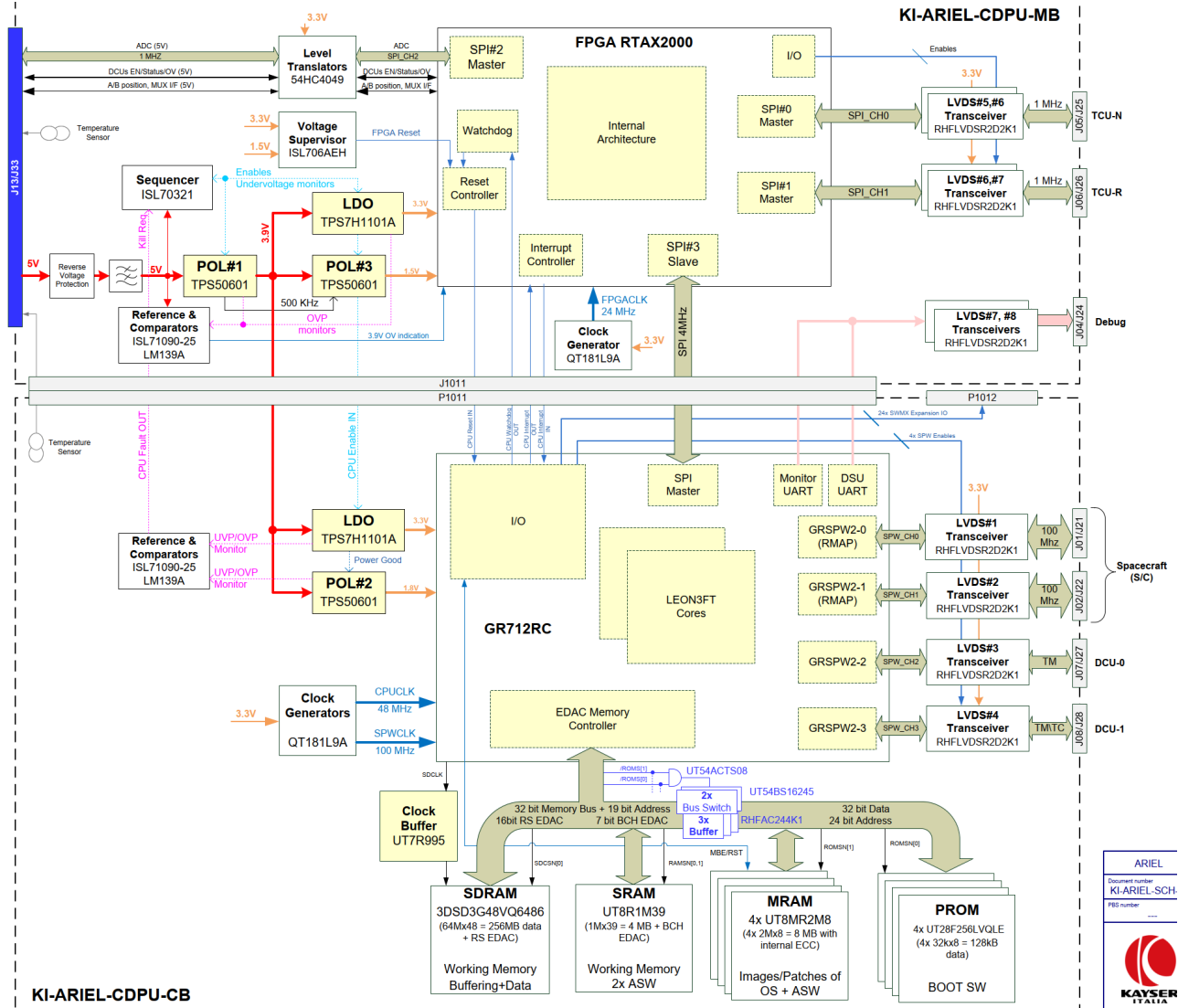


Figure 6: CDPU module block diagram (Courtesy Kayser Italia).

3.1.1 CDPU motherboard

The CDPU motherboard hosts a dual-core CPU (Cobham Gaisler GR-712RC), equipped with several types of memory:

- **PROM** to host permanently the Boot Software (128kB);
- **MRAM** Magnetic RAM (Non-Volatile Memory) to store different images of the Application Software (8MB);
- **SDRAM** to buffer transmit data (256MB);

- **SRAM** used as working memory for the Application SW processing (4MB).

All these memories (with the exception of the PROM, that is One Time Programmable) are protected against events caused by radiation by an EDAC (Error Detection and Correction) system. The two main CDPU components, that is the CPU and the FPGA, are connected through an internal SPI bus.

The CPU is based on the Leon3-FT (Fault Tolerant), a synthesizable 32-bit SPARC-V8 processor, suitable for space applications.

The CPU runs the Application SW in charge of managing the AIRS instrument and the TCU. The ASW also processes the data (science and housekeeping) collected from the monitored subsystems.

3.1.2 FPGA carrier board

The FPGA (Microsemi RTAXS2000) provides additional computational resources to accomplish the compression task on scientific data (a 2.5 compression ratio is baselined), but adds also ports for communications. In fact, the GR712RC is endowed with only six SpaceWire ports, not sufficient for all the communication needs as shown in Figure 5. The FPGA modules shall be developed using VHDL language, so it is possible to test the design using reprogrammable (A3PE3000) devices during the prototyping phases and migrate easily the design to the flight (the RTAXS2000 is programmable only once) devices.

The +5V voltage supplied by the PSU is further transformed on-board the CDPU boards: first in an intermediate 3.9V, in order to avoid potentially dangerous failures, and after in the low voltages needed by the CPU and the FPGA cores (1.8 and 1.5 Volt, respectively) and the 3.3V.

3.2 PSU board

The PSU (Power Supply Unit) hosts different DC/DC converters transforming the regulated +28V (primary supply voltage) into:

- **+5V** secondary supply to power the internal electronics and equipped with overvoltage and overcurrent protections
- A-DCUs' secondary voltages (isolated)
 1. **+5V** for the digital section
 2. **±6V** for the analog section

The secondary digital and analog isolated voltages are needed to power AIRS: feeding directly its wFEE (A-DCUs) and indirectly, by means of the latter, the AIRS cFEE and detectors. Each PSU provides the power to both A-DCUs with separated lines. The CDPU can switch on and off the power via discrete isolated commands.

The PSU performs HK acquisition using a multiplexed 12-bit serial ADC (ADC128S102) controlled by the processor via a SPI bus for voltage, current and temperature measurements.

All the housekeeping data (internal and relative to A-DCU secondary voltages) will be transmitted to S/C as telemetries together with the data collected from the other controlled subsystems (TCU and A-DCUs).

The distributed power is equipped with over-voltage protection and LCLs (Latching Current Limiters, see Figure 7), switching off the power in case the currents exceed the limit. No active limitation of the in-rush current is foreseen (that is controlled upstream by the SVM LCL function); the maximum variation ($1A/\mu s$) is guaranteed by the passive circuitry of the input EMI filter. The CDPU over-voltage protection is based on a comparator with hysteresis without latching. In case of a temporary over-voltage, the CDPU and the A-DCU are switched off and re-enabled by an automatic reset. The PSU and CDPU boards are switched on following a power-on sequence managed by the PSU, after which the Boot SW (BSW) can start. The PSU is supplied from the SVM through a +28V regulated bus protected by a class 3 LCL.

The LCL feeding the A-DCUs, instead, are normally switched off and can be turned on by the CDPU with dedicated digital enable signals (+5V and ±6V separately). In case there is a problem on the A-DCUs (e.g. an abnormal current absorption), the current is limited to a maximum value and, after a given time, a trip-off condition is reached. The CDPU module detects this condition by means of the status digital signals and reports it to the SVM as housekeeping telemetry.

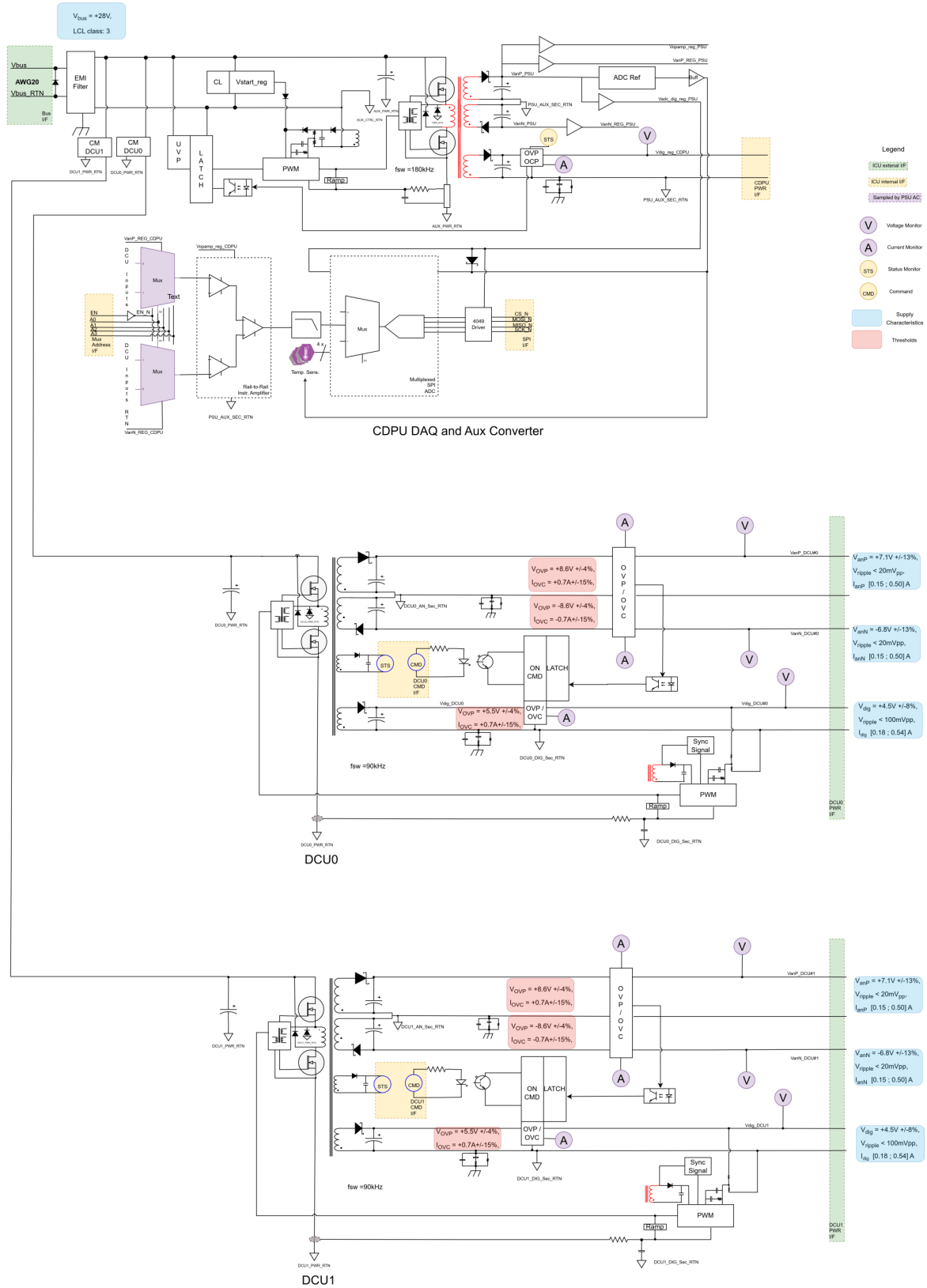


Figure 7: PSU module block diagram (Courtesy Kayser Italia).

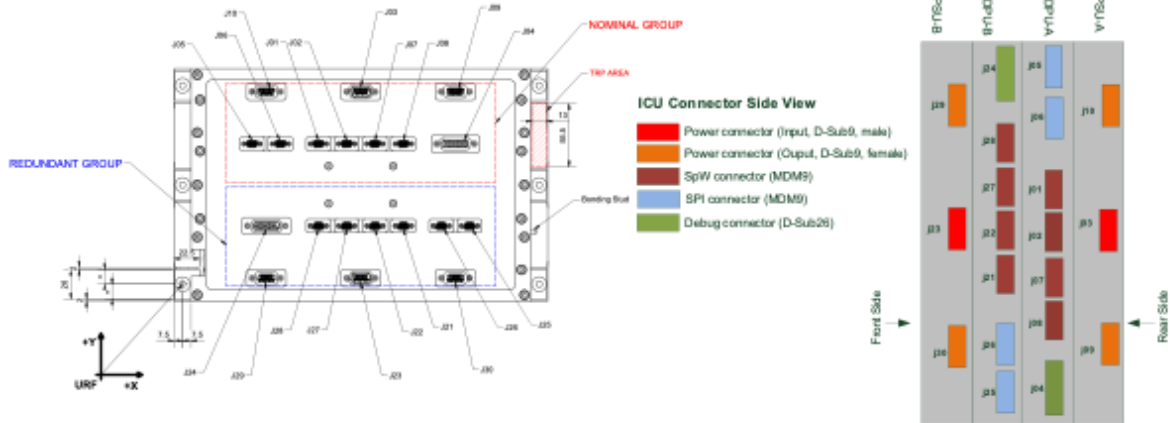


Figure 8: Connectors allocation on the top of the ICU box (Courtesy Kayser Italia).

3.3 ICU Mechanical Design

The ICU mechanical structure has been designed as a single box hosting the four redundant modules ($2 \times CDPU$ and $2 \times PSU$). The PSU are single boards, while the CDPU are double.

The PCB boards are screwed to the modules' frames. The four drawers are inserted from the top and the boards are electrically interconnected by a back-panel placed at the bottom or by board-to-board connectors. The drawers are laterally kept in position by means of Calmark *Card-Lok* retainers that also ensure the thermal coupling of the frames (and hence of the boards) with the lateral panels of the box structure.

The box dimensions are $330 \text{ mm} \times 205 \text{ mm} \times 220 \text{ mm}$ ($L \times W \times H$, against an allocated volume of $330 \text{ mm} \times 220 \text{ mm} \times 220 \text{ mm}$).

The box, made of aluminum alloy type AA 7075-T7351, is black-anodized externally (in accordance with ECSS-Q-ST-70-03C) to improve the radiating exchange with the environment. The unit will be fixed to the SVM panel by means of 2×5 M6 screws placed on the lateral panels.

4. ICU ACTIVITIES

4.1 ICU Model Philosophy

The ICU Model Philosophy, comprises the following models:

1. **Breadboard (BB)** a Cobham-Gaisler GR712RC development board, used for Application SW development
2. **Mechanical Dummy (MD)**, Mass, Volume and other mechanical properties representative (CoG, MoI). Contributes to the spacecraft SM campaign (Airbus)
3. **Engineering Model (EM)**, functional and electrical representative of flight standard, used for Application SW development (one board) and for the EM campaign at RAL
4. **Avionics Verification Model (AVM)**, EM build standard, functionally representative and with flight representative interfaces. Contributes to the spacecraft AVM campaign (Airbus)
5. **Engineering Qualification Model (EQM)**, flight representative in form, fit and functions, i.e. including electrical, printed circuit boards, thermal, mechanical fidelity. Used for SW development, not a deliverable, can be used for environmental qualification
6. **proto-Flight Model (pFM)**, final model for integration in the ARIEL PL and launch
7. **Flight Spare (FS)**, spare boards ready to substitute one of the FM boards in case of major problems

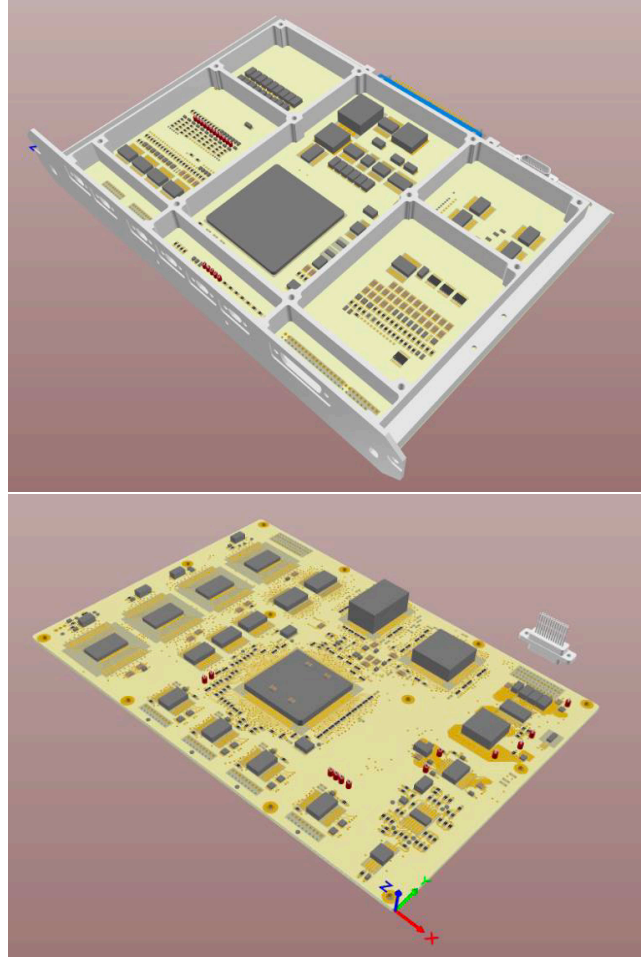


Figure 9: Isometric views of the two boards composing the CDPU (Courtesy Kayser Italia).

Table 1: ICU models utilization summary.

Model	# of ch.	Purpose	Deliv. date	Notes
BB	1	SW development	end 2021	INAF internal
MD	NA	Contributes to S/C SM camp.	Nov.2023	Deliv. to ESA/ADS
EM	2	Assess design & SW development	on-going	Deliv. to RAL for EM campaign
AVM	2	Contributes to S/C AVM camp.	Jan.2025	Deliv. to ESA/ADS
EQM	2	SW development & qual. tests	Dec.2025	Not deliverable
pFM	2	Integrated in PL FM	Sep.2026	Complete acceptance tests at box level
FS	1	Board spares	Sep.2026	Limited acceptance tests

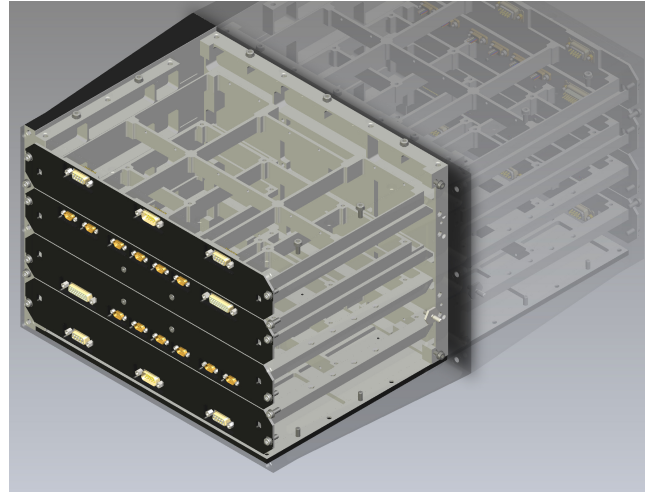
4.2 SW development

The ICU hardware described above needs, necessarily, different kind of SW to operate properly:

1. **BSW**, Boot SW
2. **BSP**, Basic Support Package
3. **ASW**, Application SW
4. **CSW**, Compression Software to be integrated in the ASW



(a) The ICU box mechanical drawing.



(b) An internal view of the ICU structure.

Figure 10: Two images of the ICU mechanical structure (Courtesy Kayser Italia).

5. FW, FPGA Firmware is programmed in VHDL language

The Operative System is a commercial component (RTEMS): a Real Time OS that is space-qualified and adopted by ESA. The drivers (Basic Support Package) needed to interface the Application Software with the OS are developed by Kayser Italia that is also in charge of realizing the ICU, its BSW and the FPGA FW, developed in VHDL (VHSIC Hardware Description Language).

4.2.1 Boot SW

The Boot SW is executed when the unit is powered on, performing the following tasks:

- Check HW integrity
- Initialize communication with the S/C
- Wait for TC to boot the ASW image stored in the NVM or to save a new ASW image

The BSW is a simple but, at the same time, very critical piece of software because it is not replaceable when in space. Due to its uniqueness, it has to be carefully developed and extensively tested before the final version. The definitive version of the Boot SW used in flight is "burned" in a One-Time-Programmable PROM.

4.2.2 Application SW

The Application SW is developed by INAF-OATo and INAF-IAPS and represents the software running on the CPU in charge of implementing all the functions needed to satisfy the mission needs:

- Manages the memories
- Manages the SpaceWire and SPI links
- Communicates with the TCU and the A-DCU, translating the S/C Telecommands
- Executes the FDIR (Fault Detection Isolation and Recovery) procedures for the ICU, the A-DCU and the TCU
- Packetizes the Science and HK data to be sent as Telemetries to the S/C

The Compression Software (CSW) is the part of the ASW implementing the lossless compression routines and is developed by the Wien University.

5. SUMMARY AND CONCLUSIONS

In this paper we have given an overview of the present design status (June 2024) of the ARIEL Instrument Control Unit. The electronics has been designed by Kayser Italia in accordance to the relevant requirements and specifications provided by INAF.

The ICU hardware has successfully passed the PDR (Preliminary Design Review) milestone and in these days the ICU project is facing the ASW, BSW and FPGA PDRs.

The detailed design of the boards (CPU, FPGA and PSU) is definitive and the dimensions and budgets are consolidated. The Mass Dummy of the metallic box has been realized (see Figure 10a) and several analyses (thermal and structural-FEM) have already been performed on this design. At the beginning of 2024 the first CPU board has been delivered to OATo to allow the development of the ASW and the production of the PSU and FPGA boards is on-going.

ACKNOWLEDGMENTS

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