A 1.76 mW, 355-fps, Electrical Impedance Tomography System with a Simple Time-to-Digital Impedance Readout for Fast Neonatal Lung Imaging

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***Abstract*—Functional lung imaging for neonates using electrical impedance tomography (EIT) requires a fast frame rate to avoid under sampling the faster respiratory rate in neonates than adults. Also, the EIT system must have low power consumption to facilitate wireless operation during kangaroo care. The application of existing EIT systems primarily designed for adults is limited by the trade-off between power consumption and speed of the impedance readout. This paper presents an integrated EIT system in a 65 nm CMOS node featuring a novel ultra-low-power time-to-digital impedance readout method based on dc cross-point-detection. To increase the resolution of the impedance readout, a dynamic comparator with multi-phase VCO-based least-common-multiple coherent clock control is used, yielding a measured impedance error of 0.94 % and a phase error of 0.81° over a frequency range from 100 kHz to 500 kHz in a 10 µs measurement time. In addition, a novel fast-settling switch matrix allows multiplexing the single impedance readout channel, significantly decreasing power consumption without degradation in speed. The EIT system has a maximum frame rate of 355 fps and a total power consumption of 1.76 mW. The impedance readout and digitization consume 172 µW, a power reduction of 83-93% compared to prior work. The frame rate is both suitable for neonatal lung imaging and other fast EIT applications. Both in-vitro and adult in-vivo measurements are presented.**

***Index Terms*—EIT, impedance readout, time-to-digital, coherent sampling, multi-phase PLL.**

I. INTRODUCTION

EVERY year, more than 13 million babies are born prematurely, many facing respiratory failure due to underdeveloped lungs and unregulated breathing. While respiratory support, particularly mechanical ventilation, enhances survival rates, it can also inflict serious harm on their delicate lungs. This often leads to chronic lung conditions extending into adulthood. A key factor in the mortality and morbidity related to respiratory failure is the heterogeneity of lung aeration, characterized by overinflation and collapse in different lung areas. Current bedside monitoring tools and imaging techniques fail to detect this uneven distribution of lung aeration, highlighting the urgent need for a continuous, non-invasive method to monitor infant lung function in neonatal intensive care units.

Electrical impedance tomography (EIT) can offer real-time, cost-effective, and radiation-free monitoring, with recent studies confirming its efficacy in assessing lung aeration in preterm infants [1]. EIT is an imaging method that maps the conductivity inside a body. It is widely used in lung monitoring [2]-[4], human-machine interfaces [5], and cancer detection [6]-[7]. The common working principle of EIT is injecting a known ac current at the boundary of a domain and measuring the induced voltages at the boundary. Electrode pairs at different locations provide a transimpedance dataset for image reconstruction. Neonate respiratory rates can be over five times faster than adults [8]. As a result, for effective neonatal lung monitoring with EIT, a high frame rate [>120 frames per second (fps)] is desirable to prevent misinterpretation of the reconstructed images due to artifacts caused by under sampling the lung volume changes [3], [9]. In addition, clinical outcomes for preterm babies are significantly improved with kangaroo care (continuous and prolonged skin-to-skin contact of the baby with the mother) [1], [10], [11]. In order to facilitate wireless operation during kangaroo care, a low power EIT system would be required to ensure extended battery life.

The trade-off between power consumption and speed creates major challenges for the impedance readout in EIT systems. I/Q demodulation is commonly used to derive the resistive and reactive parts of bioimpedance. In I/Q demodulation, the measured signal is multiplied by in-phase and quadrature signals at the injection frequency, and the products are low-pass filtered to dc to extract the resistive and reactive parts, respectively. As shown in Fig. 1, I/Q demodulation can be implemented in either analog or digital circuits. Analog implementation is power efficient, but the large time constant in the low-pass filters (LPFs) renders a long demodulation time

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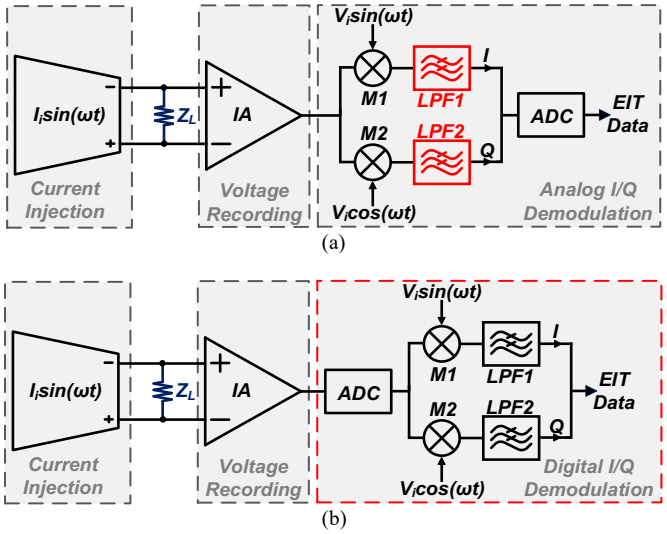


Fig. 1. Simplified block diagram of (a) analog I/Q demodulation and (b) digital I/Q demodulation.

and a low frame rate [2], [4], [12]. Digital implementation can achieve fast demodulation (by operating at a MHz level clock), but at the expense of high-power consumption, because of the high-frequency analog-to-digital conversion (ADC) and digital signal processing [3], [13].

Various strategies have been explored to address this trade-off in EIT systems. One approach involves providing each recording channel its own analog demodulation circuit with all channels operating in parallel [2], [4]. This can provide a fast frame rate but at the expense of a significant increase in circuit complexity and implementation cost. A recently proposed synchronous sampling method [14] with parallel recording achieved over 300 fps with low-power consumption by injecting a square-wave ac current and only sampling a fixed point of the induced voltage, eliminating the need for low-pass filtering. However, the absence of phase measurement is unsuitable for regional lung analysis in neonates.

To address these challenges, an integrated EIT system with a novel ultra-low-power, high-speed, noise-resistant, time-to-digital (T-D) impedance readout method is presented. By detecting the crossover points between the recorded sinusoidal voltage and a known dc reference voltage using a dynamic comparator, both the phase and magnitude can be easily derived from the time difference between their crossing points. In addition, a multi-phase least-common-multiple (LCM) coherent sampling method is proposed to control the dynamic comparator, achieving a high temporal resolution over a wide range of injection frequencies with high speed and low power consumption. Furthermore, to decrease power consumption, a fast-settling switch matrix is proposed for multiplexing a single-channel impedance readout to 16 electrodes with minimal speed penalty. Utilizing the aforementioned methods, the EIT system is capable of 355 fps with a total power consumption of 1.76 mW, of which the impedance readout only consumes 172 μW. Its high frame rate is suitable for both neonatal lung imaging and other fast EIT applications such as imaging neuronal activity [15].

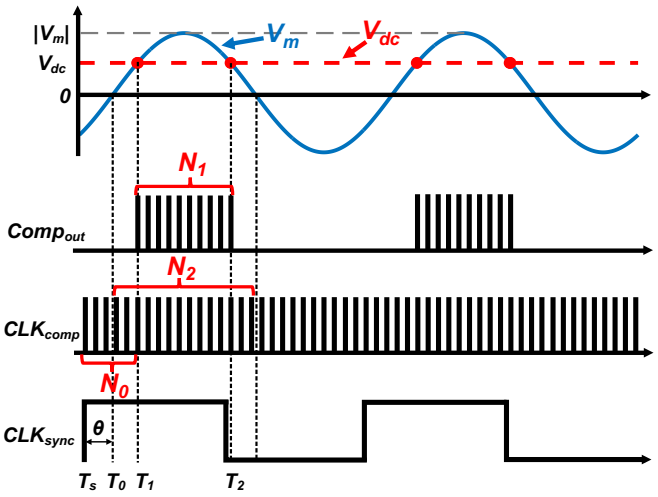


Fig. 2. Principle of the T-D impedance readout method.

The rest of this paper is organized as follows. Section II describes the proposed impedance readout and LCM coherent sampling methods, together with supporting concept level simulations. Section III presents the architecture and detailed circuits of the integrated EIT system. Measurements including in-vivo lung imaging are presented in Section IV. Comparison with other work and concluding remarks are provided in Section V.

II. Proposed T-D Impedance Readout Method

A. Operating Principle

The fundamental principle of the impedance readout method involves identifying the time intersection points, T_1 and T_2, between a pre-defined dc voltage V_{dc} and the half cycle of the measured sinusoidal voltage V_m, as shown in Fig. 2. The mid-point of the interval T_1 to T_2 defines the time when the sine wave is maximum from which its phase can be deduced. Knowing the phase, the dc voltage and the sine wave frequency, the magnitude $|V_m|$ can be calculated as:

$$|V_m| = |V_{dc}| \Big/ \sin\left(2\pi f_{sig} \frac{\frac{1}{2f_{sig}} - (T_2 - T_1)}{2}\right) \qquad (1)$$

where, f_{sig} is the excitation frequency, and T_1, T_2 represent the crossover times of V_{dc} and V_m. The phase θ is deduced by measuring the time difference between T_s (the rise time of the clock reference CLK_{sync}, synchronized with the injecting current signal) and T_0 (the zero-crossing time of V_m). The value of T_0 is:

$$T_0 = T_1 - \frac{\frac{1}{2f_{sig}} - (T_2 - T_1)}{2}. \qquad (2)$$

Consequently, the phase θ is given by:

$$\theta = 2\pi \frac{T_0 - T_s}{f_{sig}} = 2\pi \frac{\frac{T_1}{2} + \frac{T_2}{2} - \frac{1}{4f_{sig}} - T_s}{f_{sig}}. \qquad (3)$$

In practice detecting T_1 and T_2 is efficiently achieved using a

dynamic comparator controlled by a known sampling signal and counting the output pulses of the comparator. The magnitude is given by:

$$|V_m| = |V_{dc}| / \sin\left(\pi \frac{N_2 - N_1}{2N_2}\right) \quad (4)$$

where N_2 is the number of clock pulses in a half signal cycle, and N_1 is the number of pulses between T_1 and T_2. The phase can be measured by counting the clock pulses, N_0, between the rising edge of CLK_{sync} and T_0. The phase θ can be calculated as:

$$\theta = \pi \frac{[N_0 - (N_2 - N_1)/2]}{N_2}. \quad (5)$$

This T-D impedance readout method offers two significant improvements compared to traditional approaches. Firstly, it has high speed with low power consumption since there is no LPF speed limitation (unlike I/Q demodulation) and only one dynamic comparator is required for both magnitude and phase digitization. Secondly, it is resistant to amplifier saturation as long as the crossover point stays below the saturation threshold, which is especially advantageous in lung EIT systems where the signal amplitude varies greatly with the depths of respiration.

B. Noise Reduction With Multi-Phase LCM Coherent Sampling

In a T-D impedance readout, both the quantization noise of the dynamic comparator and the signal noise of the recorded voltage can degrade the accuracy of the digitized magnitude and phase. As the input is a sine wave, the quantization noise is determined by the phase resolution, the ratio between the signal frequency and the comparator sampling frequency. However, as the frequency of the injecting signal increases, it becomes challenging to generate a high sampling frequency to retain the phase resolution.

To remedy this, LCM coherent sampling can be used. It is especially effective for signals that are periodic in nature, allowing for an enhancement in phase resolution [16]. The principle is shown in Fig. 3(a). For a signal with a frequency $1/M$ and a sampling frequency $1/N$ that are not harmonically related (i.e. their frequencies do not form a simple whole-number ratio), LCM coherent sampling can be achieved by setting the total sampling window T to the LCM of the signal period, M, and the comparator sampling period, N. In the example shown in Fig. 3(a), T comprises six signal cycles with 11 slots per cycle, i.e. $M = 11$. The sampling period is every six slots, i.e. $N = 6$. As the system samples each cycle of the signal, it introduces a consistent phase shift. This shift equals $360^\circ \cdot (N/T)$. After the full sampling window T has elapsed, the accumulated phase shift will cover a full 360-degree cycle. This yields an increase in phase resolution by a factor of T/M (the resolution is enhanced by the number of signal cycles that have been taken over the duration T). While LCM coherent sampling can increase phase resolution and thus decrease quantization noise, it requires an extended measurement duration, which is problematic for high-speed EIT operation.

To circumvent this limitation, a multi-phase LCM coherent sampling method is proposed. Instead of using a single-phase clock, a multi-phase clock is used to boost the measurement speed. Since the multi-phase clock signal, labeled as a P-phase clock, provides intrinsic phase shift between each phase, it can be effectively interpolated into the LCM coherent sampling process and compresses the sampling window from T to T/P provided P is an integer divisor of T/M. An example of interpolating 3 different phases is shown in Fig. 3(b). Compared with directly using a much higher sampling clock frequency, this multi-phase sampling approach can provide higher power efficiency. A ring oscillator, the most used oscillator in the MHz frequency range, has at least 3 different phases of clock signals with the same frequency. Hence, it can provide a simple multi-phase clock interpolation without extra cost and thus consume less power compared to directly increasing the oscillator's frequency. For accurate frequency generation, a ring voltage-controlled oscillator (VCO) controlled by a fractional-N phase locked loop (PLL) is used to lock the free-running oscillator frequency to a pre-defined value. In this design, a 10-phase, 4.99 MHz clock signal is selected. For a signal frequency of 100, 200, 300, 400 and 500 kHz, a total number of 499 different sampled points can be re-ordered into one signal cycle with a sampling period of 1, 2, 3, 4 and 5 cycles for each frequency, respectively. Hence, for a constant measurement time of 10 µs, an effective phase resolution of $(1 \div 499) \approx 0.2\%$ signal cycle can be achieved for each frequency, which is sufficient for both speed and accuracy. The values of the parameters used in this design are listed in Table I.

Although quantization noise is significantly reduced by the multi-phase LCM coherent sampling method, the challenge of the signal-to-noise ratio (SNR) at the comparator inputs remains. According to (4) and (5), the value of the phase magnitude is determined by N_0, N_1 and N_2, where N_0 and N_1 are affected by noise, and N_2 is a pre-determined value. In this

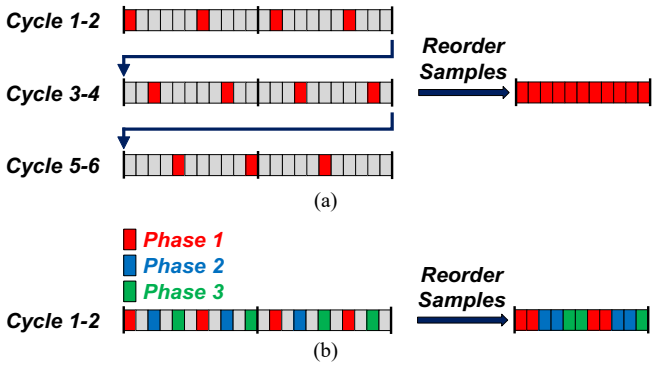


Fig. 3. Increasing temporal resolution by (a) LCM coherent sampling and (b) multi-phase LCM coherent sampling.

TABLE I
PARAMETERS USED IN THE LCM DESIGN

Parameter	Definition	Value
T	Total Sampling Window	10 µs
$1/M$	Signal Frequency	100–500 kHz
$1/N$	Sampling Frequency	4.99 MHz
P	Number of Phases	10

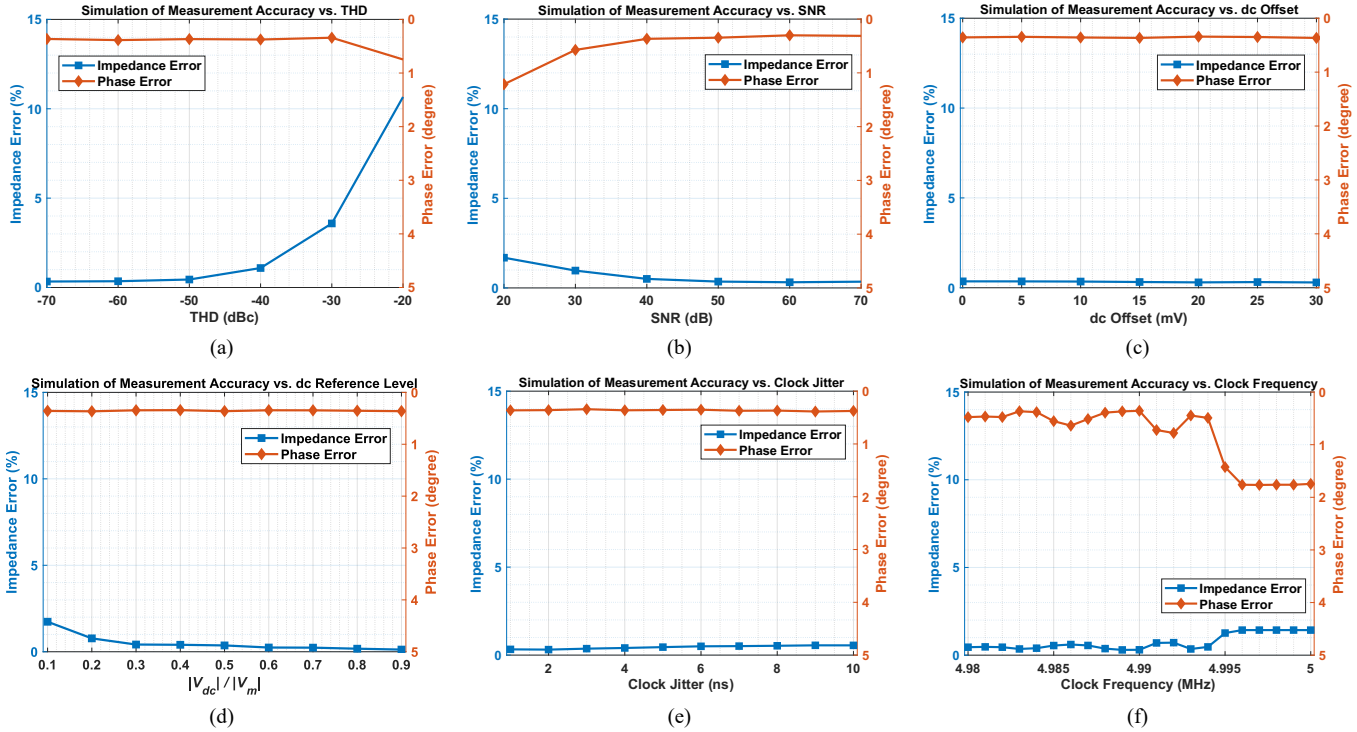


Fig. 4. MATLAB simulations of measurement accuracy as a function of (a) THD, (b) SNR, (c) dc offset, (d) dc reference level, (e) clock jitter and (f) clock frequency.

design, the impact of signal noise which exceeds the quantization step is significantly reduced by the high equivalent sampling rate of the multi-phase LCM sampling method in two ways. Firstly, since most noise follows a Gaussian distribution, the probability of incorrect positive or negative comparison is the same. Consequently, as the sampling frequency increases, N_0 and N_1 will converge towards their ideal value. Secondly, the impact of a given number of comparison errors decreases as the equivalent sampling frequency increases. In this design, with a fixed total of 499 sample points per measurement, the impact of a random noise-induced comparison error is equivalent to increasing the quantization noise from 0.2% per cycle to 0.4%. For comparison errors up to 3, the equivalent quantization noise rises to 0.8%, and with 7 errors to 1.6%. These levels remain sufficiently accurate for EIT measurements.

C. Concept Level Simulations

The accuracy of the proposed T-D impedance readout method is affected by non-idealities such as total harmonic distortion (THD), SNR, dc offset, clock jitter, inaccurate dc reference level and frequency mismatch. Concept level simulations in MATLAB (MathWorks, Natic, MA, USA) were used to examine the phase and magnitude measurement accuracy of a sinusoidal voltage with 0.4 V magnitude and 500 kHz frequency. A differential dc voltage superimposed on a common mode signal was used for cross-point detection, increasing immunity to the dc offset of the programmable gain amplifier (PGA) and even order harmonic distortion. A 4.99 MHz, 10-phase clock was used to sample the cross-point, achieving an effective temporal resolution of 0.2% signal cycle with 5 cycles of measurement, resulting in a measurement window time of 10 µs. The sinusoidal voltage had a default THD of 50 dBc and SNR of 40 dBc. The clock had a random clock jitter up to 500 ps and the value of the dc reference was chosen to be half the magnitude of the sinusoidal voltage. The THD comprised second and third harmonics of equal value. The simulated results are shown in Fig. 4. They suggest several key strategies for circuit implementation: 1) The THD of the sinusoidal voltage should be less than -40 dBc to attain a high magnitude measurement accuracy [Fig. 4(a)]; 2) The measurement accuracy of the magnitude and phase is insensitive to changes in the SNR of the impedance readout circuits when SNR >30 dB [Fig. 4(b)]; 3) The differential signal successfully eliminates the impact of the signal dc offset [Fig. 4(c)]; 4) The dc reference level should be > 0.2·$|V_m|$ to minimize magnitude measurement errors [Fig. 4(d)]; 5) Jitters in the comparator sampling clock have negligible impact on the measurement accuracy [Fig. 4(e)]; 6) The frequency deviation of the sampling clock from LCM coherent sampling has significant impact on the measurement accuracy [Fig. 4(f)]. Thus, a PLL is necessary for generating the sampling clock.

III. Circuit Design

A. EIT System Overview

The architecture of the 16-electrode EIT system is shown in Fig. 5. It comprises a signal generator (SG) ASIC and an EIT ASIC. The SG ASIC generates the input differential sine wave and the synchronized clock reference (CLK_{sync}). The EIT ASIC has a current driver, a T-D impedance readout with the proposed method and a digital control module; the latter for

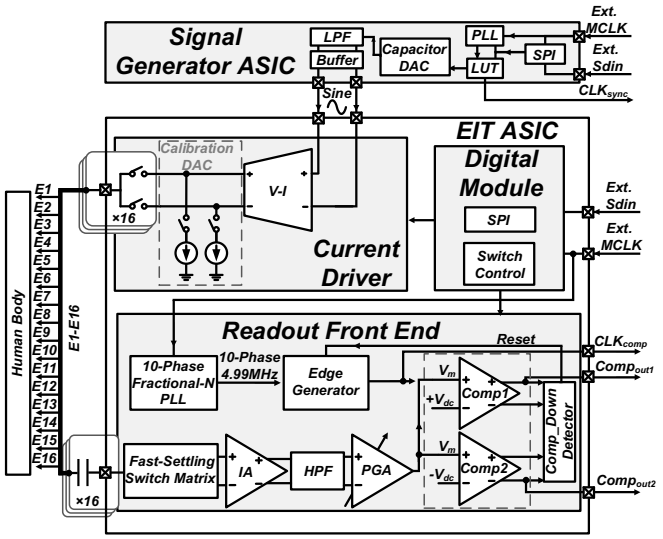


Fig. 5. Architecture of the EIT system.

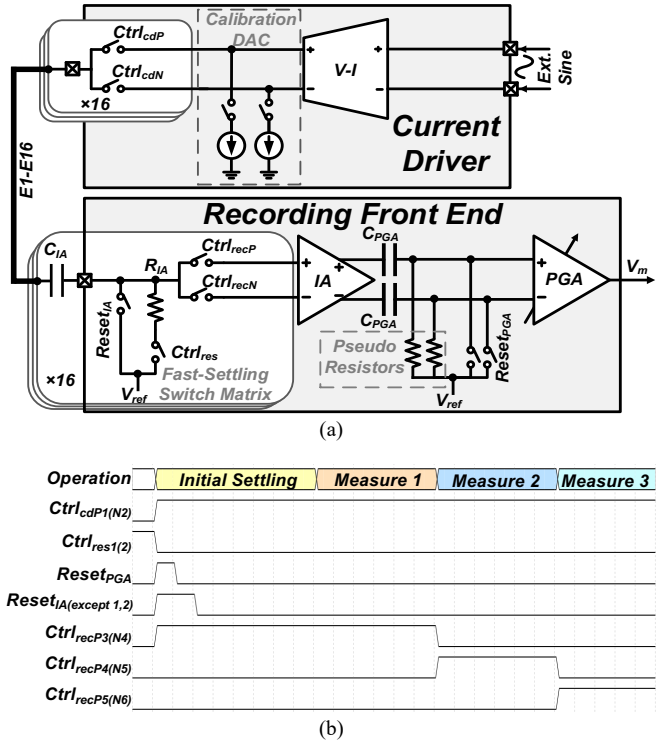


Fig. 6. (a) Simplified block of the current driver and recording front end with fast-settling switch matrix and (b) switching timing diagram.

electrode multiplexing and data communication.

In operation, the voltage-to-current converter (V-I) in the EIT ASIC transforms the differential sinusoidal voltage from the SG ASIC to current and injects it into an electrode pair via the switch matrix. The induced voltages across the remaining electrode pairs are amplified and then compared to the differential dc level. A fast-settling switch matrix, which can minimize the settling time of the high-pass filters (HPFs) during electrode switching, is used for multiplexing the single-channel impedance readout to different electrode pairs.

The output sine wave and CLK_{sync} from the SG ASIC are

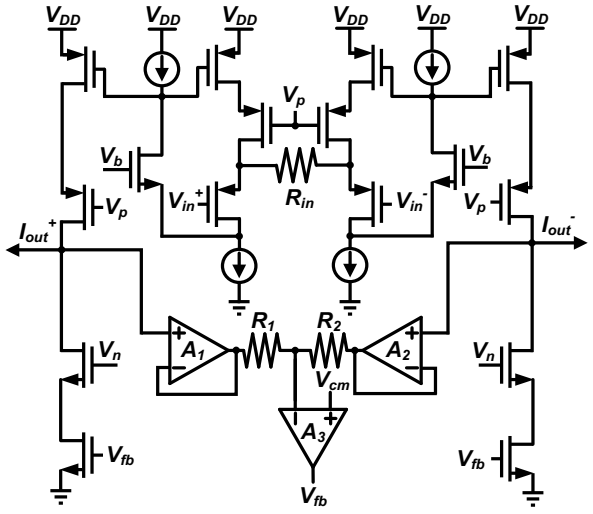


Fig. 7. Simplified schematic of the current driver.

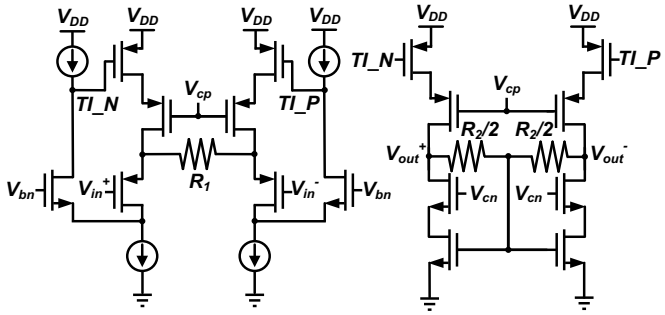


Fig. 8. Simplified schematic of the IA.

implemented by direct digital synthesis. The SG ASIC has a PLL to provide an oversampling clock, an 8-bit capacitor digital-to-analog converter (DAC) controlled by a look-up-table (LUT) for generating the pseudo sine wave and a LPF for removing the high order harmonics in the pseudo sine wave. The PLL and LUT are controlled by a serial peripheral interface (SPI) defining the frequency and magnitude of the generated sine wave. The on-chip PLL enables precise frequency control of the generated sine wave and CLK_{sync}.

For impedance digitization (T-D function), two comparators are used to detect the cross-point between the measured voltage V_m and two complementary 80 mV dc reference voltages, $\pm V_{dc}$; see Fig. 5. $V_{dc} = \pm 80$ mV is sufficient to provide > 1% magnitude measurement error for V_m signals up to 1 V_{pp} according to the simulations in Section II. To make the comparison robust to external interference, decoupling capacitors (2.4 pF) were added at the output of the PGA and at the two dc voltage references. In addition, to balance the impedances at the positive and negative input terminals of the comparators and thus ensure a similar immunity to interference, series resistors (28 kΩ) were added at the negative input terminals of the comparators. A 10-phase 4.99 MHz comparator

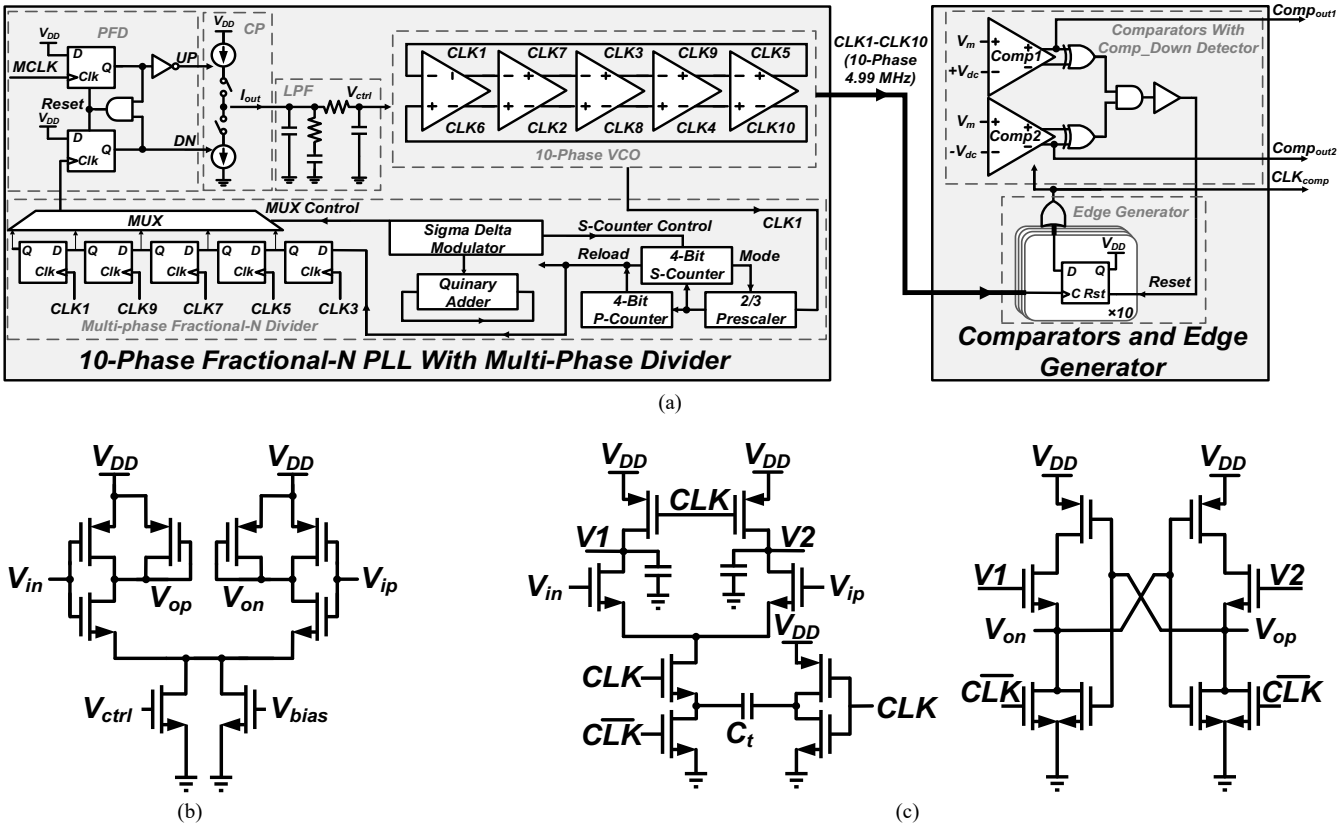


Fig. 9. Detailed schematic of (a) 10-phase PLL, edge generator and comparators, (b) VCO delay cells and (c) comparator.

sampling clock signal is generated by a fractional-N PLL with a 10-phase VCO. It achieves a constant 0.2% signal cycle phase resolution over a 10 μs measurement time by utilizing the proposed multi-phase LCM coherent sampling approach.

B. Current Driver and Recording Front End

Fig. 6(a) shows the block diagram of the current driver and recording front-end, integrated with a fast-settling switch matrix. The current driver has two calibration current DACs to remove any dc current offset at the injecting electrodes for clinical safety compliance [17]. The ac-coupled recording front end has a first-stage instrumentation amplifier (IA) and a second-stage PGA. The current driver and recording front end are multiplexed to different electrode pairs by the switch matrix.

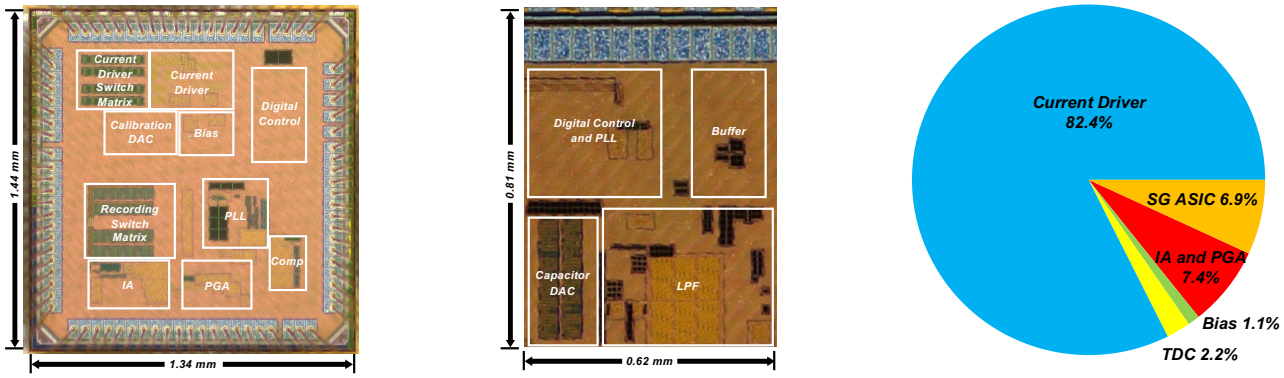
As discussed in Section II, an overall THD lower than 40 dB is suggested for the recorded voltage. The V-I converter in the current driver is based on a current feedback structure due to its superior linearity and current efficiency [18]. The simplified schematic of the current driver is shown in Fig. 7. The output current magnitude is determined by the input sinusoidal voltage and the value of the resistor R_{in}.

The schematic of the IA is shown in Fig. 8. Current feedback structure is also used in the IA due to linearity considerations and high common-mode rejection ratio [19]. Over two thirds of the power consumption of the IA is allocated to the input stage to optimize noise performance. The PGA has a gain from 2V/V to 25V/V in five steps, making it adaptive for a wide input voltage range. The PGA gain is dynamically adjusted by monitoring the output of the two comparators; this allows the system to accommodate varying voltage amplitudes measured at different electrode locations. When the output of the PGA exceeds the dc reference voltage (80 mV), the system counts the number of pulses from the output of each comparator over a measurement window. If the number of pulses is below a lower bound, the PGA gain is increased to amplify the signal. If the number of pulses is above an upper bound the PGA gain is decreased. The settled gain at each electrode location is stored and used for the subsequent frames.

C. Electrode Multiplexing with Fast Settling

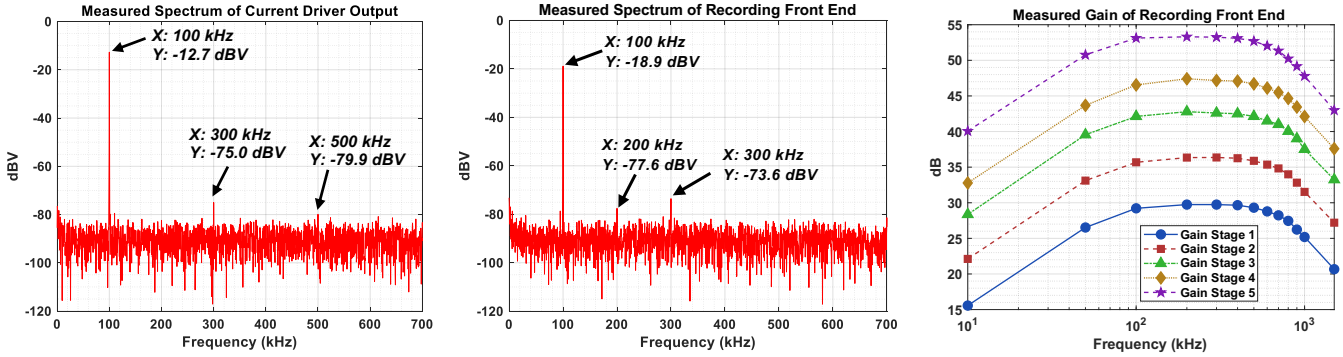
Multiplexing a single recording channel among electrodes to record each electrode voltage in series is more power efficient than parallel recording. However, as the recording electrode voltage varies with distance from the injecting electrodes, extra settling time is required for voltage recording after switching electrodes. For voltage recording, HPFs or dc-servo loops is often used to eliminate dc offset from electrodes and amplifiers, as noted in various studies [1], [3], [5], [6] [20]. When a voltage swing occurs at the input of a recording circuit, it requires time for a HPF or a servo loop to settle to a new output voltage. The duration of the settling time imposes a limit to the speed of EIT.

A fast-settling scheme was implemented in the EIT ASIC to address this limitation. Fig. 6 shows the circuit arrangement and switching sequence. The design implements 16 parallel HPFs at the electrode contacts to remove dc offset from the electrodes, and a pair of HPFs after the IA to remove its output dc offset. Each HPF has reset switches to aid settling. In Fig.



(a) (b) (c)

Fig. 10. (a) Micrograph of the EIT ASIC, (b) micrograph of the SG ASIC, and (c) power breakdown of the EIT system. The time-to-digital converter (TDC) includes the multi-phase PLL, comparators, edge generators and counters.



(a) (b) (c)

Fig. 11. Measured results of (a) FFT of the current driver output, (b) FFT of the recording front end output, and (c) gains of the recording front end.

6(a), each electrode is ac-coupled with an off-chip 100 pF capacitor, C_{IA}, followed by an on-chip resistor, R_{IA}, forming a HPF cut-off frequency of 80 kHz. After the current driver switches to a new electrode pair, for example as shown in Fig. 6(b), where the positive current output to electrode 1 (E1) via switch $Ctrl_{cdP1}$, and the negative current output to electrode 2 (E2) via $Ctrl_{cdN2}$, an initial settling period allows the C_{IA}-R_{IA} HPFs on all the other 14 electrodes to settle. The default length of this initial settling period is 16 µs but is programmable. During this period, R_{IA} is connected to a dc reference voltage, V_{ref}, via switch $Ctrl_{res}$. The output of each first-stage HPF is forced to V_{ref} via switch $Reset_{IA}$ at the beginning of the initial settling period to aid settling. After the initial settling period, the dc level at the output of all the HPFs is at V_{ref}. The IA then cycles through the HPFs via the switch pair $Ctrl_{recP}$ and $Ctrl_{recN}$ in each fast-settling switch matrix for voltage measurement. The switches in the switch matrix for the two injecting electrodes remain off to isolate them from the recording channel. Such switching does not affect the settled voltage in each first-stage HPF provided the value of C_{IA} is much larger than the parasitic capacitance at the input nodes of the IA.

The output of each second-stage HPF (after the IA) is also forced to V_{ref} via $Reset_{PGA}$ at the start of the initial settling period. $Reset_{PGA}$ turns off before $Reset_{IA}$ to ensure the voltage at both ends of C_{PGA} is at V_{ref} when voltage measurement starts. Each second-stage HPF is built with a pseudo resistor of 50 MΩ for a cut-off frequency below 1 kHz, resulting in a much larger time constant, and thus much longer settling time compared with the first-stage HPFs. As a result, the transient ripples at the IA output during the initial settling period have very little impact on the output dc voltage level of the second-stage HPFs, because the charge and discharge of the second-stage HPFs caused by these short-time ripples are negligible due to the much larger time constant. With this arrangement, the settling time required by the switching of the recording electrode pairs after the initial settling period is limited only by the slew-rate of the IA and PGA, thus providing a much quicker response compared to traditional methods.

All the switches are controlled by the on-chip control logic, which also controls the electrode switching pattern for injection and recording based on commands sent via SPI. By utilizing the fast-settling scheme, the voltages at all 14 recording electrodes are settled in parallel during the initial settling period, thus yielding a much faster EIT frame rate than conventional serial recording EIT systems. Since the HPFs are passive, this arrangement has significantly less power consumption than conventional parallel recording.

D. Multi-Phase PLL and Comparators With Edge Generator

The schematic of the multi-phase PLL and comparators with edge generator is shown in Fig. 9. As discussed in Section II, the sampling clock of the comparators is generated by a fractional-N PLL with a ring VCO, providing a high accuracy and power efficient 10-phase, 4.99 MHz clock signal. The PLL has a 10-phase ring VCO, a multi-phase fractional-N divider, a phase frequency detector (PFD), a charge pump (CP) and a LPF. The VCO has 5-stage differential delay cells to provide the required

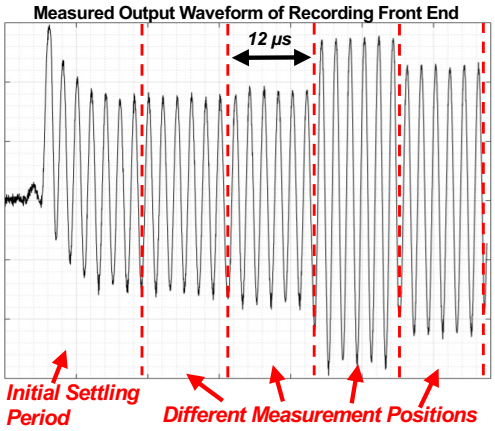


Fig. 12. Measured output waveform of the recording front end with fast-settling switch matrix.

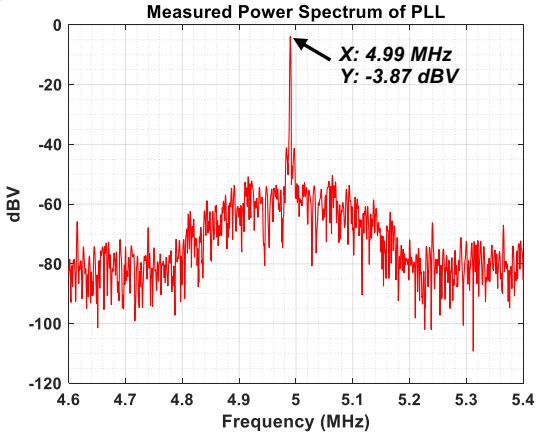
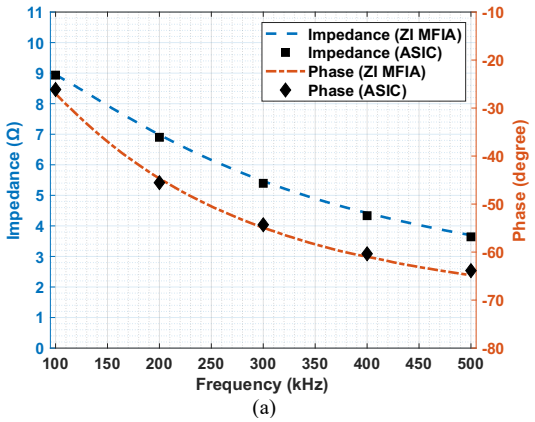


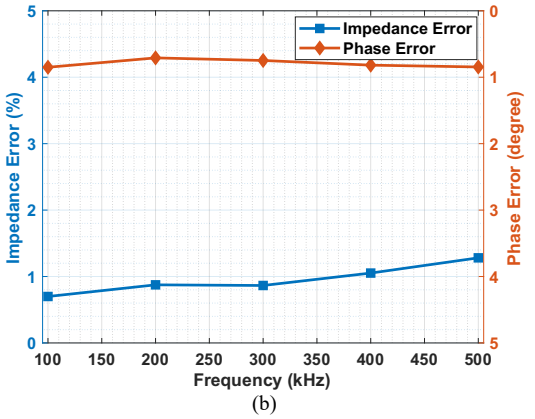
Fig. 13. Measured power spectrum of PLL output.

TABLE II
PERFORMANCE SUMMARY

Technology	65 nm CMOS	
Die Size	EIT ASIC	1.44 mm × 1.34 mm
	SG ASIC	0.81 mm × 0.62 mm
Total Power Consumption	1.76 mW	
Frame Rate	355 fps	
EIT ASIC		
Current Driver	Supply	1.8 V
	Power Consumption	1.45 mW
	Output Current	600 μA_{pp}
	THD	<-61 dBc
	Output Impedance	>1 MΩ at 500 kHz
Impedance Readout	Supply	1 V
	Power Consumption	172 μW
	Input Referred Noise	6.1 μV_{rms} (dc–2 MHz)
	Readout Method	T-D
	Comparator Frequency	10-Phase 4.99 MHz
	Gain	29.7 dB – 50.3 dB
	THD	<-53 dBc
	Frequency Range	100 kHz – 500 kHz
SG ASIC		
Supply	1 V	
Power Consumption	121 μW	
Maximum PLL Frequency	64 MHz	



(a)

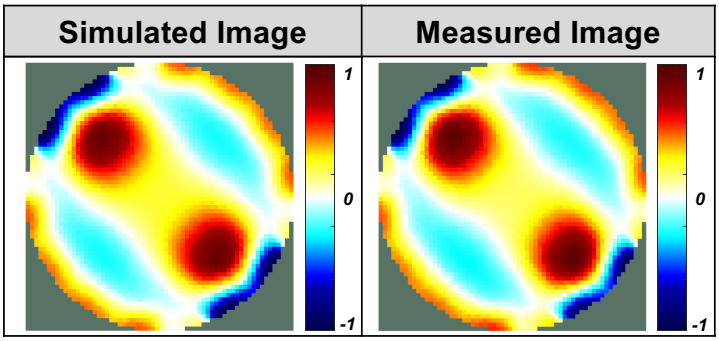


(b)

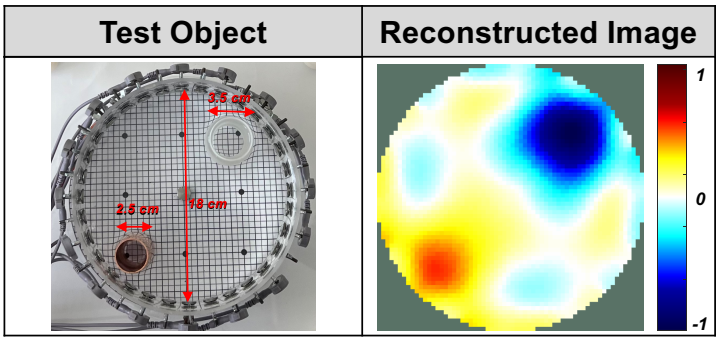
Fig. 14. (a) Comparison of impedance measurements with the EIT ASIC and ZI MFIA using a 10 Ω//80 nF load, and (b) impedance and phase measurement errors.

10-phase signal of as shown in Fig. 9(b). In the fractional-N PLL, the output frequency of the VCO is locked at a pre-defined value determined by the fractional-N divider and the input reference clock *MCLK*. During operation, the output clock signal of the VCO is divided by a programmable divider. The divided signal is compared with *MCLK* by a PFD to control the CP when charging and discharging the control voltage of the VCO, V_{ctrl}. The fractional dividing ratio is achieved by changing the dividing ratio of the divider between each cycle and averaging them. The LPF between the CP and VCO helps to remove the high frequency ripples due to the averaging process. To further reduce the frequency ripples and the required averaging cycles for generating the 4.99 MHz frequency, a multi-phase fractional-N divider is used. It has a coarse division stage with a P/S counter and a 2/3 prescaler, and a fine division stage with a 5-phase delay chain and a multiplexer. A third-order MASH Sigma-Delta modulator and a quinary adder are used to control both division stages. This architecture utilizes the intrinsic phase delay of the multi-phase phase clock, where the divided signal after the prescaler and P/S counter is further processed by the 5-phase delay, providing an extra fractional dividing ratio of 0.2, 0.4, 0.6 and 0.8 without averaging [21]. This method significantly reduces both the averaging cycles required for generating the required 4.99 MHz signal and the high frequency ripples. It also relaxes the cut-off frequency requirement of the LPF.

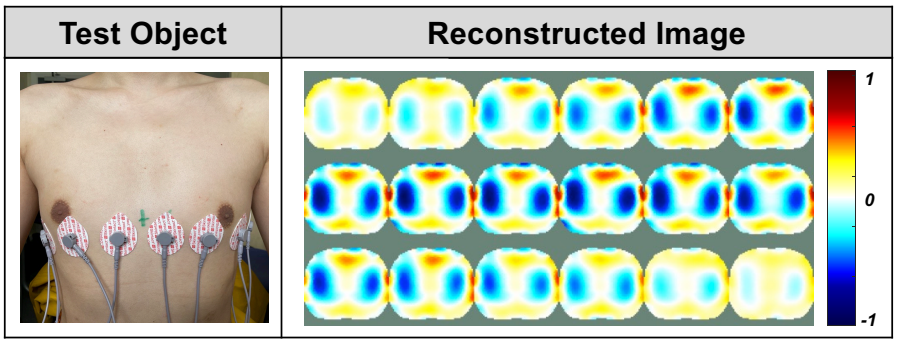
The comparators for cross-point detection should be fast and accurate to reduce errors during comparison and have low power consumption. A two-stage dynamic comparator with a dynamic



(a)



(b)



(c)

Fig. 15. (a) Reconstructed images of resistive phantom with simulated data and measured data, (b) in-vitro reconstructed image of a water tank with copper and nylon bars, and (c) in-vivo reconstructed image of air volume change during an entire deep respiratory cycle.

pre-amplification stage and a dynamic latch was used [22]. The schematic is shown in Fig. 9(c). The pre-amplification stage decreases the input referred noise and kickback noise. The tail capacitor C_t operates as a charge pump, which can pull down the source voltage of the input pairs to $-V_{DD}$. This significantly increases the comparison speed to sub-ns. According to simulations, the comparator has an input referred noise of 270 μV_{rms} and 600 ps comparison speed (common-mode input voltage at the middle of the supply).

The comparators are initiated when the 10 DFFs in the edge generator are triggered by the 10-phase clock generated by the PLL. After comparison, a *Reset* signal [Fig. 9(a)] is generated that resets the DFFs in the edge generator and in turn the comparators. The rising edge triggering and self-reset logic interpolates the 10-phase clock signals with minimum cost, thus simplifying the design complexity and reducing power consumption. During operation, an SR latch implemented at the output of each comparator generates a pulse between T_1 and T_2 in Fig. 2, and the clock pulses during pulse N_1 are counted by a counter. The same method is used for counting the value of N_0 between T_s and T_1.

IV. Measured Results

A. Chip Overview

The EIT ASIC and the SG ASIC were fabricated in a 65-nm CMOS process and occupy a die area of 1.9 mm^2 and 0.5 mm^2, respectively. Their micrographs are shown in Figs 10(a) and (b). The two ASICs have a total power consumption of 1.76 mW. The current driver has a maximum output current amplitude of 700 μA_{pp} with 1.45 mW total power consumption from a 1.8 V supply. The readout front end and the SG ASIC consume 172 µW and 121 µW respectively from a 1 V supply. The detailed power breakdown is shown in Fig. 10(c).

The measured spectrum of the current driver output is shown in Fig. 11(a). The current driver has a THD of <-61 dBc and an output impedance of >1 MΩ at 500 kHz. For the THD

TABLE III
COMPARISON WITH PRIOR WORK

	JSSC'15[27]	ISSCC'17[2]	TBioCAS'19[3]	ISSCC'19[4]	SSCL'23[14]	This Work
Application	Lung Ventilation	Lung Ventilation	Lung Ventilation	Lung Ventilation	Peripheral Nerve	Lung Ventilation
Readout Method	Analog I/Q	Analog I/Q	Digital I/Q	Analog I/Q	SC	T-D
Technology (nm)	180	65	350	130	180	65
Supply (V)	1.8	1.2	±9	1.0	1.8	1.0 and 1.8
Power Consumption (mW)	10.4	6.96	250/Channel[a]	1.53	4.84	1.76
Max. Injection Current (μA_{pp})	1000	1000	6000	200	50	700
Number of Electrodes	32	48	16	16	16	16
Bandwidth (kHz)	10–200	10–256	45–1000	15.625–125	1–18	100–500
SNR (dB)	56.3	N/A	54.3	N/A	N/A	52.6
Max. Frame Rate (fps)	20	70	122	5	312[b]	**355**
Power Consumption of Readout Front End[c] (μW)	N/A	2362[a]	N/A	994	1373	**172**
Energy of Readout Front End per Frame (μJ)	N/A	33.74	N/A	198.80	4.40	**0.48**
FoM[d] ($\frac{\text{Frame}}{\text{s}\cdot\mu\text{W}}$)	N/A	1.42	N/A	0.08	3.64	**33.02**

[a] The power consumption of analog-to-digital converter is not included.
[b] With continuously updated baseline cancellation.
[c] Including the power consumption for signal conditioning and digitization.
[d] FoM = (Frame Rate × Number of Electodes)/Power Consumption of Readout Front End.

measurement of the recording front end, a 10 Ω resistive load was connected to the current driver output and the input of the recording front end. The measured spectrum is shown in Fig. 11(b). The recording front end has a THD <-53 dBc, which is sufficient for accurate impedance measurement according to the simulations in Section II. The measured gain is from 29.7 dB to 50.3 dB in five steps, shown in Fig. 11(c). The dc to 2 MHz input referred noise is 6.1 μV_{rms}.

Fig. 12 shows the measured output waveform of the recording front end with the fast-settling switch matrix. It has <0.5 μs settling time after the initial settling period. With 12 μs for each impedance measurement (2 μs margin and 10 μs measurement window) and 20 μs time margin for the initial settling period, the EIT ASIC achieves a constant frame rate of 355 fps and a temporal resolution of 0.2 signal cycle at current injection frequencies of 100 kHz, 200 kHz, 300 kHz, 400 kHz or 500 kHz. The measured power spectrum of the PLL output is shown in Fig. 13. Its output frequency is accurately locked at 4.99 MHz. Table II summarizes the performance of the EIT system.

B. Magnitude and Phase

A parallel RC model of 10 Ω and 80 nF for the neonatal thorax [23]-[24] was used to evaluate the accuracy of the EIT ASIC. Impedance measurements were taken at 100 kHz, 200 kHz, 300 kHz, 400 kHz and 500 kHz with a 600 μA_{pp} drive current. A 10 Ω film resistor load was used to calibrate the intrinsic phase shift of the EIT system before a measurement. The magnitude and phase results from the EIT ASIC were compared to those using a Zurich Instruments MFIA Impedance Analyzer (ZI MFIA; Zurich Instruments AG, Switzerland) when measuring the same load. The comparison is shown in Fig. 14(a). The detailed impedance and phase measurement errors are shown in Fig. 14(b). Over the frequency range of 100 kHz to 500kHz the average impedance and phase measurement errors of the EIT system compared with the ZI MFIA are 0.94% and 0.81° respectively.

C. In-Vitro and In-vivo Image Reconstruction

EIDORS open-source software with the Gauss-Newton algorithm [25] was used for image reconstruction. The measured absolute magnitude data was used as the input to the software. The EIT system used a 500 kHz, 600 μA_{pp} drive current. In the reconstructed image, a color map from red to blue is used to represent the different impedances, where the conductance increases when the color changes from blue to red. The reconstructed images are shown in Fig. 15. Fig. 15(a) shows images reconstructed from simulated results using an ideal resistive phantom (left) and measured results with an identical resistive phantom implementation (right). The quality of the measured image was quantified by the difference from the simulated image at each pixel using the method (FoM_{FR}) proposed in [26]. The measured image has a global full reference (FR) SNR of 14.7 and a region of interest FR SNR of 0.8. The calculated FoM_{FR} is 0.14 $\frac{\text{nW}\cdot\text{s}}{\text{Hz}\cdot\text{frames}}$, which shows a significant improvement compared to the FoM_{FR} of 670 $\frac{\text{nW}\cdot\text{s}}{\text{Hz}\cdot\text{frames}}$ of the EIT system in [26].

To evaluate the SNR of the EIT ASIC alone, the method in [27] was used. More than 300 data frames were measured with the resistive phantom under the same condition. The average SNR over the 300 data frames is 52.6 dB.

For in-vitro testing, an 18 cm water tank filled with 0.5 S/m saline solution containing 2.5 cm copper and 3.5 cm nylon cylinders was measured. The setup and reconstructed image are shown in Fig. 15(b). The reconstructed image clearly shows the two objects.

For in-vivo measurement, 16 Ag/AgCl electrodes were attached to the thorax of a male adult volunteer[1] to measure the impedance variation during breathing. The setup and

[1] Middlesex University London, Ethics application number 15553, 14 March 2024.

reconstructed images of an entire deep respiratory cycle are presented in Fig. 15 (c). The reconstructed images show the regional air volume changes during breathing.

V. Conclusion

An EIT system for neonate lung monitoring has been developed. By utilizing a multi-phase VCO based time-to-digital impedance readout method and a fast-settling switch matrix, the EIT system achieves 355 fps frame rate at 1.76 mW total power consumption. The readout front end for signal conditioning and impedance digitization consumes only 172 μW. Table III provides a comparison with other work. The EIT system in this work achieves 83%-93% power reduction for the readout front end and 1.14-71 times frame rate increase. A figure of merit (FoM) for the readout front end that considers the frame rate, power consumption and number of electrodes is proposed. The EIT system in this work achieves 9.1 times higher FoM compared with prior work.

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