Dielectric breakdown of oxide films in electronic devices

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Abstract

Dielectric breakdown is a sudden and catastrophic increase in the conductivity of an insulator caused by electrical stress. It is one of the major reliability issues in electronic devices employing insulating films as gate insulators and energy and memory capacitors. In spite of extensive studies, our understanding of underlying physical mechanisms driving the breakdown process and atomistic models of dielectric breakdown remain controversial. This Review provides a historic and synoptic overview of the enormous amount of data and knowledge accumulated on experimental and theoretical studies of dielectric breakdown in different insulating materials focusing on describing phenomenological models and novel computational approaches.

Keywords: Dielectric Breakdown, Dielectrics, Insulating Materials, Electronic Devices, Mechanisms

1 Introduction

Dielectric breakdown (DB) occurs in all insulating materials – gases, liquids or solids, when the electric field caused by an applied voltage exceeds the material's dielectric strength. This fascinating phenomenon refers to the sudden and catastrophic increase in the conductivity of an insulator and its mechanisms have been the subject of modern theories for more than 100 years (see e.g. refs. [1–4]). It is one of the most important reliability and performance issues in Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) [5–7], semiconductor memories [8, 9], dielectric high-energy density capacitors [10, 11] (also using multi-layer ceramics [12] and polymers [13]), piezoeletric actuators [14], and microwave devices [15]. Dielectric breakdown has been studied even in cell membranes [16]. When this phenomenon occurs in the gate oxide(s) of a transistor, it causes a short that compromises device/circuit functionality. Due to the critical importance of DB for the reliability of microelectronic devices, the behaviour of oxides traditionally used in these devices (SiO_2, HfO_2, Al_2O_3) is better understood and will be the main focus of this review. However, the knowledge and models created in this area may be useful in many other applications including electroceramics for next-generation energy-storage capacitors and solid state electrochemistry [17].

In spite of extensive research efforts by industry and academia over more than 60 years, the physical mechanisms driving the breakdown processes are not fully understood and their complexity has increased along with that of the transistor and the integrated circuit. The continuous adoption of new materials [18] and 3D and more complex device architectures [19], driven by technology scaling, further complicates our understanding. Accurate, physics-based breakdown models are vital both for design and manufacture of new devices, and correct projections of device lifetimes. In the field of semiconductor devices, the time-dependent dielectric breakdown (TDDB) testing is typically done under field- and/or temperature-accelerated conditions and reliable models are paramount for extrapolating characterization results to real operating conditions. Understanding and improving the performance of these devices requires considering the interplay between electronic and ionic processes at electrodes, interfaces, and inside the solid electrolyte at different pressures, temperatures, and cycle numbers. This is essentially a material problem, and elucidating how device characteristics are linked to the material's properties requires multidisciplinary approaches.

The complex process of material degradation under bias involves a range of electronic and ionic reactions that unfold inside and at the interfaces of disordered nanoscale films of several materials comprising modern devices. At the electrical level, this complex interplay of competing physical phenomena manifests itself as a current evolution over time for the device stressed at time $t = 0$ (the leakage current is one of the main metrics used to characterize material degradation and breakdown, as discussed in Section 3). Details and specific features observed in current evolution ultimately depend on the properties of device and materials under consideration. A classic example is the rather different behaviour observed in thick and thin MOSFET gate oxides under electrical stress, despite the underlying physics of degradation is the same. Thick oxide films show an initial decrease of the current followed by an abrupt increase corresponding to hard breakdown (HBD) (see **Figure 6a**), while

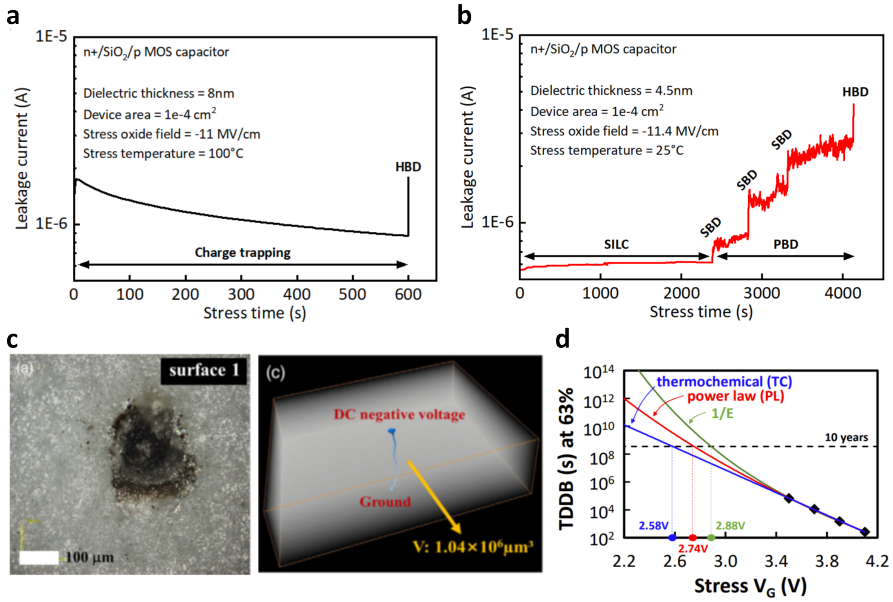


Fig. 1 Fundamentals of the dielectric breakdown process. a— The I-t trace resulting from a thick dielectric layer under CVS exhibit a current decreasing in time due to charge trapping and an abrupt HBD [20]. b— The I-t trace resulting from a thin dielectric layer under CVS exhibit an initial SILC phase, followed by a PBD phase comprising a sequence of SBD and a final HBD [20]. c— Physical damage in dielectric zirconia-toughened alumina (ZTA) after HBD: TEM imaging of the surface (left) shows a crater-like feature at the breakdown spot, while the micro-CT imaging (right) reveals a columnar structure connecting the two sides of the sample (bottom) [21]. d— TDDB projections of different models (E model, 1/E model, and power-law E model) extrapolated from high-voltage measurements highlight a significant reliability difference between the models [22].

the thin films exhibit a much more complex behavior (see **Figure 6b**), in which a stress-induced leakage current (SILC) is initially observed, followed by a progressive breakdown stage (PBD) consisting of several soft breakdowns (SBD) and ending with a HBD [20]. There is a fairly general consensus that a leakage current observed in the first stages is caused by the generation of individual defects (often called traps) inside different oxides. Further differences are observed in materials in which mechanisms other than defect generation play an important role, such as ionic diffusion in low-k dielectrics. The kinetics of degradation and breakdown depend also on the film morphology and are different for polycrystalline and amorphous films [23]. It is assumed that initial defect generation in amorphous films occurs at random positions, while in polycrystalline films there is defect segregation at grain boundaries. The nature of these defects and mechanisms of their creation are still debated and are discussed in more detail below. Nevertheless, the final steep increase of the current at the HBD stage is a universal feature observed in all devices and materials under electrical stress. This HBD stage manifests itself as a significant oxide damage that can be visualized with imaging techniques, see **Figure 6c**.

The results of experimental characterization of metal-insulator-semiconductor (MIS) or metal-insulator-metal (MIM) stacks are usually rationalized using theoretical models developed over the years. Most phenomenological models can be classified according to the dependence of the probability of forming a critical defect concentration as a function of applied electric field **E**. Among the proposed models, those based on the thermochemical (TC) bond-breaking (**E** model) [24–26], the 1/**E** [27, 28], and the power-law **E** model [29, 30] are the most widely adopted, as discussed in detail in Section 4. When applied to the experimental data for the accelerated TDDB tests, these models give very different lifetime extrapolations (see **Figure 6d**) highlighting the importance of a better understanding. More recent models [31, 32] emphasize the importance of the structural and electronic properties of a material in determining the character of TDDB voltage dependence.

In this Review, we discuss the current and emerging research trends in this interdisciplinary field and new physical perspectives on the dielectric breakdown. In the next section, we briefly overview the dielectric materials used in devices and the DB properties that are the focus of this perspective. In Section 3 we discuss the methods used and the results of experimental characterization of materials and TDDB. In Section 4 we provide a broad overview of phenomenological breakdown models proposed in the literature, and in Section 5 we discuss recent atomistic models of DB in traditional wide bandgap oxides. A short overview of degradation and breakdown in other oxides is given in Section 6 and the summary and perspective are provided in Section 7.

2 Dielectric materials

The main dielectrics used (or investigated) in the most relevant semiconductor devices (transistors and memories) are summarized in **Table 2**. From the 1960s, research on DB or time-dependent DB (TDDB) has focused mainly on SiO_2 because the unique properties of this dielectric and its interfaces with Si made it a primary gate insulator in front-end-of-line (FEOL) applications in the semiconductor industry [33]. However, drastic dimension scaling for higher performance and the resulting decrease in thickness of SiO_2 layers led to diminishing reliability margins due to electron tunneling through the oxide layer.

To further enhance chip performance in advanced nodes, new insulator materials, such as the so-called high-k (high dielectric constant) stacks (HfO_2/SiO_2) and low-k dielectrics (lower dielectric constant with respect to SiO_2) (e.g. SiOCH) [103, 105], as well as new spacer materials (SiBCN and SiOCN) [104] relative to Si_3N_4, have been introduced or considered in FEOL, back-end-of-line (BEOL), and middle-of-line (MOL) contexts, respectively. It is important to note that DB does not only concern MOSFETs, but also any other device or part of an integrated circuit (IC) comprising insulating oxides. Although degradation dynamics and breakdown physics are general, differences related to both the application and the materials are usually observed. In Dynamic Random Access Memory (DRAM) technology (see **Box 1**), continuous scaling and the demand for high capacitance density have led to the adoption of

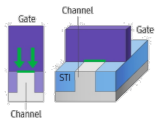
Table 1 List of the main dielectric materials used in the most relevant semiconductor devices and their main applications. V_{TH} tuning refers to the use of oxides (mostly TMOs) to control the threshold voltage (V_{TH}) of a transistor (see e.g. [64]). A synthetic description of each device is reported in **Box 1**.

Dielectric materials used in the most relevant semiconductor devices			
Device	Application	Materials	Specific Features
Planar MOSFET	Gate Dielectric V_{TH} tuning	SiO_2; SiON [34–37]; Si_3N_4 [38]; Ta_2O_5 [39–41]; TiO_2 [42]; Al_2O_3 [43]; La_2O_3 [44], [45]; CaF_2 [46]; CeO_2 [47, 48]; HfO_2 [49–51]; ZrO_2 [49, 52]; $SrTiO_3$ [44, 53, 54]; Gd_2O_3 [55, 56]; Y_2O_3 [44, 56, 57]; Pr_2O_3 [58]; Er_2O_3 [59]; Nd_2O_3 [60]	
FinFET	Gate Dielectric V_{TH} tuning	SiO_2; HfO_2 [49–51]; Al_2O_3 [61]; La_2O_3 [62–64]; MgO [64]; Y_2O_3 [62, 64]	3D structure
GAA Nanosheet	Gate Dielectric V_{TH} tuning	SiO_2; HfO_2 [49–51]; Al_2O_3 [61]; La_2O_3 [62–64]; MgO [64]; Y_2O_3 [62, 64]	3D structure, conformality
2D Transistors	Gate Dielectric	CaF_2 [65]; MgO [66]; hBN [65]	
DRAM	Capacitor	Si_3N_4 [67]; Ta_2O_5 [40, 68, 69]; TiO_2 [70–72]; Al_2O_3 [73]; La_2O_3 [74]; HfO_2 [75]; ZrO_2 [76, 77]; $SrTiO_3$ [78]; Y_2O_3 [79]	3D structure, very thin multilayer stack
3D-NAND	Tunnel layer(s) Storage layer	SiO_2; Si_3N_4 [80, 81]; Al_2O_3 [81]; HfO_2 [82]	3D structure (cylindrical)
Magnetic RAM	Tunnel barrier	MgO [83]	Complex multilayer stack
Power transistors	Gate dielectric	SiO_2 [84]; Si_3N_4 [84]; high-k materials [84]	
RRAM	Switching dielectric	SiO_2 [85, 86]; Ta_2O_5 [87–89]; TiO_2 [88–91]; Al_2O_3 [88–90]; HfO_2 [88, 89]; SiCOH [92]; MgO [93]; hBN [94]	
Ferroelectrics	FE layer	HfO_2 [77, 95]; ZrO_2 [77]	Polarization Switching
BEOL	Capacitor	Si_3N_4 [96, 97]; Al_2O_3 [97]; HfO_2 [97]	
	MIIM diode	Ta_2O_5 [98]; TiO_2 [99]; Al_2O_3 [100]; HfO_2 [101]; Nb_2O_3 [102]	
	low-k	SiOF [103, 104]; SiCOH [103, 104]	Cu contamination, line edge roughness (LER)

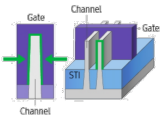
complex 3D geometries and physically thin multi-layer high-k dielectric stacks [106–109]. Breakdown in DRAMs devices thus shares similar characteristics with those of modern 3D transistors.

In power transistors, the major difference from logic devices is the use of wide bandgap semiconductor channels, namely AlGaN/GaN and SiC, and quite thick oxides [84], see **Box 1**. Despite the huge progress made in recent years, GaN and SiC still form quite defective interfaces with dielectrics [84], which affects overall device reliability

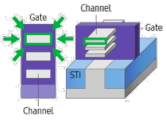
Box 1 – Semiconductor Devices



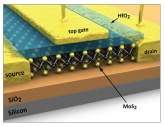
The **planar MOSFET** transistor features a flat structure with three main layers: a metal gate, a thin insulating dielectric stack, and a semiconductor. It controls the current flow between source and drain terminals by applying voltage to the gate and drain terminals. Figure adapted with permission from [110].



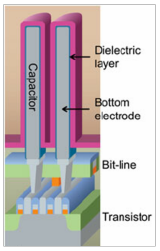
The **FinFET** is an advanced transistor featuring a three-dimensional structure where the insulating dielectric stack is wrapped around a thin vertical "fin" of semiconductor material, providing better control over the current flow. Figure adapted with permission from [110].



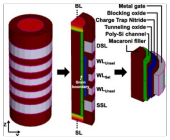
The **nanosheet** transistor is a cutting-edge technology designed to improve upon FinFET transistor. It features a multi-layered structure, where several thin horizontal layers, or "nanosheets," of semiconductor material, surrounded by the gate dielectric stack, are stacked on top of each other. Figure adapted with permission from [110].



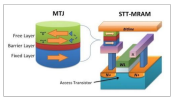
2D transistors exploit two-dimensional materials, such as graphene or transition metal dichalcogenides, to further improve electrical properties. Being in its early development phases the technology has several integration challenges, including the identification of the proper gate dielectric material. Figure reproduced with permission from [111].



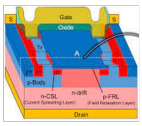
DRAM (Dynamic Random Access Memory) is a type of volatile memory that stores binary data in capacitors. The data stored in the capacitor is read and written by using a dedicated access transistor. Modern state-of-the-art 3D DRAM technologies feature cylindrical-like capacitors, made of a very thin multi-layer dielectric stack, that are vertically stacked on their access transistors. Figure reproduced with permission from [112].



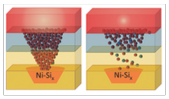
3D NAND technology represents state-of-the-art non-volatile Flash memories widely used in storage devices like solid-state drives (SSDs). Individual memory cells are stacked vertically up to 321 layers (and counting). Each cell (either charge trapping or floating gate) comprises multiple dielectric layers wrapped around a semiconductor channel in a cylindrical structure. Figure reproduced with permission from [113].



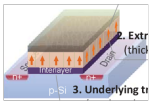
Magnetic RAM (MRAM) is a non-volatile memory device that utilizes the magnetic properties of materials to store and read information bit. Most common technology implementations rely on a magnetic tunnel junction (MTJ) comprising a very thin MgO dielectric. Figure reproduced with permission from [114].



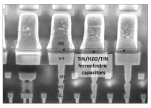
Power Transistors are semiconductor devices designed to handle and control large amounts of electrical power in electronic circuits. They exploit standard dielectrics on silicon and wide band-gap semiconductor substrates such as SiC and GaN and AlGaN. Figure adapted with permission from [115].



Resistive RAMs (RRAM) are non-volatile memories in which the information bit is stored by changing device resistance. In the common Transition Metal Oxides (TMO)-based RRAM technology, device operation relies on a controlled breakdown of one or more dielectrics. Figure adapted with permission from [116].



Ferroelectric transistors, **FeFETs**, and memories, **FeRAM**, exploit the unique properties of ferroelectric materials. These are dielectrics with an electric polarization that can be switched and reversed by an external electric field. Figure adapted with permission from [117].



BEOL devices refer to components and structures that are fabricated in the latter stages of the fabrication process, after the creation of transistors and other active components (FEOL). They comprise a variety of dielectrics mainly used in MIM capacitor structures. Figure reproduced with permission from [118].

[119, 120]. Nevertheless, breakdown and degradation have been reported to behave similarly to Si-based MOSFETs, with consistent statistical behavior [119, 121, 122] and identifiable SILC and SBD/PBD phases [121]. Extrinsic early failures due to contamination and oxide defects represent an additional problem [123, 124] that is expected to be solved by improving the oxide growth process [123].

In addition to semiconductor devices, the DB phenomenon is extremely relevant for BEOL interconnect architectures, where low-k dielectrics (such as SiCOH) and copper are used to reduce parasitic resistance and capacitance of the interconnect network [103]. The adoption of these materials strongly affected the reliability of the interconnect structure. The quality of SiCOH dielectrics is much lower than that of SiO_2 with a significant amount of carbon and hydrogen-related traps [125–127]. On the other hand, degradation often involves metal ion migration [128] from the Cu metal line [129], or from the Ta-based barrier included to prevent it [130]. Finally, BEOL interconnect structures are typically affected by Line Edge Roughness (LER)

issues [131]. As a consequence of these additional phenomena, the breakdown of low-k dielectrics often exhibits rather different trends with respect to standard SiO_2 and high-k dielectrics, especially with regard to its voltage dependence [125, 132, 133]. This led to the development of new BD models (or to the revision of existing ones) [134], as discussed in Section 4.

In memory applications (see **Box 1**), dielectric degradation has historically been considered much more relevant than DB. This is especially true in Flash devices, where SILC can seriously compromise their retention and endurance characteristics and lead to device failure well before the breakdown event [135]. Therefore, only a few papers dealt with DB in Flash memories (see for example [136]). On the other hand, DB of new insulators, such as MgO, in magnetic random access memory (MRAM) technology is currently being intensively investigated [83, 137, 138]. Another class of memory devices exploits the fact that, although DB is an irreversible catastrophic event, it is preceded by a more gradual and reversible degradation of a dielectric accompanied by a decrease in its resistivity shown in **Figure 6b**. Many thin oxide films in metal–insulator–metal (MIM) or metal-oxide-semiconductor (MOS) structures show reversible resistive switching (RS) effects. This phenomenon is exploited by most resistive memory (ReRAM) devices that operate by the alternate creation and partial destruction of a conductive filament. In these filamentary ReRAM structures, DB does not cause failure, since it is intrinsic to device operation and data storage. Resistive switching-based memory devices explore a wider range of amorphous and polycrystalline oxides, such as TiO_2, Ta_2O_5, $SrTiO_3$, VO_2 and others [139] and use similar processes to reversibly change their resistivity.

In the burgeoning field of energy storage in dielectrics, lead-based (e.g. PZT, PZLT) and lead-free ceramics (such as titanate and niobate perovskites), ceramic multilayers and ceramic and polymer films play the major roles [10, 12, 13]. The breakdown strength of these devices is often determined by their structure (e.g. core-shell), morphology (such as pores, voids, microcracks, grain boundaries), as well as intrinsic defects (oxygen vacancies, impurities) [11].

Finally, we note that novel 2D materials-based devices have a similar problem of integration with dielectrics and degradation of these dielectrics during device operation. A wide bandgap 2D hBN is currently widely used in 2D nanodevices employing graphene and 2D transition metal dichalcogenides. However, its low dielectric constant and defective films cause reliability issues. This brings into consideration new dielectric films, such as cubic CaF_2 [46], MgF_2 and others [65] with better dielectric and reliability properties [140].

3 Experimental Characterisation

Our understanding of the mechanisms of degradation and DB is based on experimental evidence collected over the past 60 years, as reviewed in [6, 7, 23, 141] and briefly outlined in this section.

Electrical characterization is the primary source of real-time and *post mortem* characterization of the oxide degradation processes, providing information on their dynamics and consequences. The most common technique used in microelectronics

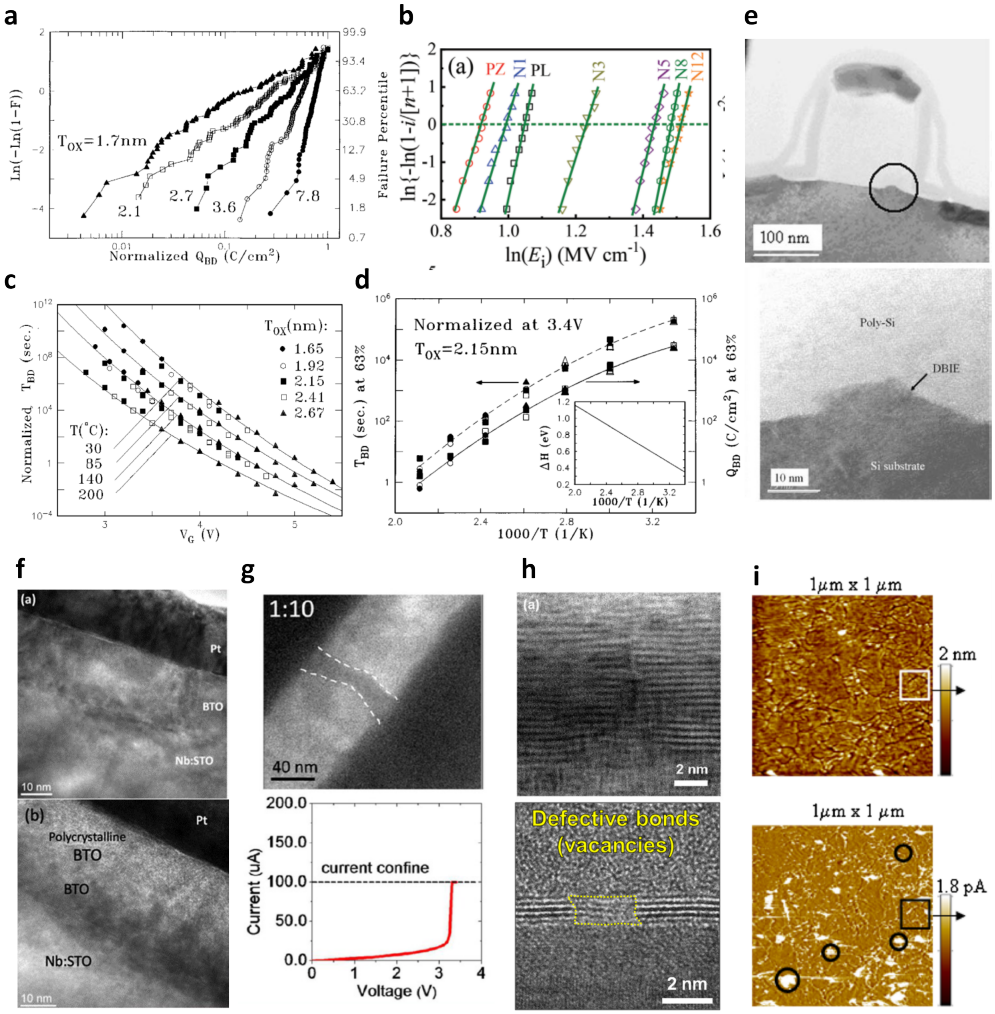


Fig. 2 Electrical and structural characterization of the dielectric breakdown process. a— The t_{BD}/q_{BD} associated to the HBD condition are stochastic variables that follow a Weibull distribution. The exhibited thickness dependence of the shape parameter beta suggests a percolative nature of the dielectric degradation process [142]. b— The V_{BD} and the related dielectric strength are also Weibull-distributed stochastic variables [143]. c— The t_{BD}/q_{BD} exhibit a complex voltage-dependence, with a significant deviation at low-field with respect to the exponential trend that can be extracted at high-field [144] d— The t_{BD}/q_{BD} also exhibit a complex temperature-dependence, revealing a non-Arrhenius trend over large temperature ranges [30]. e— TEM image of a Si/SiO_2 transistor after HBD, showing the DBIE of silicon from the substrate into the oxide [145]. f— TEM image of a Pt/BTO/Nb:STO heterostructure before (top) and after (bottom) the HBD, showing the formation of a polycrystalline BTO region, not present in the pristine device [146]. g— TEM image of a conductive filament formed in a Pt/ZnO/Pt MIM after stress (top). The formation of the filament corresponds to a steep increase in current (bottom) [147]. h— Characterization of h-BN electrical degradation: HRTEM image of the breakdown spot in a h-BN capacitor after a SBD (top) showing the loss of crystallinity of the material [148], similar to the electrical-induced degradation revealed by TEM (bottom) attributed to missing atoms (boron vacancies) [149]. i— AFM (top) and C-AFM (bottom) images of an uncapped $HfO_2/SiO_2/Si$ structure (HfO_2 side). The AFM analysis does not reveal any macroscopic feature associated to DB, but the C-AFM highlights the presence of highly condutive breakdown spots (circles) [150].

involves applying constant voltage stress (CVS) across the device [151], measuring current leakage until dielectric breakdown is reached. This is manifested by an extremely high leakage current or conductivity and is characterized by a time-to-breakdown (t_{BD}), also referred in literature as TDDB, and the charge-to-breakdown (q_{BD}) [151–153].

Under CVS, thick dielectric layers show an initial reduction of the current in time, attributed to charge trapping phenomena, followed by an HBD [6, 141, 151] (I-t trace in **Figure 6a**). In contrast, thin dielectric layers exhibit a complex current evolution with time (I-t trace in **Figure 6b**) [6, 23, 151, 154]: SILC is detected in the initial degradation phase, followed by a sequence of small current increases (SBD), possibly terminating with an HBD or failing through a progressive breakdown process (PBD, see **Figure 6b**). In the latter case, the dielectric breakdown might not be clearly detected, requiring a periodic monitoring of the failure condition via static current-voltage (I-V) measurements [155–157]. Qualitatively similar results have been obtained when applying constant current stress (CCS) [151].

For a rapid evaluation of the robustness of the devices, a ramped voltage stress (RVS) can be used, extracting the voltage-to-breakdown (V_{BD}) [151], or breakdown voltage, which can be mapped to an equivalent t_{BD} [158, 159]. The RVS tests are currently the preferred test used for high-energy density capacitors and piezoelectric ceramics [13, 143, 160], where the V_{BD} is linked to the materials' dielectric strength. Similar techniques have also been applied for investigating the evolution of the degradation of 2D materials [148, 161].

Interestingly, even nominally identical devices exhibit slightly different breakdown metrics (i.e. t_{BD}, q_{BD}, and V_{BD}) [23], suggesting that macroscopic dielectric breakdown results from different combinations of microscopic events, averaged over the volumes of the devices. This is also supported by the difference in recorded SBD/PBD currents for nominally identical devices [23, 162, 163]. The breakdown metrics can thus only be described in statistical terms with a distribution function well described by the Weibull distribution [5, 164] (see **Figure 7a,b**). Broader distributions of t_{BD} and q_{BD} (i.e. lower shape parameter beta) are usually associated with thinner devices [153]. Under the assumption that a critical defect density is required to trigger DB [164–166], such statistical behavior is well reproduced by a percolation model [162, 164, 167]. This suggests that the degradation process involves the generation of defects at random positions in the dielectric, culminating in the formation of a percolation path that connects the electrodes. Deviations from purely Weibull statistics can also be explained by defect clustering phenomena [168].

The t_{BD} and q_{BD} statistics revealed complex field and temperature dependencies, whose origin is still debated [5]. Although approaching an exponential field dependence at high-field (with a field acceleration factor proportional to the dielectric permittivity), breakdown statistics exhibit material- and process-dependent deviations at sufficiently low-field [22, 144, 169–171] (**Figure 7c**). The t_{BD} and q_{BD} statistics also follow an approximately Arrhenius temperature dependence, revealing small deviations over sufficiently large temperature ranges [30, 144] (**Figure 7d**). Similarily, the V_{BD} statistics also reveal dependencies on temperature and stress ramp rate, with a higher V_{BD} associated to a steeper ramp, i.e. a shorter time under stress [159, 172, 173].

As the application of an electrical stress leads to the injection of electrons and holes into dielectric layers via different mechanisms illustrated in **Box 2**, the experimental leakage current can be explained by recognizing the percolation paths' defects as stable electron traps [141] forming a conductive path through the dielectric layer(s). Several experimental techniques have been used to reveal the structure and chemical composition of devices under stress and breakdown spots.

Transmission electron microscopy (TEM), commonly used to evaluate the quality of device fabrication and the resulting structural characteristics (such as the thickness, uniformity, conformity, and morphology of the layers), allowed the identification of many typologies of structural changes occurring in the dielectrics during the DB process, including: the emergence of hillocks caused by dielectric breakdown-induced epitaxy (DBIE) [145, 174, 175] (**Figure 7e**), the local phase change of the dielectric's phase with the disruption of its crystallinity (**Figure 7f**) [146], the formation of crater-like damage spot on the dielectric's surface [21] (**Figure 6c**) and of columnar features connecting the electrodes (**Figure 7g**). [147, 176–178].

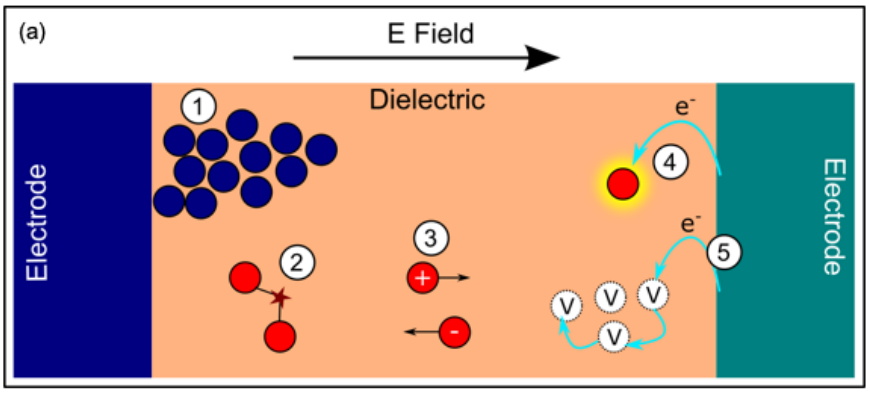
Several TEM measurements have indicated local melting at breakdown spots [179] consistent with the large power dissipated through the MOS stack. However, direct observation of heating caused by high current is still challenging. This behavior was also confirmed by High Resolution TEM (HRTEM) and Scanning TEM (STEM) [180, 181], also revealing an atomic-level degradation on damaged 2D materials as missing atoms in the lattice structure (**Figure 7h**) [148, 149].

Atomic Force Microscopy (AFM) also revealed the presence of crater-like features due to melting after extreme DB [182], similar to the TEM results. Fragile bubble-like features were also identified [177], originating from the accumulation of oxygen under the exposed electrode, which is released during oxide degradation. The release of oxygen from the dielectric under stress suggest that the final HBD occurs in an oxygen deficient material, possibly with the formation of metallic-like, VO_s-rich regions. On the contrary, being released during dielectric degradation, oxygen ions should play a minor role in the final stages of the DB process.

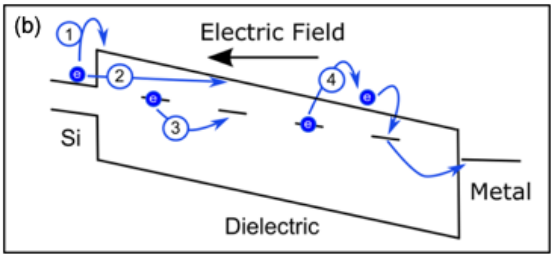
Less disruptive DBs, producing less evident features, are harder to discern from pristine materials via AFM [150, 183, 184]. In such cases, breakdown spots are better identified via Conductive AFM (C-AFM) [150, 183–186], detecting the high-conductivity regions at the exposed surface of the device (**Figure 7i**). Tomographic applications of C-AFM has been used to study conductive filaments in RRAMs [187–191], revealing the columnar conductive structures connecting the electrodes, thus supporting the hypothesis of a common nature of DB and forming processes in RRAM devices. X-ray microtomography (micro-CT) also revealed columnar structures [21], connecting crater-like spots on opposite surfaces of the device, observed after HBD of the dielectric (**Figure 6c**).

The chemical composition of degraded dielectric layers has been further studied by Electron Energy Loss Spectroscopy (EELS) and Energy-dispersive X-ray (EDX) spectroscopy. EELS applied to SiO_2 [192] and high-k HfO_2 [193] films after stress showed the presence of oxygen-deficient regions in damaged sites, supporting the hypothesis that oxygen vacancies are involved in the DB process. Conversely, EDX on damaged

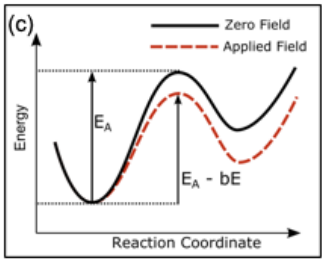
Box 2 – Processes in oxides under field-stress



A large number of processes occur when a dielectric is subjected to an external electric field. 1 - Protrusion of the electrode atoms into the dielectric. 2 - Bond breakage (vacancy generation). The exact mechanism causing bond breaking is contentious. 3 - Charged species drift-diffuse due to field. 4 – Species such as ions and defects can be charged by tunneling of carriers from the electrode. 5 – Transfer of electrons through defects (vacancies shown as an example). The processes given are not necessarily independent, for example drift-diffusion (process 3) is affected by charging of the species (process 4).



Electron transport through the dielectric under field stress occurs via transitions into the band and defect states. Application of bias causes sloping of the bands which leads to alignment of states, leading to an increased tunneling rate. Process 1 is Schottky (thermionic) emission, where electrons are thermally activated into the dielectric CB. Process 2 is Fowler-Nordheim tunneling, where tunneling is directly from Si CB to the dielectric CB. Process 3 is trap-assisted-tunneling (TAT), where electrons tunnel between adjacent traps. Process 4 is Poole-Frenkel tunneling, where electrons tunnel between trap and CB states under the influence of an external field.



Both diffusion and bond-breaking are thermally activated processes. Thus, the energetic barrier to formation is the 'activation energy' that controls the diffusion and bond-breakage rate. An applied electric field can lower the activation energy by bE, with E being the electric field strength, and b the coupling strength to the electric field.

BEOL low-k dielectric highlighted the presence of interconnect metal [23, 132], suggesting a substantially different DB mechanism, driven by metal ion drift into the dielectric.

Electron Paramagnetic Resonance (EPR) [194], electrically detected magnetic resonance (EDMR) and near-zero-field magnetoresistance (NZFMR) [195] are powerful techniques that allow detecting paramagnetic defects in devices even under stress. In pristine Si-based MOS systems, EPR allowed the identification of positively charged dangling bonds (P_b centers) at the Si/SiO_2 interface and their reduction after hydrogen passivation [196–198]. Recent NZFMR measurements made with spin-dependent recombination current involving defects at and near the Si/SiO_2 boundary reveal the generation of P_b interface defects and oxide defects near the Si/SiO_2 interface [195, 199] associated with Si dangling bonds (so-called E′ centers). In Si/high-k systems, similar results were obtained for interface defects, suggesting a similar Si interface oxidation, while peculiar states are detected for the different high-k oxides in the bulk, possibly related to oxide-specific defects, such as oxygen vacancies [200–202]

Finally, static I-V and C-V measurements at different stages of the device degradation allow for the detection of electrically active defects in the dielectric [203, 204]. Combining these results with multiscale modeling and theoretical calculations allowed to profile the defects' space and energy distributions and identify the corresponding atomic defects, such as oxygen vacancies in SiO_2 [203], HfO_2 [203], and Al_2O_3 [204].

We note that none of these techniques has sufficient resolution to precisely identify and localize the atomic level changes involved in the DB process. The experimental data confirm the percolative nature of the leakage current and degradation dynamics caused by the generation of point defects. However, the exact nature and the mechanisms of formation of these defects are not established experimentally.

4 Phenomenological electrical breakdown models

Figure 8 provides a synthetic overview of the progress in our understanding and modelling of the DB process. The most significant findings and advancements are reported with respect to a timeline marked by the major developments in the transistor technology and mainly correspond to traditional gate oxides, such as SiO_2, HfO_2 and Al_2O_3.

Following the widespread adoption of MOS technology in the 1960s, the breakdown of the SiO_2 dielectric was soon recognized as a key reliability issue of the device. The initial research efforts in the 1960s and 1970s [141, 205–211] led to the development of the first models, mainly based on impact ionization (II) processes [208, 209, 212, 213] (these can be considered as the predecessors of the anode hole injection theory [27, 214]), illustrated in **Figures 8 and 9b**. These qualitative models postulated that electrons injected into the oxide (see **Box 2**) cause the formation of (relatively fixed) positive hole charges by means of lattice ionization. The resulting changes in the electric field further support the II process, establishing a positive feedback that culminates with DB [208, 209, 213]. These models described the observed negative-resistance type instability [209, 213] in good agreement with the data at the time, but required further improvements, as in insulators, charge carriers do not normally

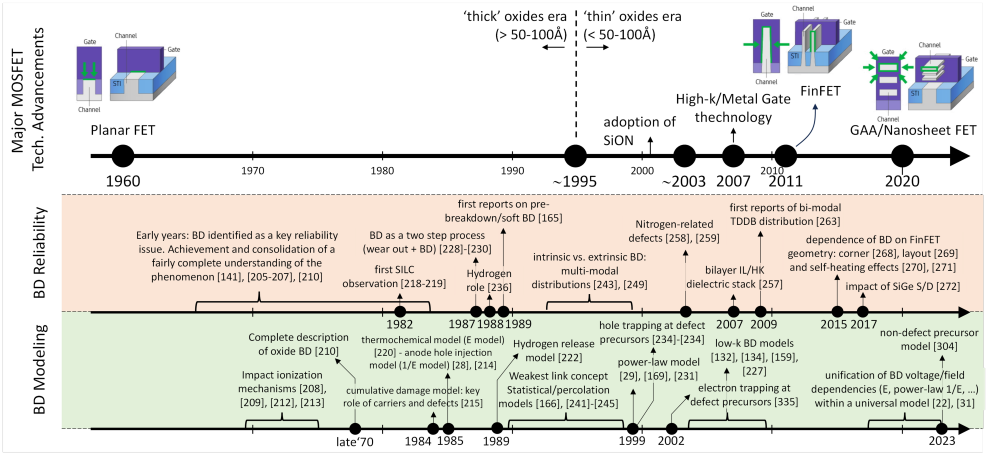
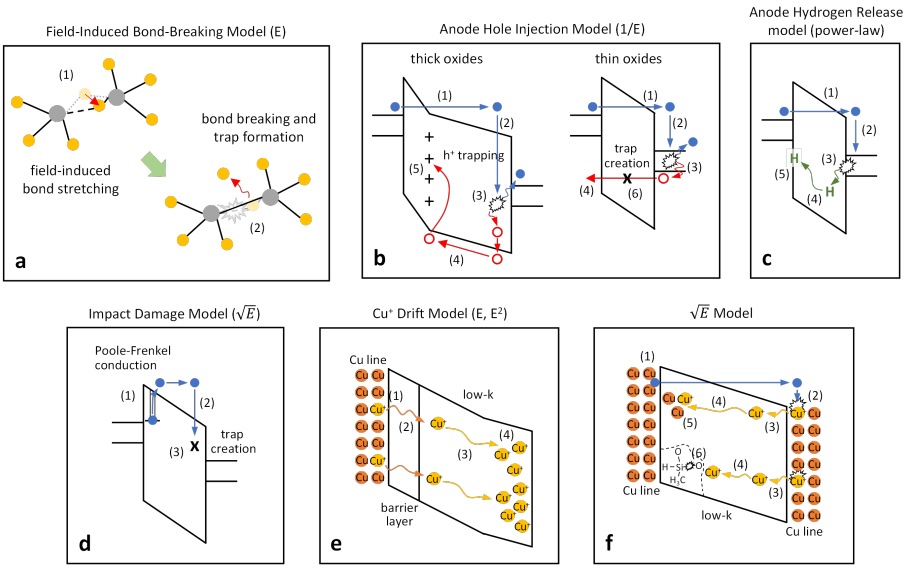


Fig. 3 Synthetic overview of the progresses made in the understanding of the breakdown process and in its modelling reported with respect to a timeline marked by the major developments in the transistor technology.

acquire sufficient energy to cause the required damage [215]. Consequently, alternative theories were proposed [215–217] in the early 1980s, following the discovery of the stress-induced leakage current (SILC) phenomenon by Maserjian and Zamani [218, 219], see **Figure 8**. While stressing a MOS structure with a relatively thin oxide, they observed a dramatic increase in conductance after large tunnel injection, which was ascribed to the buildup of positive states probably due to the breaking of strained Si-O-Si bonds [219]. Although conceptually similar to the positive charge buildup postulated by impact ionization models [208, 209, 212, 213], this new scenario was quite revolutionary as it implied – for the first time – that a defect generation mechanism was involved in the degradation and breakdown of the dielectric. This concept became the basis of the (largely overlooked) work by Jonscher and Lacoste that followed shortly after [215] and linked the DB with the presence of point defects in the insulator. They proposed that the application of an electric field promotes the creation of additional defects by the injected carriers (a process considered to be easier near preexisting ones) followed by the onset of a cumulative process that leads to the formation of defect clusters. Eventually, these clusters are thought to grow and form a breakdown path – a conductive channel between the electrodes [215]. This phenomenological theory did not provide any description of the actual defect generation processes. However, most of these ideas contributed to the development of the current, more sophisticated and material-related microscopic models discussed in Section 5.

Following these ideas, DB was recognized as a two-step process with a wear-out phase followed by a destructive phase [228–230]. Research efforts focused on identifying the possible mechanisms of the stress-induced generation of traps and the role of carriers and defects in determining the breakdown led to the development of the main competing breakdown theories still used today. The thermochemical (TC) model has been proposed in 1985 [220], the anode hole injection (AHI) model in 1989 [27, 214],



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Key features included into the the most relevant BD models

Model	Carriers' Injection	Carriers' Conduction	Ionization	Hydrogen	Field-induced Bond Breakage	Cu+ Diffusion	Carriers Trapping	Charge Accumulation	Field dependence	t_{BD} Equation
AHI	X	FN	X	–	–	–	X	X	1/E	$t_{BD} \propto exp\left(\frac{B+H}{E}\right)$
Thermochemical	–	–	–	–	X	–	–	–	E	$t_{BD} \propto exp\left(-\frac{E_A - bE}{k_B T}\right)$
AHR	X	FN	X	X	–	–	–	–	E^N	$t_{BD} \propto V^N$
Impact Damage	–	PF	X	–	X	–	–	–	$\sqrt{E}$	$t_{BD} \propto exp\left(-\gamma\sqrt{E} + \frac{E_T}{\mu q E}\right)$
Cu⁺ Drift	–	–	–	–	–	X	–	X	E, E^2	$t_{BD} \propto exp\left(\frac{E_A - \gamma E^2}{k_B T}\right) f(C_e, T, E)$ $t_{BD} \propto exp\left(\frac{E_A - q\lambda E}{k_B T}\right)$
$\sqrt{E}$	X	Schottky, PF	X	–	X	X	–	–	$\sqrt{E}$	$t_{BD} \propto exp(K\sqrt{E})$

Fig. 4 Schematic representation of the most relevant phenomenological DB models. (a) Thermochemical model [220]: (1) the applied electric field stretches/distorts oxide bonds, weakening them; (2) a new trap is created by the breaking of a weak bond. (b) Anode Hole Injection (AHI) model [27, 221]: (1) electrons are injected into the oxide by FN tunneling; (2) tunneling electrons release their energy into the lattice (thick oxides) or at the anode (thin oxides); (3) electron-hole pair are generated by impact ionization; (4) generated holes are injected back into the oxide, where they lead to (5) a positive charge build-up (thick oxides) or a generation of new traps (thin oxides). (c) Anode Hydrogen Release (AHR) model [222]: (1) electrons are injected into the oxide by FN tunneling; (2) tunneling electrons release their energy at the anode; (3) Si-H bonds present at the interface are broken by impact ionization; (4) the released hydrogen atoms (positively charged) move back into the oxide under the action of the electric field; (5) new traps are created at the cathode interface and in the oxide bulk as a result of the interaction between hydrogen atoms and the oxide lattice. (d) Impact damage model [223]: (1) electrons are injected into the oxide by the Poole-Frenkel (PF) mechanism; (2) injected electrons are accelerated by the electric field until they undergo a scattering event in which their energy is released to the lattice; (3) a new trap is created if the energy released by the electrons is high enough. (e) Copper drift model [224, 225]: (1) trap-assisted ionization of Cu atoms; (2) injection of ionized Cu^+ into the oxide (a low-k dielectric); (3) drift of Cu^+ toward the cathode interface; (4) accumulation of Cu^+ atoms at the cathode interface. This increases the local electric field, onsetting a positive feedback that eventually leads to DB. (f) $\sqrt{E}$ Copper model [132, 226, 227]: (1) electrons injection and transport towards the anode (by FN tunneling and trap assisted PF mechanism in the capping dielectric [227] or Schottky emission and band transport [132]); (2) ionization of Cu atoms; (3) injection of Cu^+ atoms into the dielectric (a low-k material); (4) Cu^+ atoms move toward the cathode; DB can be determined by the accumulation of Cu^+ atoms at the cathode interface [226, 227] as in model (e), by (5) the accumulation of neutralized Cu atoms that form a conductive metallic short between cathode and anode [132], or (6) by oxide bond breaking facilitated by the local strain induced by Cu^+ atoms [132]. (g) Summary of the key features included into the the most relevant BD models as in **Figure 9a-f**. We refer the reader to the cited papers for the definition of the symbols used in models' t_{BD} equations.

and the anode hydrogen release (AHR) model in 1999 [222]. These models are also known, respectively, as the E model, 1/E model, and power-law model [29, 231] on the basis of the predicted dependence of the DB time on the electric field. They are illustrated in **Figure 9** and their key features are summarized in **Figure 9g** along with those of other major models developed few years later (mid-2000s) to account for specific phenomena observed in the breakdown of low-k dielectrics (such as Cu^+ diffusion) [125, 134].

In the thermochemical model, **Figure 9a**, defects are generated by breaking oxide bonds weakened by the applied electric field [220]. This process culminates with the dielectric breakdown that is thus described as a field driven phenomenon in which carrier transport and current play only a minor role. The dependence of the TDDB on the electric field is exponential (see **Figure 9g**), which is why this model is also known as the E-model. It has strong link to the microscopic structure and properties of a material and is capable of explaining most of the experimental evidence [232]. However, it does not explain the different DB times reported for the same oxide field for different oxide thicknesses and voltage polarities [233]. Subsequent versions of the model tried to close this gap by including a (current-related) bond weakening process induced by hole-trapping [234, 235].

The AHI model, **Figure 9b**, is a current-based breakdown model that originated from the early impact ionization models of the 1970s. The main idea is that electrons injected into the oxide by Fowler-Nordheim (FN) tunneling (see **Box 2**) gain enough energy to create holes by impact ionization either inside the oxide or at the cathode (depending on the thickness of the oxide), as depicted in **Figure 9b** [27, 221]. The generated holes are then injected back into the oxide where they can either be trapped at existing defects (increasing the local field and triggering a positive feedback leading to DB [27]) or create new active traps responsible for dielectric degradation and breakdown [221]. Since the electron current is described via the FN tunneling mechanism, the model predicts an exponential dependence of the TDDB on the inverse of the electric field, (see **Figure 9g**), and is thus known as the 1/E-model. It is able to explain a wide range of experimental TDDB data, but fails to explain the strong temperature dependence of DB (a direct consequence of the negligible T-dependence of FN tunneling). Moreover, it has been strongly criticized because of the insufficient II hole generation rate [232].

AHR theory [222] was promoted by the discovery that hydrogen can serve as an important source of electrically active defects in SiO_2 films [236, 237] and also contribute to their generation. The AHR model is very similar to the AHI model, but with hydrogen atoms instead of holes. It is illustrated in **Figure 9c**: electrons injected through the oxide by FN tunnelling can acquire enough energy to release hydrogen atoms present at the anode interface by means of impact ionization. These free positively charged H atoms diffuse back into the oxide under the action of the applied electric field (see **Box 2**), generating traps by their interaction with the oxide lattice [222]. The AHR model was subsequently related to the empirical power-law model proposed ten years later [238, 239], in which TDDB is proportional to the (N^{th}) power of the voltage [29, 231], see equation in **Figure 9g**. Being similar to the AHI model, the AHR model also fails to explain the strong temperature dependence of

DB. In addition, the amount of hydrogen available at the anode interface may not be enough to cause DB, especially in thick oxides [232].

Recent models aim to describe the breakdown of low-k dielectrics in copper-based BEOL interconnect architectures [103], a growing concern for the reliability of the whole integrated circuit (see also the brief discussion in Section 2). The most relevant ones are the impact damage model [223], a variant of the AHI model that assumes the PF mechanism instead of FN tunneling for electron transport through the oxide (see **Box 2** and **Figure 9d)**, and models accounting for the possible role played by the motion of Cu atoms [132, 224–227], see **Figure 9e,f**. Importantly, these low-k DB models usually give different field dependence of DB (mainly $\sqrt{E}$ and E^2), as summarized in **Figure 9g**.

Parallel to the development of the main DB models discussed above, the understanding that DB was preceded by the generation of traps and that the process is random in nature and quite uniform across the entire oxide [240] led to the development of statistical models based on weakest link and percolation theories [166, 241–245]. Their foundations can be found in prior theoretical studies on the statistical nature of dielectric breakdown [246–248]. These models provide a fairly comprehensive picture of DB (nearly independent of the mechanisms considered for trap generation, often not specified) and well reproduced its thickness dependence [244] and the observed bimodality of its distribution [243, 249].

Further important steps in understanding the breakdown physics and its modeling were mainly determined by fundamental changes in transistor technology, see **Figure 8**. The transition from thick to thin (silicon dioxide) gate dielectrics in the mid-1990s unveiled the more gradual nature of the DB process and the existence of a non-destructive breakdown phase, referred to as quasi-, early or soft breakdown [165, 250–252]. Although causing a significant oxide degradation (typically manifested in the form of an anomalous increase of the SILC current [250] and current oscillations [250, 252]), such soft breakdown event did not necessarily constitute the device failure [253] (see **Figure 6b**). An additional progressive breakdown phase was also reported, in which continuous degradation [254, 255] and/or additional multiple SBD events occurred [256] before the final hard breakdown stage. The adoption of silicon oxynitride and of a high-k-based stack shortly after [comprised of a thin SiO_2-based interfacial layer (IL) and a thicker HfO_2 high-k (HK)] [257] as the gate dielectric in MOSFETs, introduced important changes in the physics of dielectric degradation and in breakdown dynamics. Although the introduction of nitrogen simply led to the appearance of nitrogen-related traps [258, 259] that could actively participate in dielectric wear out, the adoption of the high-k/metal gate technology [257], led to more profound changes.

The intrinsic high defectivness of the HK and its interaction with the underlying IL [260–262] brought additional complexity that translated into bi-modal TDDB distributions [263], a strong dependence of SILC and DB on stress polarity [263, 264] and the need to understand the degradation sequence of the IL/HK stack [265–267]. Finally, the adoption of 3D structures, such as FinFET, Gate-All-Around (GAA), and Nanosheet transistors [19], further complicated the scenario, introducing several geometry-related effects [268–272]. The use of materials with lower thermal conductivity and the additional insulation provided by the 3D structure to improve gate

control have led to a reduced ability to dissipate the heat generated in the transistor channel [273]. These so-called self-heating (SH) effects can significantly accelerate dielectric degradation, thus posing serious reliability problems even during the early device's life [273]. Recent studies have shown that the local transistor temperature can increase by nearly 50°C in scaled FinFET technologies [274] and by nearly 90°C in stacked nanosheet transistors [275] due to SH effects. In the latter case, this translates into a strong reduction in the TDDB of a single device (around two orders of magnitude) that is significantly alleviated during actual AC circuit operation [275]. A second important effect related to the 3D geometry of the transistor is the crowding of the electric field occurring at the channel edge regions. A recent study on nanosheet transistor shows that the maximum electric field at channel corners increases with corners' curvature, determining a reduction of TDDB up to three orders of magnitude [275]. Electric field effects are also at the origin of the TDDB dependence on the FinFET layout experimentally observe din [276].

Similar models have been proposed to predict reliability of low-k dielectrics used in integrated circuits. In the charge transport model [277], the dielectric failure originates from the interaction of high energy electrons with the dielectric matrix. The electrons gain energy due to the applied electric field and lose energy to the matrix through collisions with defects or other constituents of the dielectric. The energy released during the collisions is used to generate additional defects, and the mobile electrons become trapped within the dielectric by these defects. Implemented in the set of time-dependent differential equations, this model provides accurate device life-times [277] but does not specify the nature of defects involved. The DB model suggested in [278] is also defect agnostic. In this reaction diffusion drift model, H-passivated bonds or defect states are broken via injection of electrons and/or holes, oxide field and temperature. Released H atoms or ions diffuse and subsequently break other bonds to generate H_2 molecules and other hydrogen species, which diffuse or drift away. Broken bonds result in bulk traps, whose concentration at a given time is governed by the rate of defect depassivation. The solutions of kinetic equations describe the dependence of t_{BD} on temperature and oxide thickness.

5 Atomistic breakdown models of gate oxides

In spite of their importance, the nature of defects and their atomistic models as well as the mechanisms and kinetics of their generation in devices are still investigated, aided by the exponential growth of computer speed and hence our ability to accurately model the properties of novel devices at the atomic level of detail [279, 280].

Extensive studies of amorphous SiO_2 films paved the way for many perceptions and models, which have been transferred to other materials that entered the field. One of these is the importance of oxygen vacancies. The review by Deal et al. [281] was one of the first to suggest that Si directly at the Si/SiO_2 interface cannot be completely oxidized due to the lattice mismatch, so there is always excess Si and oxide is oxygen deficient. More recently, the EELS analysis performed at the site of breakdown in [192] has demonstrated that oxygen depletion is the chemical and atomistic mechanism responsible for the formation of oxide breakdown path in the ultrathin SiO_2.

Thus oxygen vacancies in SiO_2 became the primary candidates responsible for oxide degradation and breakdown path formation. They can exist in positive and negative charge states [282, 283] and their atomistic structures have been studied in several theoretical calculations reviewed in [284–286].

However, for particular defects to be effective in oxide degradation processes, they must satisfy additional criteria. One of them is the ability to change the charge state and contribute to the leakage current through the oxide upon bias application to electrodes. This requires that the defect charge transition level is located close to the Fermi energy of an electrode [286, 287] responsible for the carrier injection via tunneling (see **Box 2**). Secondly, electron tunneling between defects [the so-called Trap-Assisted Tunneling (TAT) shown as process 3 in **Box 2b**] should be efficient enough to explain the experimentally observed SILC and TDDB (see **Figure 6**b). It has been demonstrated in [288] that the SILCs in SiO_2 gate oxide films can be best explained by the generation of neutral electron traps in the oxide layer. According to the theoretical results [286], neutral O vacancies can be responsible for TAT of electrons from Si through the oxide [289]. In this process, an electron can tunnel from an electrode to a nearby neutral O vacancy that negatively charges it and then tunnels through other neutral vacancies until it reaches another electrode that contributes to SILC, as illustrated in **Box 2b**. The two other processes contributing to the current in **Box 2b** are the thermionic emission (often described/confused with the Pool-Frenkel effect, which is a simplified empirical description weakly linked to the process' physics) and the Fowler-Nordheim effect, shown as 1 and 2 in **Box 2b**, respectively. Their relative contributions depend on the bias applied and the properties of defects in the oxide. The calculations of TAT rates require knowledge of the defect structure and relaxation energies upon changes in the charge state. Apart from negatively charged O vacancies [31, 283], the hydrogen-related defects with hydrogen atom incorporated into an oxygen vacancy (the so-called hydrogen bridge) and the hydroxyl E' center turned out to be even better candidates for this process [286].

By analogy to silica, oxygen vacancies and hydrogen-related defects have been considered as the prime candidates for being involved in electrical degradation of high-k (HfO_2, ZrO_2, Al_2O_3) and other oxides [290, 291]. Many oxide films are oxygen deficient as a result of growth conditions or oxygen scavenging by metal layers. Film characterization is difficult [292] but the TEM, EELS and XPS data confirm oxygen deficiency in HfO_2 (see e.g. [293]), $BaTiO_3$ [146], $SrTiO_3$ and other oxides [294]. However, disorder in amorphous oxide films creates new challenges. In many studies in amorphous oxide films, oxygen deficiency is equated with existence of oxygen vacancies and their ability to reversibly trap and release electrons is taken for granted [286, 295]. This intuition stems from observations that the electrical performance [296] of polycrystalline and amorphous oxide films of the same composition is qualitatively similar. The notion of oxygen vacancy is well defined in fully coordinated amorphous SiO_2. However, to what extent the analogy between structures and electronic properties of defects in other crystalline and amorphous oxides can be stretched is still unclear, as discussed in [297]. This uncertainty stems from the fact that amorphous structures of many oxides, such as HfO_2, Al_2O_3, TiO_2, Ta_2O_5 and others, are characterized by distributions of atomic coordinations [295, 297]. The multi-scale modeling in [298] suggested

that preexisting O vacancies in a-SiO_2 and a-HfO_2 can contribute to SILC through thin oxide films. These calculations also confirm that further electrical degradation of the oxide layer and the HDB requires the generation of new vacancies. However, the mechanisms of vacancy creation and their structure are still debated [297, 299].

The thermochemical **E** model [24, 25] illustrated in **Figure 9a** is based on Metal–Oxygen (Me–O) bond breaking and defect creation in oxides as a result of electric field application and polarization of the dielectric. These processes have high barriers for the new defect generation [32, 302] and ignore the strong evidence that electron and hole injection, as well as hydrogen inter-diffusion from electrodes, can be involved in oxide degradation mechanisms [6]. On the other hand, recent atomistic simulations attempt to reconcile the effects of the field and carrier injection in defect creation and provide a direct link between atomistic mechanisms of defect creation and temporal evolution of electron current in devices under bias application [31, 303–305]. These models are based on a series of simulations explaining the role of injected electrons and holes in the degradation of amorphous and polycrystalline oxide films [302]. Trapping of these electrons at structural precursor sites reduces the energy barriers for the creation of O vacancies, and these barriers as well as those for O-ion diffusion are further lowered by the field [302].

The concept of precursor sites is specific for amorphous and polycrystalline films [295]. The simulations demonstrate that the elongated Si-O bonds and wide O-Si-O bond angles in a-SiO_2 [306] and the elongated Hf-O bonds in a-HfO_2 [307] can cause spontaneous trapping of up to two electrons at these sites, as shown in **Figures 10a,b**. Such sites therefore serve as precursors for electron trapping. The capture of electrons weakens the adjacent Si-O and Hf-O bonds, which break in a strong electric field assisted by thermal activation [295, 302, 308, 309]. Simulations demonstrate that, even at the close to breakdown fields, barriers for defect pair generation are more affected by the bond weakening caused by the electron localization rather than the field strength [302]. This leads to the creation of a neutral oxygen vacancy and interstitial O^{2-} ion, as illustrated in **Figures 10a,b** for the case of amorphous HfO_2. In addition, the electron trapping by oxygen vacancies both in a-SiO_2 and a-HfO_2 facilitates the creation of new vacancies at nearby sites (see **Figure 10b**). Due to this so-called "energetic correlation" effect, where pre-existing O vacancies locally increase the generation rate of additional vacancies, accelerating the oxide degradation process [32]. We note that similar electron and hole trapping phenomena causing bond breaking have been recently predicted also in amorphous $Ge_2Sb_2Te_5$ used in phase change memory devices [310].

The multiscale simulations of the whole DB process using this mechanism [32] demonstrate that, as more vacancies are generated, current increases and so does the energy that is transferred from carriers to trap sites and lattice during the TAT events. Eventually, this leads to an increase in temperature that is typically localized within a highly conductive defect region [31], further accelerating the degradation process. When distances between vacancies become less than approximately 0.5 nm, a defect sub-band is formed in which the conduction mechanisms become Ohmic and the Joule heating effect is included in calculations. This process is illustrated in **Figure 10c-n**. It is important to note that the field-induced direct bond breaking suggested in the

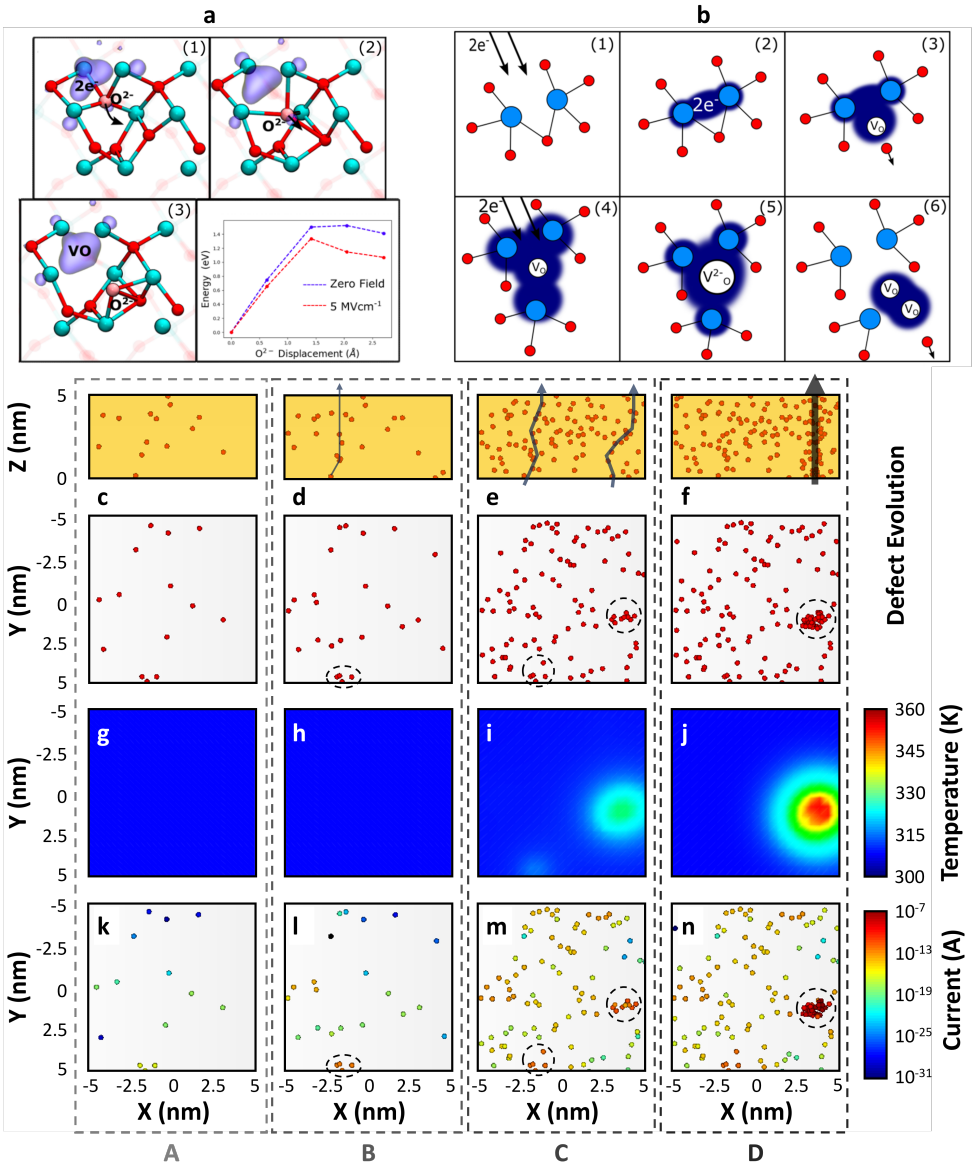

Fig. 5 (a) Schematic representation from [22] of the two-electron injection-driven vacancy formation in HfO_2. 1) HfO_2 precursor defect occupied by two electrons. 2) Oxygen ion displaced due to thermal fluctuation. 3) Interstitial-Vacancy pair formed. The graph is an energy profile of the defect formation, indicating the effect of energy reduction under field stress. (b) Schematic of the degradation model. 1) A precursor motif in a-HfO_2 captures two electrons. 2) After capturing two electrons, a bi-electron trap is formed. 3) The bi-electron trap undergoes a thermally activated process (overcoming a 1.5 eV energy barrier) where an oxygen atom is displaced to form a V_O^0-O_I^{2-} pair. 4) The newly-created V_O defect captures electrons. 5) After capturing two electrons, a -2 charged oxygen vacancy is formed. 6) A nearby O ion is displaced out of its position, creating a nearby vacancy. The activation energy for this reaction is lower than in 3). (c)-(f) distribution of oxide traps (red spheres) along the thickness and in the X, Y plane; (g)-(j) 2D (X, Y) temperature map; (k)-(n) 2D (X, Y) map of the current driven by oxide traps. Dashed circles identify (d),(l) the first SBD spot, (e),(m) the first and second SBD spots, and (f),(n) the final HBD spot. The results shown in (c) to (n) are obtained by means of simulations performed with the Ginestra® software [300] for illustration purposes. Oxygen ions created in the trap generation process (e.g. Si–O bond breaking), see Section 3, are not shown for simplicity. It must be noted that the maximum temperature reached in the HBD phase [during the thermal runaway phase, see (j)] strongly depends on the adopted stress voltage and current compliance. Values of 200°C and above can be easily reached and have been reported in the literature [31, 32, 301].

TC **E** model typically requires much higher activation energies, but becomes feasible when the oxide is already highly degraded due to the increase of local temperature and the redistribution of the internal electric field in the process of conductive path formation [267].

This new class of atomistic DB models reconciles many breakdown theories (**E**, power-law, 1/**E**, ...) within a more universal picture. They explain the transition from the **E** to the power law dependence of the TDDB on the stress voltage [22] and correctly reproduce its temperature and field dependencies in amorphous SiO_2, HfO_2 and Al_2O_3 [311]. Furthermore, they can provide fundamental insights on the evolution of dielectric degradation with an unprecedented level of detail, as shown by **Figure 10c-n**. One can monitor the evolution of the population of stress-generated traps, thus identifying the formation of the SBD **Figure 10d** and HBD **Figure 10f** spots, and the associate local temperature **Figure 10g-j** and current **Figure 10k-n** increase. However, unlike many phenomenological models, they are not analytical and require complex and time-consuming simulations.

6 Degradation and breakdown in other dielectrics

The applicability of microscopic mechanisms and atomistic models discussed in the previous Section in relation to traditional oxides SiO_2, HfO_2 and Al_2O_3 to a wider range of materials is yet to be demonstrated. In materials, such as silicon nitride and Transition Metal Oxides (TMO, such as ZrO_2, TiO_2, Ta_2O_5, ...), degradation is expected to be controlled by microscopic processes similar to those considered in the atomistic BD models described in Section 5 (with obvious differences in the atomic nature of the traps involved). The large amount of reliability data collected during the application of these materials in electronic devices (see Table 2) evidenced strong similarities of their degradation process with those in SiO_2 and HfO_2. Charge transport has been demonstrated to be assisted by traps and attributed to silicon [312] or nitrogen [313] vacancies in SiN films, and mostly oxygen vacancies in TMOs [314–317]. These pre-existing defects are also responsible for the observed SILC [317–319], and are believed to play key roles in subsequent degradation and DB processes [317, 320]. Similar behaviour is also observed in Si-based low-k dielectrics (e.g. SiCOH) with the most important differences attributed to *extrinsic* factors, such as Cu diffusion from adjacent metal lines [132].

Some important lessons can also be learned from the very extensive modeling of a filamentary resistive switching, particularly in the so-called valence-change MIM memory devices using oxide films [294, 321, 322]. The mechanisms of changes in oxide conductance observed for different voltage levels, voltage polarities and current densities, referred to as "resistive switching" have a lot in common with time-dependent DB, as pointed out in [323]. Many atomistic models of electron transport through these oxide films assume the existence of oxygen vacancies and consider the effect of impurities on the energy of their creation. For example, it is assumed that in an initial, so-called electroforming step, oxygen is extracted from the oxide layer introducing oxygen vacancies via an oxygen exchange reaction at one of the two metal/oxide interfaces [321]. The importance of oxygen vacancies has been highlighted in the TEM study

of DB in $BaTiO_3$ films as illustrated in **Figure 7f** [146]. The formation of oxygen vacancy clusters relative to structures containing the same number of disordered oxygen vacancies was used to assess the thermodynamic stability of conductive filament channel formation in several binary metal-oxides [324]. However, these models typically do not include mechanisms for the generation of new vacancies or other defects required for HBD.

In materials characterized by significantly different atomic structures (as in single layer materials or 2D materials) or with important additional physical properties (phase change, magnetic switching, etc.) the atomistic models presented in Section 5 may not apply. In novel 2D devices employing graphene and 2D chalcogenides, such as MoS_2 and WS_2, layered dielectrics like hexagonal boron nitride (hBN) could represent an excellent solution for device fabrication. Therefore, their degradation and DB is actively investigated (see e.g. [7, 148, 325, 326]), demonstrating fundamental differences with respect to *traditional* dielectrics, such as layer-to-layer DB [325] and the formation of molecular bridges [148]. In chalcogenide materials used in the development of Phase Change Memories (PCM) and Ovonic Threshold Switching (OTS) selectors, defects responsible for charge-trapping and transport phenomena have been recently demonstrated [327, 328]. However, their role in material degradation and breakdown has not yet been evaluated, with thermal breakdown historically considered the dominant mechanism [329].

Accurate predictions of DB strength and kinetics using first-principles calculations are currently unfeasible for complex perovskites and other materials, such as those used in capacitors. A different approach was developed in ref. [330] to screen perovskite materials for breakdown strength using an informatics-based approach and a transferable machine learning (ML) model. This model was trained and validated on a limited amount of accurate data generated through extensive first-principles calculations, and it allows the intrinsic dielectric breakdown strength of perovskites with different chemical compositions to be predicted in a highly efficient manner. After screening several thousand materials for stability, the intrinsic dielectric breakdown field of the most promising perovskites were calculated using the approximate Frohlich-von Hippel criterion [2] predicting that, ignoring defects, the boron-containing perovskites may be extremely tolerant toward high electric fields. Recent ML calculations led to a similar conclusion [331]. Assuming that the intrinsic dielectric breakdown field in the insulators is determined purely by the chemistry of the material, this approach has been applied to the screening of a wide range of insulators in [332]. A supervised ML algorithm known as "genetic programming" was used in [333] to identify simple models for dielectric breakdown strength of materials. It identifies the bandgap and phonon cut-off frequency as the two most relevant parameters. These early and still simplifid approaches pave the way to further applications of ML techniques in this field.

7 Outlook and Perspective

Dielectric breakdown of materials is a complex and multiscale problem at the interface between materials science, physics, solid state electrochemistry, and electronic

engineering. This is reflected in the diversity of chemical structures and morphologies of dielectrics and the number of competing models that describe their breakdown behaviour.

Phenomenological/empirical models either adopt empirical relations between the breakdown time and the stress conditions, such as in the case of the power-law model [29, 231], or provide a general probabilistic description in which DB is achieved as soon as defects randomly placed in a discretized cubic lattice create a connection between the two electrodes. This is the case in the so-called percolation models [245], which explain well several characteristic features of the experimental DB data (Weibull slope, area scaling, thickness dependence), but do not provide any insight into microscopic mechanisms.

On the contrary, physics-based models are typically based on a microscopic description of the processes involved in the degradation and breakdown of the dielectric material. They usually provide a link with material properties (e.g. bonds' nature, traps, dielectric constants, bands, etc.) and possess predictive capabilities (when properly tuned and calibrated). The thermochemical [27, 214, 220, 221], the hydrogen-based [222, 334], and atomistic models [31, 32, 234, 235, 304, 335] all fall into this category. The recently proposed multilevel energy agnostic framework [336] also falls into this category, although it has been developed independently on the actual microscopic defect generation process. Still, these models are very specialized and their transferability beyond traditional gate oxides into the realm of complex perovskites or 2D materials is unclear. Nevertheless, the developed models and methodology, represent a good starting point and a path to follow. In particular, temperature and voltage are key factors that accelerate the degradation process and the time-to-breakdown. Quite generally, the breakdown process can be thought to comprise two distinct phases as identified in the late 80s [228–230] (see Figure 8).

In the initial phase, the temperature and voltage application induce the creation of atomic defects. This process is strongly material dependent. Such defects can either assist the current transport (the leakage current increases) or trap charge (the current decreases in case of electron trapping). The defect generation is related to the breakage of atomic bond (e.g. Hf-O): this process, historically considered as uniform, can happen preferentially in close proximity to existing defects or defect precursors, and hence depends on material properties. The weakest atomic bond will be the first to be broken, i.e. the one triggering the degradation. In ternary and quaternary oxide as in BEOL, this requires to carefully investigate atomic strength.

In the second phase, once a certain number of atomic defects has been generated, the current starts increasing, inducing a local temperature increase and an internal potential redistribution triggering the positive feedback that leads to the formation of the conductive path. This process is material independent. The conductive filament size can be controlled only by limiting the power dissipation and the maximum current by imposing a current compliance during the DB experiment.

Improving device and material robustness against DB requires engineering material atomic bonds. Once the second phase is reached, the breakdown dynamics is controlled by the positive feedback loop, which is independent of the material properties. Delaying the triggering of phase 2 is thus key, and this mandates to both identify the weakest

atomic bonds in the material and to improve the bond strength through appropriate passivation (e.g. nitridation). However, this is not a trivial task. In the case of amorphous materials, bond strengths can be stochastically distributed depending on local bond lengths/angles. The presence of grains, grain boundaries, and interfaces lowers the bond strength compared to that in the bulk, further complicating the understanding. Manufacturing process is also playing a role, requiring theoretical calculations to be coupled with physical characterization and metrology (e.g. XPS, FTIR) to enable the atomic-level material engineering required for BD improvement.

In summary, the tremendous efforts of 60 years of DB research have led to a general shared understanding of breakdown physics and to the identification of the key phenomena involved. However, many details of the microscopic, material-dependent nature of the degradation process are yet not fully understood and therefore require further investigation. These include the role of interfaces between dielectric films and electrodes, effects of hydrogen present in oxide films after growth and injected during anneal and device operation, as well as importance of interface roughness and partial crystallization of oxide films. Closing this knowledge gap is necessary to reach a unified and self-consistent description of all experimental data and material-dependent trends that have been reported [5, 232]. Such an ambitious task can be easily considered as the "holy grail" of gate oxide reliability and cannot be achieved without the development and use of microscopic, material-related atomistic models capturing the growing complexity associated to extreme device scaling and adoption of new materials.

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Acknowledgments

AP acknowledges the FAR 2022-2023 project of the "Enzo Ferrari" Engineering Department of the University of Modena and Reggio Emilia, Italy, for financial support. JS and ALS are grateful to EPSRC (grant number EP/P013503/1, EP/R034540/1) for financial support. Via our membership of the UK's HEC Materials Chemistry Consortium, which is funded by EPSRC (grants No. EP/R029431, EP/X035859/1), this work used the ARCHER2 UK National Supercomputing Service (http://www.archer2.ac.uk). The authors are grateful to Ernst Wu, Gennadi Bersuker, Valeri Afanas'ev, Tibor Grasser, Souvik Mahapatra, Tony Kenyon, Adnan Mehonic for valuable discussions.

Competing Interests

Dr. Luca Larcher works at Applied Materials, the company that develops Ginestra® software, which is mentioned in the paper and has been used to produce figures 5c-n.

Short Summary

This Review provides a historic and synoptic overview of the data and knowledge accumulated on experimental and theoretical studies of dielectric breakdown in different insulating materials focusing on describing phenomenological models and novel computational approaches.

Display Items

Table 2 List of the main dielectric materials used in the most relevant semiconductor devices and their main applications. V_{TH} tuning refers to the use of oxides (mostly TMOs) to control the threshold voltage (V_{TH}) of a transistor (see e.g. [64]). A synthetic description of each device is reported in **Box 1**.

Dielectric materials used in the most relevant semiconductor devices			
Device	Application	Materials	Specific Features
Planar MOSFET	Gate Dielectric V_{TH} tuning	SiO_2; SiON [34–37]; Si_3N_4 [38]; Ta_2O_5 [39–41]; TiO_2 [42]; Al_2O_3 [43]; La_2O_3 [44], [45]; CaF_2 [46]; CeO_2 [47, 48]; HfO_2 [49–51]; ZrO_2 [49, 52]; $SrTiO_3$ [44, 53, 54]; Gd_2O_3 [55, 56]; Y_2O_3 [44, 56, 57]; Pr_2O_3 [58]; Er_2O_3 [59]; Nd_2O_3 [60]	
FinFET	Gate Dielectric V_{TH} tuning	SiO_2; HfO_2 [49–51]; Al_2O_3 [61]; La_2O_3 [62–64]; MgO [64]; Y_2O_3 [62, 64]	3D structure
GAA Nanosheet	Gate Dielectric V_{TH} tuning	SiO_2; HfO_2 [49–51]; Al_2O_3 [61]; La_2O_3 [62–64]; MgO [64]; Y_2O_3 [62, 64]	3D structure, conformality
2D Transistors	Gate Dielectric	CaF_2 [65]; MgO [66]; hBN [65]	
DRAM	Capacitor	Si_3N_4 [67]; Ta_2O_5 [40, 68, 69]; TiO_2 [70–72]; Al_2O_3 [73]; La_2O_3 [74]; HfO_2 [75]; ZrO_2 [76, 77]; $SrTiO_3$ [78]; Y_2O_3 [79]	3D structure, very thin multilayer stack
3D-NAND	Tunnel layer(s) Storage layer	SiO_2; Si_3N_4 [80, 81]; Al_2O_3 [81]; HfO_2 [82]	3D structure (cylindrical)
Magnetic RAM	Tunnel barrier	MgO [83]	Complex multilayer stack
Power transistors	Gate dielectric	SiO_2 [84]; Si_3N_4 [84]; high-k materials [84]	
RRAM	Switching dielectric	SiO_2 [85, 86]; Ta_2O_5 [87–89]; TiO_2 [88–91]; Al_2O_3 [88–90]; HfO_2 [88, 89]; SiCOH [92]; MgO [93]; hBN [94]	
Ferroelectrics	FE layer	HfO_2 [77, 95]; ZrO_2 [77]	Polarization Switching
BEOL	Capacitor	Si_3N_4 [96, 97]; Al_2O_3 [97]; HfO_2 [97]	
	MIIM diode	Ta_2O_5 [98]; TiO_2 [99]; Al_2O_3 [100]; HfO_2 [101]; Nb_2O_3 [102]	
	low-k	SiOF [103, 104]; SiCOH [103, 104]	Cu contamination, line edge roughness (LER)

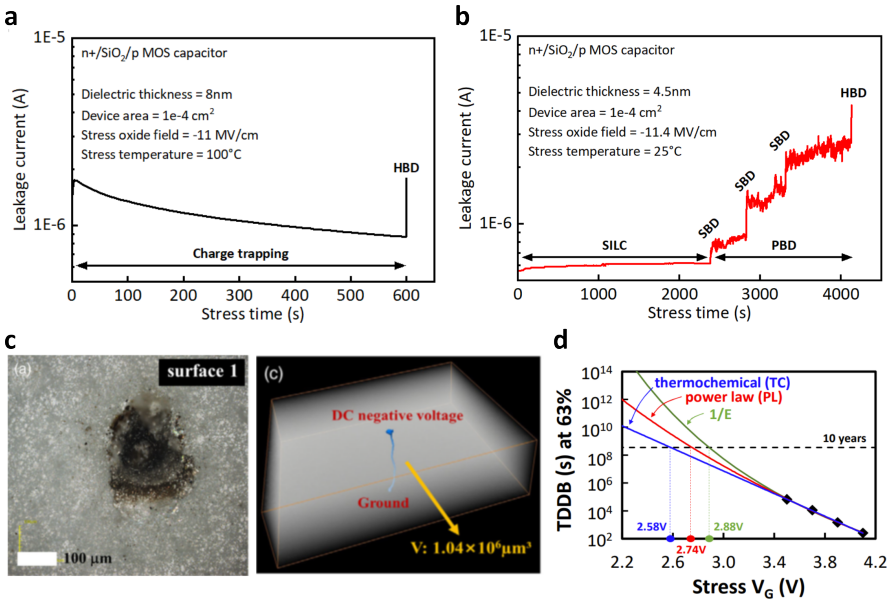


Fig. 6 Fundamentals of the dielectric breakdown process. a— The I-t trace resulting from a thick dielectric layer under CVS exhibit a current decreasing in time due to charge trapping and an abrupt HBD [20]. b— The I-t trace resulting from a thin dielectric layer under CVS exhibit an initial SILC phase, followed by a PBD phase comprising a sequence of SBD and a final HBD [20]. c— Physical damage in dielectric zirconia-toughened alumina (ZTA) after HBD: TEM imaging of the surface (left) shows a crater-like feature at the breakdown spot, while the micro-CT imaging (right) reveals a columnar structure connecting the two sides of the sample (bottom) [21]. d— TDDB projections of different models (E model, 1/E model, and power-law E model) extrapolated from high-voltage measurements highlight a significant reliability difference between the models [22].

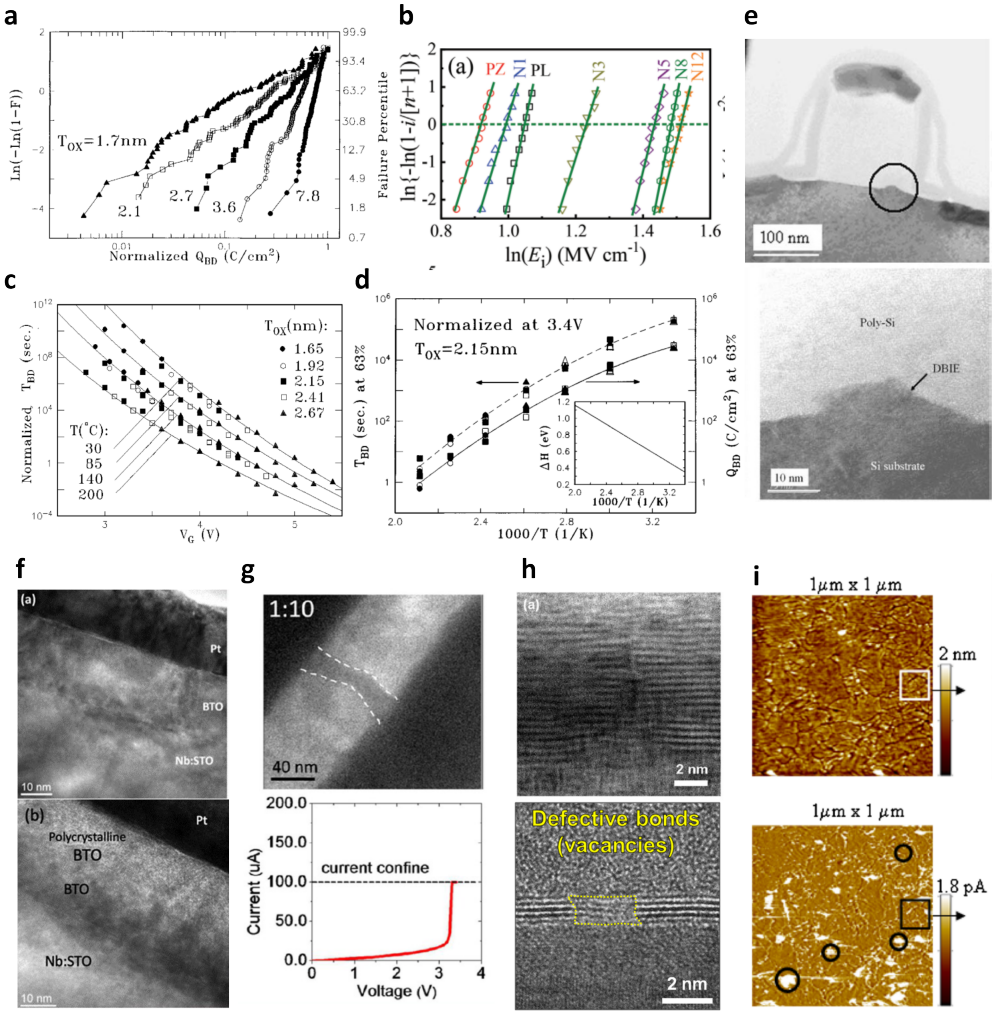


Fig. 7 Electrical and structural characterization of the dielectric breakdown process. a— The t_{BD}/q_{BD} associated to the HBD condition are stochastic variables that follow a Weibull distribution. The exhibited thickness dependence of the shape parameter beta suggests a percolative nature of the dielectric degradation process [142]. b— The V_{BD} and the related dielectric strength are also Weibull-distributed stochastic variables [143]. c— The t_{BD}/q_{BD} exhibit a complex voltage-dependence, with a significant deviation at low-field with respect to the exponential trend that can be extracted at high-field [144] d— The t_{BD}/q_{BD} also exhibit a complex temperature-dependence, revealing a non-Arrhenius trend over large temperature ranges [30]. e— TEM image of a Si/SiO_2 transistor after HBD, showing the DBIE of silicon from the substrate into the oxide [145]. f— TEM image of a Pt/BTO/Nb:STO heterostructure before (top) and after (bottom) the HBD, showing the formation of a polycrystalline BTO region, not present in the pristine device [146]. g— TEM image of a conductive filament formed in a Pt/ZnO/Pt MIM after stress (top). The formation of the filament corresponds to a steep increase in current (bottom) [147]. h— Characterization of h-BN electrical degradation: HRTEM image of the breakdown spot in a h-BN capacitor after a SBD (top) showing the loss of crystallinity of the material [148], similar to the electrical-induced degradation revealed by TEM (bottom) attributed to missing atoms (boron vacancies) [149]. i— AFM (top) and C-AFM (bottom) images of an uncapped $HfO_2/SiO_2/Si$ structure (HfO_2 side). The AFM analysis does not reveal any macroscopic feature associated to DB, but the C-AFM highlights the presence of highly condutive breakdown spots (circles) [150].

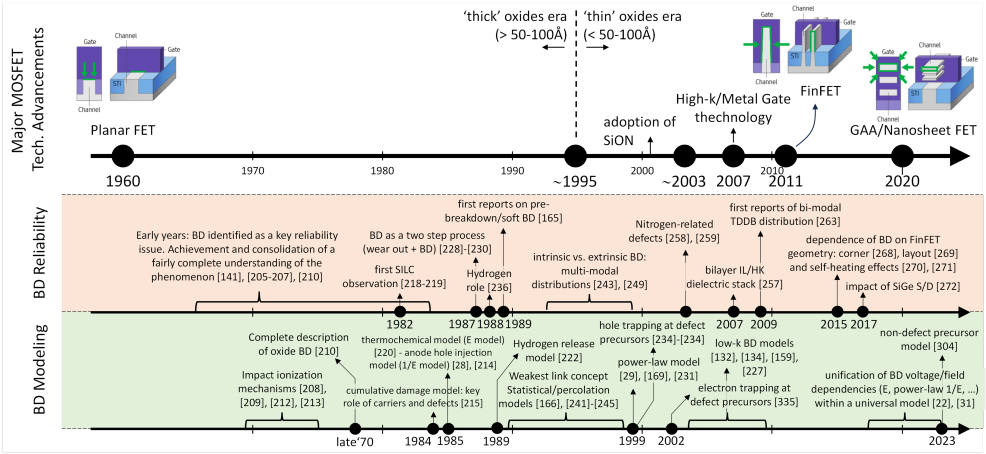
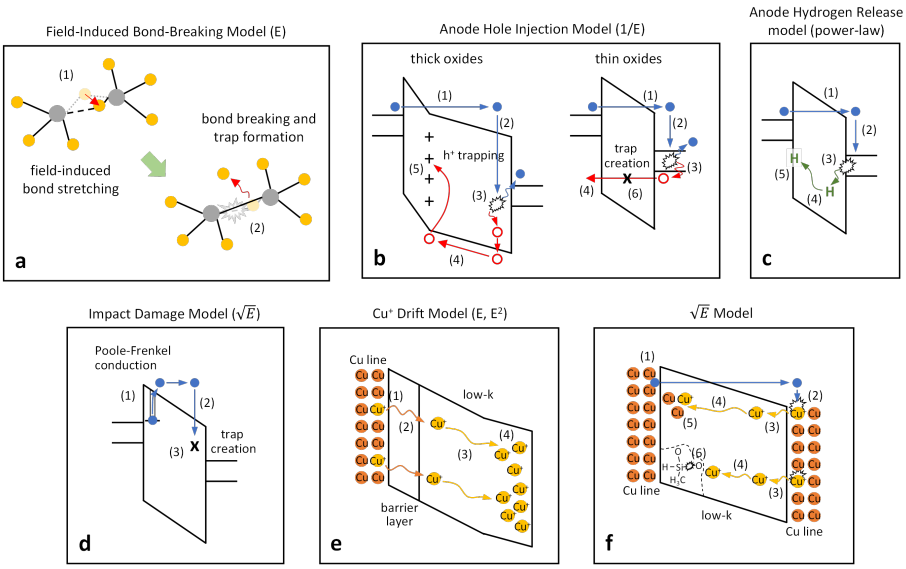


Fig. 8 Synthetic overview of the progresses made in the understanding of the breakdown process and in its modelling reported with respect to a timeline marked by the major developments in the transistor technology.



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Key features included into the the most relevant BD models

Model	Carriers' Injection	Carriers' Conduction	Ionization	Hydrogen	Field-induced Bond Breakage	Cu+ Diffusion	Carriers Trapping	Charge Accumulation	Field dependence	t_{BD} Equation
AHI	X	FN	X	–	–	–	X	X	1/E	$t_{BD} \propto exp\left(\frac{B+H}{E}\right)$
Thermochemical	–	–	–	–	X	–	–	–	E	$t_{BD} \propto exp\left(-\frac{E_A - bE}{k_B T}\right)$
AHR	X	FN	X	X	–	–	–	–	E^N	$t_{BD} \propto V^N$
Impact Damage	–	PF	X	–	X	–	–	–	$\sqrt{E}$	$t_{BD} \propto exp\left(-\gamma\sqrt{E} + \frac{E_T}{\mu q E}\right)$
Cu^+ Drift	–	–	–	–	–	X	–	X	E, E^2	$t_{BD} \propto exp\left(\frac{E_A - \gamma E^2}{k_B T}\right) f(C_e, T, E)$ $t_{BD} \propto exp\left(\frac{E_A - q\lambda E}{k_B T}\right)$
$\sqrt{E}$	X	Schottky, PF	X	–	X	X	–	–	$\sqrt{E}$	$t_{BD} \propto exp(K\sqrt{E})$

Fig. 9 Schematic representation of the most relevant phenomenological DB models. (a) Thermochemical model [220]: (1) the applied electric field stretches/distorts oxide bonds, weakening them; (2) a new trap is created by the breaking of a weak bond. (b) Anode Hole Injection (AHI) model [27, 221]: (1) electrons are injected into the oxide by FN tunneling; (2) tunneling electrons release their energy into the lattice (thick oxides) or at the anode (thin oxides); (3) electron-hole pair are generated by impact ionization; (4) generated holes are injected back into the oxide, where they lead to (5) a positive charge build-up (thick oxides) or a generation of new traps (thin oxides). (c) Anode Hydrogen Release (AHR) model [222]: (1) electrons are injected into the oxide by FN tunneling; (2) tunneling electrons release their energy at the anode; (3) Si-H bonds present at the interface are broken by impact ionization; (4) the released hydrogen atoms (positively charged) move back into the oxide under the action of the electric field; (5) new traps are created at the cathode interface and in the oxide bulk as a result of the interaction between hydrogen atoms and the oxide lattice. (d) Impact damage model [223]: (1) electrons are injected into the oxide by the Poole-Frenkel (PF) mechanism; (2) injected electrons are accelerated by the electric field until they undergo a scattering event in which their energy is released to the lattice; (3) a new trap is created if the energy released by the electrons is high enough. (e) Copper drift model [224, 225]: (1) trap-assisted ionization of Cu atoms; (2) injection of ionized Cu^+ into the oxide (a low-k dielectric); (3) drift of Cu^+ toward the cathode interface; (4) accumulation of Cu^+ atoms at the cathode interface. This increases the local electric field, onsetting a positive feedback that eventually leads to DB. (f) $\sqrt{E}$ Copper model [132, 226, 227]: (1) electrons injection and transport towards the anode (by FN tunneling and trap assisted PF mechanism in the capping dielectric [227] or Schottky emission and band transport [132]); (2) ionization of Cu atoms; (3) injection of Cu^+ atoms into the dielectric (a low-k material); (4) Cu^+ atoms move toward the cathode; DB can be determined by the accumulation of Cu^+ atoms at the cathode interface [226, 227] as in model (e), by (5) the accumulation of neutralized Cu atoms that form a conductive metallic short between cathode and anode [132], or (6) by oxide bond breaking facilitated by the local strain induced by Cu^+ atoms [132]. (g) Summary of the key features included into the the most relevant BD models as in **Figure 9a-f**. We refer the reader to the cited papers for the definition of the symbols used in models' t_{BD} equations.

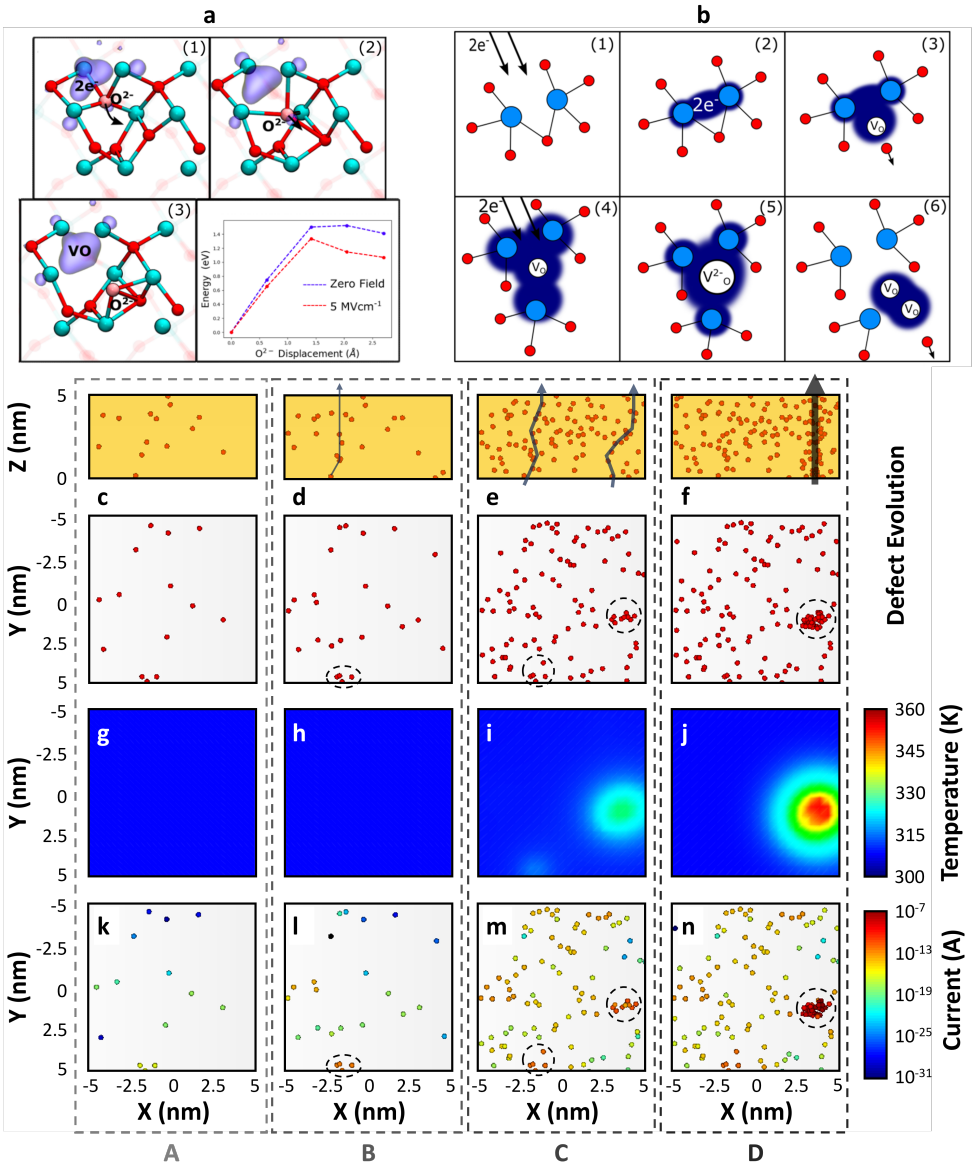
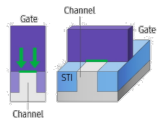
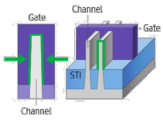


Fig. 10 (a) Schematic representation from [22] of the two-electron injection-driven vacancy formation in HfO_2. 1) HfO_2 precursor defect occupied by two electrons. 2) Oxygen ion displaced due to thermal fluctuation. 3) Interstitial-Vacancy pair formed. The graph is an energy profile of the defect formation, indicating the effect of energy reduction under field stress. (b) Schematic of the degradation model. 1) A precursor motif in a-HfO_2 captures two electrons. 2) After capturing two electrons, a bi-electron trap is formed. 3) The bi-electron trap undergoes a thermally activated process (overcoming a 1.5 eV energy barrier) where an oxygen atom is displaced to form a V_O^0-O_I^{2-} pair. 4) The newly-created V_O defect captures electrons. 5) After capturing two electrons, a -2 charged oxygen vacancy is formed. 6) A nearby O ion is displaced out of its position, creating a nearby vacancy. The activation energy for this reaction is lower than in 3). (c)-(f) distribution of oxide traps (red spheres) along the thickness and in the X, Y plane; (g)-(j) 2D (X, Y) temperature map; (k)-(n) 2D (X, Y) map of the current driven by oxide traps. Dashed circles identify (d),(l) the first SBD spot, (e),(m) the first and second SBD spots, and (f),(n) the final HBD spot. The results shown in (c) to (n) are obtained by means of simulations performed with the Ginestra® software [300] for illustration purposes. Oxygen ions created in the trap generation process (e.g. Si–O bond breaking), see Section 3, are not shown for simplicity. It must be noted that the maximum temperature reached in the HBD phase [during the thermal runaway phase, see (j)] strongly depends on the adopted stress voltage and current compliance. Values of 200°C and above can be easily reached and have been reported in the literature [31, 32, 301].

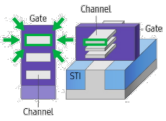
Box 1 – Semiconductor Devices



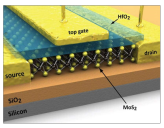
The **planar MOSFET** transistor features a flat structure with three main layers: a metal gate, a thin insulating dielectric stack, and a semiconductor. It controls the current flow between source and drain terminals by applying voltage to the gate and drain terminals. Figure adapted with permission from [110].



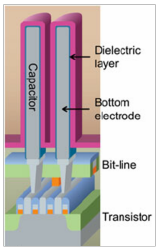
The **FinFET** is an advanced transistor featuring a three-dimensional structure where the insulating dielectric stack is wrapped around a thin vertical "fin" of semiconductor material, providing better control over the current flow. Figure adapted with permission from [110].



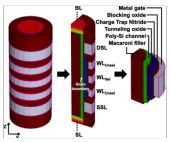
The **nanosheet** transistor is a cutting-edge technology designed to improve upon FinFET transistor. It features a multi-layered structure, where several thin horizontal layers, or "nanosheets," of semiconductor material, surrounded by the gate dielectric stack, are stacked on top of each other. Figure adapted with permission from [110].



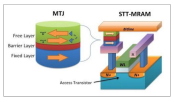
2D transistors exploit two-dimensional materials, such as graphene or transition metal dichalcogenides, to further improve electrical properties. Being in its early development phases the technology has several integration challenges, including the identification of the proper gate dielectric material. Figure reproduced with permission from [111].



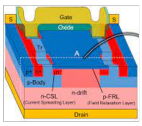
DRAM (Dynamic Random Access Memory) is a type of volatile memory that stores binary data in capacitors. The data stored in the capacitor is read and written by using a dedicated access transistor. Modern state-of-the-art 3D DRAM technologies feature cylindrical-like capacitors, made of a very thin multi-layer dielectric stack, that are vertically stacked on their access transistors. Figure reproduced with permission from [112].



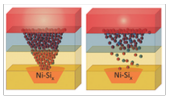
3D NAND technology represents state-of-the-art non-volatile Flash memories widely used in storage devices like solid-state drives (SSDs). Individual memory cells are stacked vertically up to 321 layers (and counting). Each cell (either charge trapping or floating gate) comprises multiple dielectric layers wrapped around a semiconductor channel in a cylindrical structure. Figure reproduced with permission from [113].



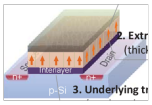
Magnetic RAM (MRAM) is a non-volatile memory device that utilizes the magnetic properties of materials to store and read information bit. Most common technology implementations rely on a magnetic tunnel junction (MTJ) comprising a very thin MgO dielectric. Figure reproduced with permission from [114].



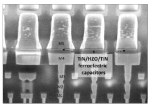
Power Transistors are semiconductor devices designed to handle and control large amounts of electrical power in electronic circuits. They exploit standard dielectrics on silicon and wide band-gap semiconductor substrates such as SiC and GaN and AlGaN. Figure adapted with permission from [115].



Resistive RAMs (RRAM) are non-volatile memories in which the information bit is stored by changing device resistance. In the common Transition Metal Oxides (TMO)-based RRAM technology, device operation relies on a controlled breakdown of one or more dielectrics. Figure adapted with permission from [116].

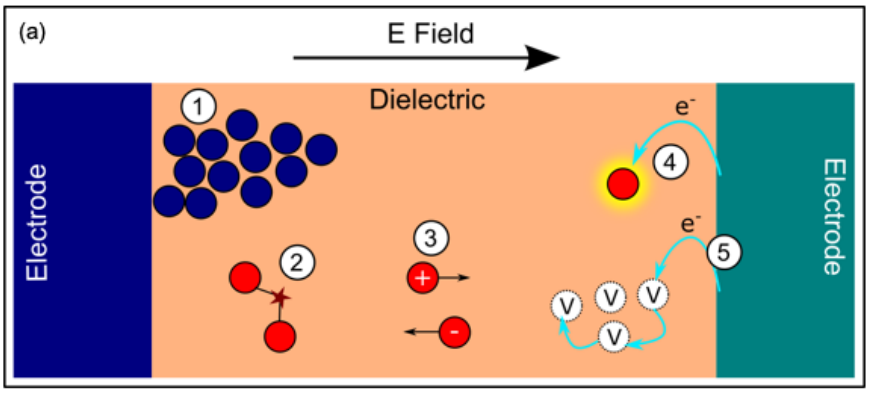


Ferroelectric transistors, **FeFETs**, and memories, **FeRAM**, exploit the unique properties of ferroelectric materials. These are dielectrics with an electric polarization that can be switched and reversed by an external electric field. Figure adapted with permission from [117].

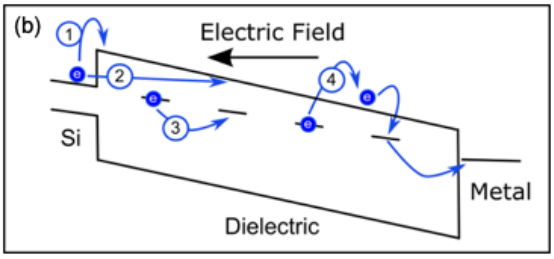


BEOL devices refer to components and structures that are fabricated in the latter stages of the fabrication process, after the creation of transistors and other active components (FEOL). They comprise a variety of dielectrics mainly used in MIM capacitor structures. Figure reproduced with permission from [118].

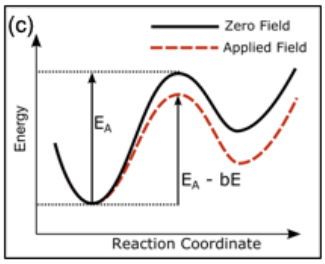
Box 2 – Processes in oxides under field-stress



A large number of processes occur when a dielectric is subjected to an external electric field. 1 - Protrusion of the electrode atoms into the dielectric. 2 - Bond breakage (vacancy generation). The exact mechanism causing bond breaking is contentious. 3 - Charged species drift-diffuse due to field. 4 – Species such as ions and defects can be charged by tunneling of carriers from the electrode. 5 – Transfer of electrons through defects (vacancies shown as an example). The processes given are not necessarily independent, for example drift-diffusion (process 3) is affected by charging of the species (process 4).



Electron transport through the dielectric under field stress occurs via transitions into the band and defect states. Application of bias causes sloping of the bands which leads to alignment of states, leading to an increased tunneling rate. Process 1 is Schottky (thermionic) emission, where electrons are thermally activated into the dielectric CB. Process 2 is Fowler-Nordheim tunneling, where tunneling is directly from Si CB to the dielectric CB. Process 3 is trap-assisted-tunneling (TAT), where electrons tunnel between adjacent traps. Process 4 is Poole-Frenkel tunneling, where electrons tunnel between trap and CB states under the influence of an external field.



Both diffusion and bond-breaking are thermally activated processes. Thus, the energetic barrier to formation is the 'activation energy' that controls the diffusion and bond-breakage rate. An applied electric field can lower the activation energy by bE, with E being the electric field strength, and b the coupling strength to the electric field.