A compact SPICE model for current transients within the subthreshold regime of memristors

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***Abstract*— In memristors and resistance switching devices, there is a region prior to switching which exhibits current transients with potentially useful dynamics. We refer to this region as the subthreshold region owing to it occurring prior to any switching threshold. These transients exhibit a characteristic peaked response with a fast rise in current followed by a slower decay. This behaviour has previously been used to quantify the mobilities of defects drifting within the active layer of the devices, but it has also been used in neuromorphic circuits to carry out edge detection, to implement homeostasis within artificial synapses and could have uses in replicating eligibility traces. We present an empirical SPICE model to reproduce these transients within circuit simulators. The model is compared with experimental datasets for a range of applied voltages and we present experimentally verified parameters for readers to use within their own simulations.**

***Keywords*— memristor, ReRAM, SPICE, modelling subthreshold.**

I. Introduction

In the pursuit for energy efficient bio-inspired computing, novel electronic devices such as memristors [1], [2] have played an important role in replicating the behaviours of biological synapses [3]. The resistance of these devices can be modulated by applying voltage pulses across the device. This property resembles the potentiation and depression behaviours of synapses where action potentials induce changes in the synapse's conductivity.

While potentiation and depression of a memristor's conductance typically occur under opposite voltage polarities, there is a region of operation where both potentiation and depression occur under the same polarity [4]. This could prove advantageous for circuit designers if it meant synapse circuits could be developed within the constraint of single rail power supplies. We refer to this region of operation as the subthreshold regime owing to it occurring before any discrete switching thresholds are met.

The subthreshold regime's characteristic behaviour is illustrated in Fig 1. When a constant voltage is applied to the device its conductance increases rapidly - eventually reaching a maximum - after which, the conductance slowly decays. Both potentiation and depression have been induced without switching voltage polarities.

This behaviour results in a unique current transient with a prominent peak. Transients similar to this have been observed in a range of oxides [5]–[7] suggesting the behaviour could be induced in the many oxide-based memristors in use today.

Historically, this current transient has been used as a method of characterization. Of particular interest is the timing of the peak, which has been used to measure the mobility of mobile ions within a oxide thin film [5], [7]–[9]. This methodology is based on a space charge limited current model in which the peak is the result of a migrating space charge generating an ionic current [10], [11]. However, the validity of applying this model is not certain. For example, alternative explanations of the current transient argue that ionic currents are negligible and electronic currents are the source of the current transient [8]; if true, this would invalidate ion mobility measurements obtained from the transient's peak. Whilst there is not yet a consensus on the physical model behind these transients, there is a general trend towards an explanation which involves the electronic conductivity being modulated via a combination of charge trapping and the migration of space charge [12].

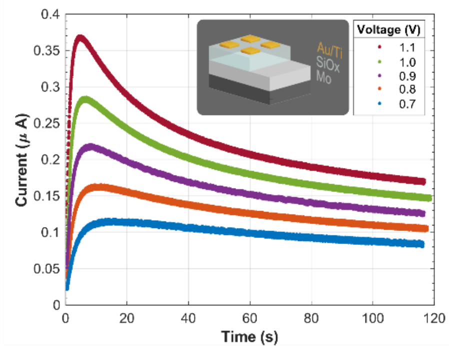

Fig 1. **The current transient phenomenon.** The current transient induced within an silicon oxide based memristor device (inset) is plotted for a number of step potentials with a range of magnitudes. The transient is a combination of a rapid increase in device current, followed by a slower decay, resulting in a characterisatically peaked reponse. The top contact is grounded while the positive voltage is applied to the bottom molybdenum contact.

Whether this behaviour can be used as a characterization tool is not yet clear, but there remains the potential to utilize the behaviour within neuromorphic computing. One such example is the use of the subthreshold regime to efficiently carry out edge detection within spike encoded images [13]. Equally, the device has shown promise in replicating synaptic behaviours such as in reproducing homeostatic behaviours [4] and the slow time dynamics of the behaviour could have use in replicating eligibility traces [14], [15]. Such long time dynamics are challenging to implement with RC circuits, however by exploiting the migration of slow ions they become obtainable. However, for circuit designers to experiment with this unique device behaviour, a model is sorely needed to enable efficient simulation.

In this paper, we present a compact SPICE model to replicate the subthreshold behaviour of devices. We will document the structure of the model and then demonstrate its accuracy in replicating constant voltage experiments.

II. Devices

The device has a metal-insulator-metal structure as illustrated in the inset of Fig 1. The top metallic contact is a combination of a 100 nm thick gold layer deposited by

electron beam evaporation and a 3 nm thick titanium buffer layer between the gold and oxide layer to improve adhesion. This contact has a size of $200 \times 200\ \mu m$. The insulator layer is a sub stoichiometric amorphous silicon oxide of thickness 35 nm deposited via magnetron sputtering. The bottom electrode is a 300 nm thick molybdenum thin film deposited via sputtering. The device was previously fabricated for use as a switching resistance memory device [16].

To induce the current transient behaviour studied in this paper, the device must undergo an electrical stressing process described in [4]. This involves applying a constant current source to the device to induce electrical defects within the oxide layer. This process results in a permanent increase in conductivity and the ability for the device to now exhibit the peaked current transients of the subthreshold regime. The magnitude of the constant current source can be tuned to modulate the dynamics of the current transient, for example by selecting for largely the depression or the potentiation of conductance.

After stressing, the device exhibits current transients as shown in Fig 1. Voltages are applied to the device at the molybdenum electrical contact while the gold electrical contact is grounded. These transients are observed for a range of voltages from 0.7 V to 1.1 V. If larger voltages are used, stressing can occur causing a gradual drift in device conductance, hence the experiments are limited to voltages $\leq 1.1\ V$. The current transients in Fig 1 form the dataset which will be used to fit the model parameters in later sections.

III. SPICE Model Definition

The current transients in amorphous silicon oxide devices appear to be the result of two separate changes occurring within the device simultaneously, resulting in both an increase and decrease in conductance. These two changes in conductance differ in several ways. Firstly, in their timing, the increase in conductance is significantly faster than the decay. Secondly, in their volatility, the increase in conductance relaxes to its initial state within tens of milliseconds while the decay in conductance can take hours to fully reset. Thirdly, in their material dependence, the decay

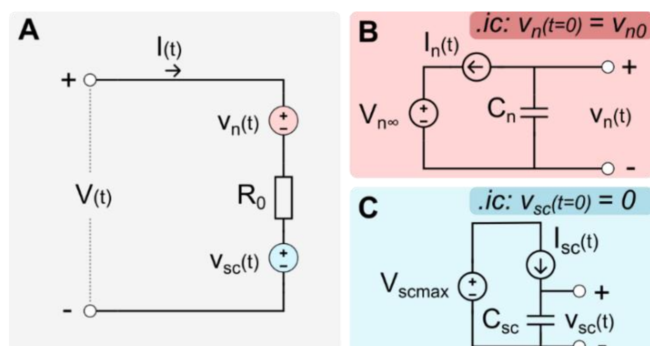

Fig 2. **SPICE Model diagram. (A)** The SPICE model produces an output current, $I(t)$, given an input voltage, $V(t)$. The circuit consists of a single resistor, R_0, in addition to two voltage sources which act to reduce or increase the magnitude of the voltage applied to the resistor. These voltage sorces are described by the sub-circuits highlighted in blue and red. **(B)** The voltage source, $v_n(t)$, has an initial value of v_{n0} and reduces over time leading to an increase in device current. (**C**) In contrast, the voltage source $v_{sc}(t)$ has an initial value of $0\ V$ and increases over time causing a reduction in the current flowing through the device. All capacitors are set to a value of $1\ F$, whereas the values of the resistors and voltage biases are obtained from fitting the experimental data.

in conductance can be removed by changing the material of the electrodes [12]. This has led to the conclusion that the two changes are driven by different mechanisms and can exist in isolation which will be detailed in the following sections. We will first present the SPICE models for each of these processes separately and then combine the two to obtain the final model.

A. Increase in Conductance

The rapid increase in conduction appears to be the result of charge trapping. This is supported by its faster timescales, its greater volatility as well as experiments where optically injected carriers were shown to accelerate the process [12].

One explanation of how charge trapping affects device conductance is that the height of a Schottky-like barrier is modulated via the population of interface states [17], [18]. Whilst Schottky barriers are strictly formed between metal-semiconductor interfaces; studies have identified similar barriers within memristor devices [19]. Our silicon oxide devices are rectifying, suggesting they too have an interface barrier at one of the metal-insulator interfaces. Equally, the filaments in our devices are formed of silicon rich regions within the oxide, hence it's feasible that the interface between these filaments and metal contacts do resemble a Schottky interface.

We model this Schottky barrier as a voltage drop, $v_n(t)$, which acts to reduce the voltage across the active layer of the device as shown in Fig 2. As the height of the Schottky barrier shrinks, the potential across the active layer increases, resulting in a larger device current.

The voltage drop caused by the Schottky-like barrier, $v_n(t)$, is time dependent and is modelled with the sub-circuit illustrated in Fig 2B. The magnitude of the voltage drop is represented within the sub-circuit by the voltage across the capacitor, C_n. It has an initial value of $v_{n0}$and is discharged by the current source, $I_n(t)$. The rate of discharge is defined by the current source whose magnitude is proportional to the difference between the current voltage drop across the Schottky barrier and its final equilibrium value as detailed in equation 1 where α corresponds to the probability of trapping a carrier and the voltage difference relates to the concentration of unpopulated states. The current source discharges the capacitor to a final equilibrium voltage, $v_{n\infty}$, where the trapping and de-trapping currents are equal.

$$I_n(t) = \alpha \times [v_n(t) - v_{n\infty}] \qquad (1)$$

B. Decay in conductance

There is strong evidence that the decay in conductance is the result of charged ions drifting within the oxide thin film. This has been proposed in the majority of publications on such current transients [5]–[7]. This is largely based on the decay in conductance being a slow process occurring on the time scale of tens to hundreds of seconds; a time scale too long to be associated with the trapping of electrons or holes. Further, in support of a drifting defect hypothesis, it has been shown that the process can be reversed by applying a voltage of opposite polarity despite the device exhibiting significantly smaller currents in the opposite polarity [12]. In our model, we continue with this approach and assume the presence of migrating defects. Importantly, we assume the ionic current induced by the migrating space charge is

negligible in comparison to the electronic currents as predicted by [8].

The electronic current through the device is assumed to be via a conductive channel within the oxide. In our silicon oxide devices, this is a silicon rich filament that forms during electrical stressing. Such filaments are common in memristors and have been observed in our devices using etching C-AFM techniques [20].

To induce an electronic current through these filaments there must be a potential across the channel. In our model, the migrating space charge modulates this current by reducing the potential experienced along the filament. This space charge is most likely a positively charged ion accumulating near the top gold electrical contact. This claim is supported by the observation that the effect of the accumulating of space charge can be removed by changing the material of the top electrical contact from gold to ITO [12]. The exact species of this ion is not yet certain. A significant amount of oxygen migration, and their associated oxygen vacancies, has been observed migrating throughout the device when under bias [21], suggesting this could be a valid candidate, but equally, in other devices hydrogen has been found to define device behaviour [22] and hydrogen has been detected within our devices in large quantities. Because it is not yet certain which ion is responsible, we therefore assume a generic space charge.

The impact of the space charge on the conductive channel is as follows. Initially, the space charge has a homogenous distribution. When the voltage is applied to the device, this imparts a force on the space charge which begins to drift and accumulate at the device electrode where it is blocked from exiting the oxide. This accumulation forms a region of higher concentration of space charge that consumes some portion of the potential applied across the device. This results in a lower potential drop across the conductive channel. As the space charge accumulates, this voltage drop increases meaning less potential is dropped across the channel causing a steady reduction in device current. Eventually, the drifting force imparted on the space charge will reach equilibrium with the diffusion and Coulombic repulsion formed by the accumulated space charge, leading to a steady state condition. When the potential is removed, the space charge diffuses back to its original distribution.

We model this process using the circuit illustrated in Fig 2. The conductive channel is modelled with a fixed resistance R_0. The voltage across the conductive channel is defined by the applied potential at the terminals of the device, $V(t)$, and the voltage source, $v_{sc}(t)$, which represents the voltage drop caused by the accumulated space charge. This voltage source is time dependent and is defined by the subcircuit shown in Fig 2C. As the voltage of this source increases overtime, the voltage across the fixed resistor drops and the device current also reduces.

The sub-circuit in Fig 2C tracks the accumulation of the space charge and its corresponding voltage drop, which is represented by the voltage across the capacitor C_{sc}. This capacitor is charged by the current source, $I_{sc}(t)$, generating a current according to equation 2. It is defined by the voltage applied across the device and, μ, which symbolises the mobility of the space charge. The current source draws charge from a voltage source representing the steady state voltage drop i.e. the maximum voltage drop consumed by the accumulated space charge, V_{scmax}.

$$I_{sc}(t) = [V_{scmax} - v_{sc}(t)] \times \ldots \\ [\mu(V(t) - v_{sc}(t))] \quad (2)$$

C. Combined Model

To complete the model, the subcircuits for both potential drops are combined as shown in Fig 2A. The two voltage drops act upon a single resistor representing the conductive channel, R_0. In practice, this channel does not exhibit ohmic conduction and so its resistance will have a voltage dependence. This is taken into account when we collect the meta-parameters.

IV. Parameter Fitting & Model Performance

The complete model has a total of six parameters, identified in Table 1. They will be fit to the dataset plotted in Fig 1, which contains current transients observed in a single device for a range of voltages from 0.7 V to 1.1 V.

Initially, the model is individually fit to each voltage trial and will then be generalised in a later stage. Fitting is carried out in MATLAB using the `fminsearch` function which employs the simplex search method [23] to minimise an error function which has been set to the mean-squared-error. The process of fitting individual voltage trials results in a set of parameters which exhibit voltage dependencies except for one exception, $v_{n\infty}$, which is spread around a central value for different voltages and so is assumed to be independent of the applied voltage. For this parameter we calculate the mean average of its value across the dataset and then set it as constant, $v_{n\infty} = 0.35\,V$.

The prediction of the model when parameters are re-optimised for each specific voltage case is plotted in Fig 3A. An example residual for the case of $V = 0.7\,V$ is plotted in Fig 3B which exhibits the worst residuals due to the lower device currents, it shows a maximum error of 13% which occurs at the onset of the transient. However, these errors drop rapidly resulting in mean error of only 1.9% across the duration of the transient. For all voltage cases the absolute error remains $< 5\,nA$ throughout the transient. This is a reasonable fit, however, there is a persistent oscillation occurring in the residuals of all voltage cases suggesting the model is missing some dynamics within the current transient. Naturally, this approach to fitting will result in a good fit because of the re-optimisation of parameters for each voltage case. However, the model is not yet generalized. In its current form the parameters of the SPICE model must be modified depending on the voltage being applied to the device. Ideally, the model would be generalized wherein a single set of parameters applies to a range of applied voltages.

To generalise the model, we must modify it to account for the voltage dependency of each parameter. Inevitably, this process introduces error into the model's behaviour and increases fitting residuals. However, the ability to predict device behaviour for a range of voltages using only a single set of parameters justifies this reduction in accuracy. For each of the voltage dependent parameters, we fit the parameter values to a suitable function, as indicated in Table 1 and illustrated in Fig 4A-E. From these functions we extract the coefficients that describe the voltage dependency, for

example the gradient and offset of a single order polynomial. We refer to these coefficients as meta-parameters because they encompass the parameters obtained previously from fitting the experimental data.

TABLE I. MODEL PARAMETER VALUES

Parameter	Function	Value
R_0	Exponential	$R_0(V) = 6.00 \times 10^6\, exp(-1.07V)$
α	Linear	$\alpha(V) = 1.09V - 0.454$
$v_{n\infty}$	Constant	$v_{n\infty} = 0.35$
v_{n0}	Linear	$v_{n0}(V) = 1.03V - 0.391$
μ	2nd Order Polynomial	$\mu(V) = -0.038V^2 + 0.142V - 0.057$
V_{scmax}	Exponential	$V_{scmax} = 5.17 \times 10^{-2}\, exp(2.01V)$

The predictions of the generalised model are shown in Fig 4F. The errors between experimental and simulated device currents for each voltage curve have increased in comparison to the voltage specific parameters. However, the advantage of the generalised model is that its parameters no longer require refitting for different applied voltages.

A significant divergence of the generalized model occurs for the case of $V = 1.1\,V$. As evident in Fig 4F, the model consistently predicts a lower device current within the first half of the transient. This may be due to the larger applied voltage and corresponding currents causing electrical stressing within the oxide. It is known that these devices respond to electrical stressing with an increase in device conductivity. [4]

We can correct for this by introducing a stressing term that acts to increase the number of traps within our representation of the Schottky interface. The discharge current described in equation 1 is modified to include a term that charges the capacitor, C_n, simulating the creation of additional trap sites. This term is proportional to the current flowing through the device, $\sigma I(t)$, where σ represents the probability of defect creation for a given magnitude of current, $I(t)$. This results in equation 3.

$$I_n(t) = \alpha \times [v_n(t) - v_{n\infty}] - \sigma I(t) \qquad (3)$$

The result of introducing this additional stressing term is plotted in Fig 5. The two models are contrasted both with and without the stressing term and it is evident that introducing the stressing term, where $\sigma = 5.71 \times 10^5$, improves the model's performance in the first half of the transient. Note, however, that the model is no longer generalized because this stressing term does not apply to smaller voltages.

To summarise, the SPICE model proposed in Fig 2 can be generalised for silicon dioxide devices for voltage ranges within $0.7\,V - 1.0\,V$. Beyond this, the model must be modified to account for the additional stressing occurring within the oxide by introducing a stressing term as described by equation 3. However, the validity of this stressing term has not been validated for voltages beyond $1.1\,V$ hence it is highly likely that further modifications would need to be made to account for stressing accurately in future work.

V. LIMITATIONS & FUTURE WORK

In its current format, the model's parameters are limited to a voltage range which avoids significant additional stressing. For example, we have limited our device characterisation to voltages $\leq 1.1\,V$. If the voltage is increased to the point that stressing begins to occur the shape of the transient changes and the model no longer holds. This range can be determined by running multiple trials at a fixed voltage, if there is a gradual increase in conductance across trials, the applied voltage should be reduced.

To extend the model to more general inputs, beyond that of a step potential, the relaxation dynamics of the current transient need to be included. This can be done by including leakage terms to the charge trapping and space charge circuitry which discharge or charge their respective capacitors.

Finally, this is an empirical model that has in part been influenced by the physical model of the device. However, there is still a significant degree of uncertainty as to what causes the current transients and whether this differs between devices of different materials. To develop more complete models, further work needs to be done to verify the physical mechanisms of this behaviour.

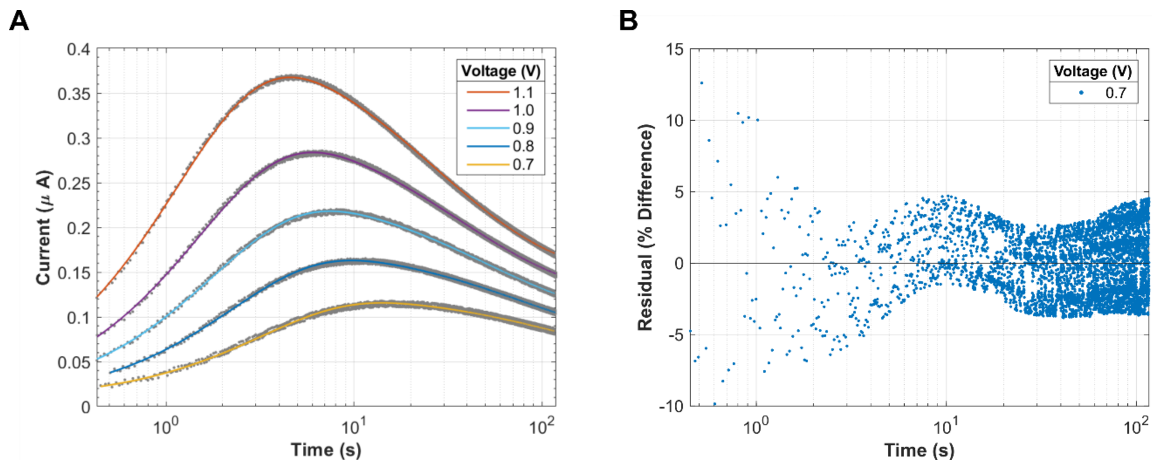

Fig 3. **Fitting performance of the SPICE model. (A)** The model's response is compared with experimental data for a range of voltages. Experimental datapoints are indicated with gray points while model predictions are plotted with solid coloured lines. For each voltage case, the parameters in table 1 are refitted to minimise the mean-squared-error between the experimental and model's response. **(B)** The residuals between the model's prediction and experimental data is plotted for $V = 0.7\,V$ which exhibits the largest error of 13% at the onset of the transient which is predominantly due to noise within the experimental data. In contrast, the average percentage difference for the duration of the transient is 2% with absolute residuals never exceeding 5 nA.

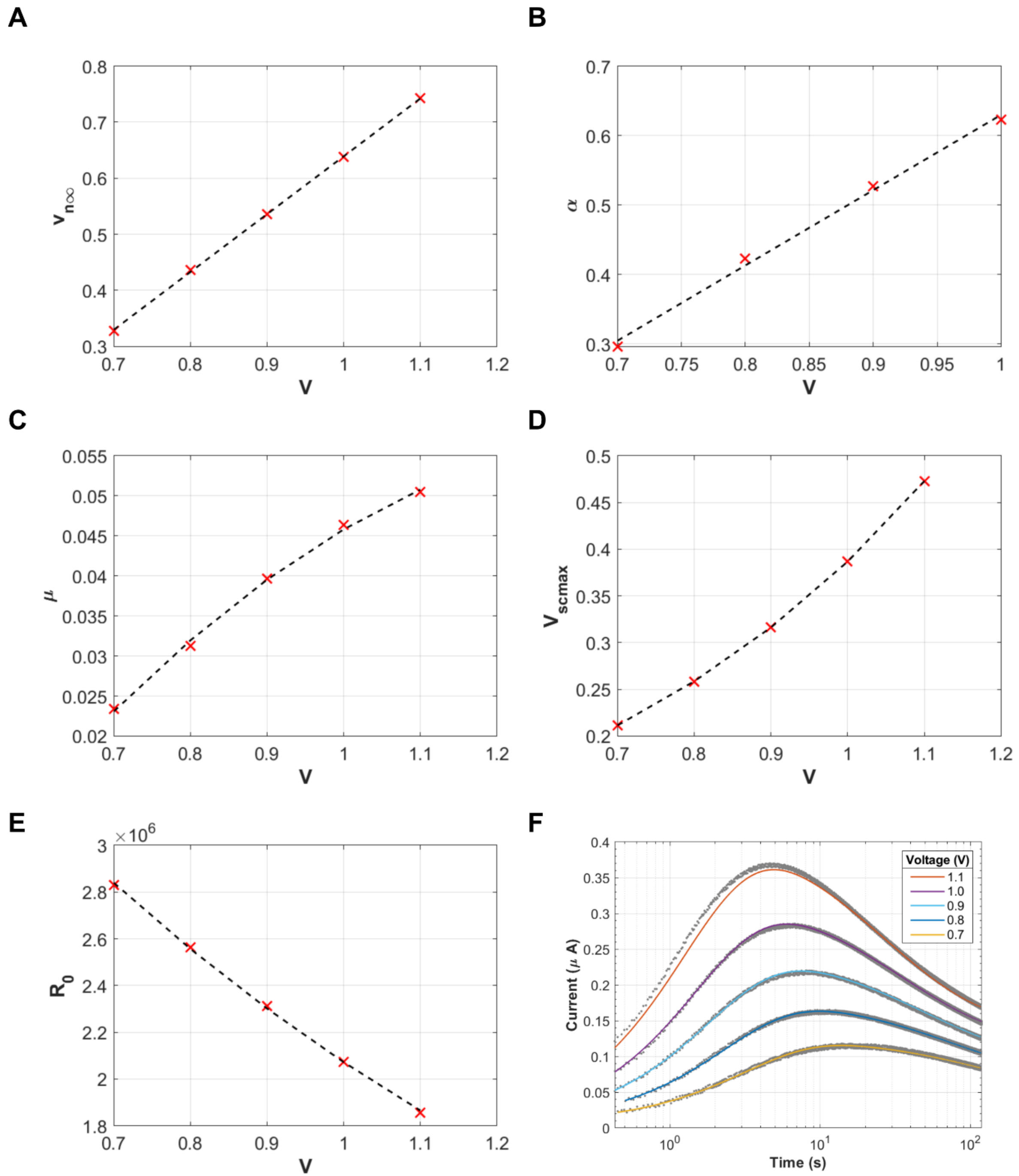

Fig 4. **Fitting of the model's meta-parameters (A-E)** The fitting for each of the model's parameters is plotted using the equations described in Table 1. The coefficients of these functions are referred to as meta-parameters and are then used in the generalised model to produce a black box model that can reproduce the current-time response to any voltage between 0.7 and 1.0 V. **(F)** The response of the generalised model is plotted alongside the experimental data. This model uses the meta-parameters described previously. The generalised model breaks down at larger voltages, i.e. at $V = 1.1\ V$, which we assume is due to the additional stressing of the oxide that occurs at higher voltages and device currents.

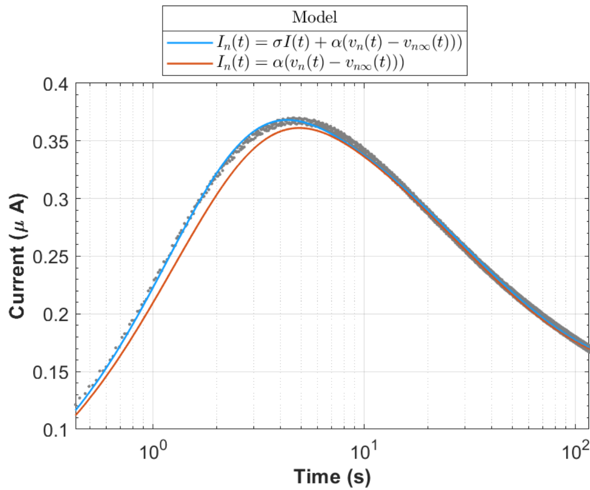

Fig 5. **Improving the fit at higher voltages.** Two versions of the generalised model are plotted for $V = 1.1\,V$. As indicated in the legend, the model including an additional stressing term, $\sigma I(t)$ where $\sigma = 5.71 \times 10^5$, achieves a better performance at this higher voltage in comparison to the model without the stressing term. We believe the need for this term suggests that stressing is starting to occur within the oxide at this higher voltage.

VI. Conclusion

We have presented an empirical SPICE model to simulate the current transients observed in the subthreshold regime of a silicon oxide memristor device. The model achieves a fit which exhibits peak errors of $\leq 13\%$ and a mean average error of $< 2\%$ when compared against experimental data. The model was generalised using meta-parameters to enable a single set of parameters for a range of applied voltages.

This model will prove useful both to circuit designers wishing to explore using this unique behaviour within neuromorphic circuits, as well as to device researchers investigating the causes of the current transient. With this SPICE model, designers can replicate previous studies which employed the subthreshold behaviour to determine edges within images, implement homeostasis within artificial synapses and explore more novel uses within memristive circuits.

VII. References

[1] L. O. Chua, "Memristor—The Missing Circuit Element," *IEEE Transactions on Circuit Theory*, 1971, doi: 10.1109/TCT.1971.1083337.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[3] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett*, 2010, doi: 10.1021/nl904092h.

[4] D. J. Mannion, V. C. Vu, W. H. Ng, A. Mehonic, and A. J. Kenyon, "Unipolar potentiation and depression in memristive devices utilising the subthreshold regime," *IEEE Trans Nanotechnol*, pp. 1–8, 2023, doi: 10.1109/TNANO.2023.3284144.

[5] S. Zafar *et al.*, "Oxygen vacancy mobility determined from current measurements in thin Ba0.5Sr0.5TiO3 films," *Appl Phys Lett*, vol. 73, no. 2, pp. 175–177, Jul. 1998, doi: 10.1063/1.121746.

[6] J. Wang and S. Trolier-McKinstry, "Oxygen vacancy motion in Er-doped barium strontium titanate thin films," *Appl Phys Lett*, vol. 89, no. 17, p. 172906, Oct. 2006, doi: 10.1063/1.2364127.

[7] F. El Kamel, P. Gonon, L. Ortega, F. Jomni, and B. Yangui, "Space charge limited transient currents and oxygen vacancy mobility in amorphous BaTiO3 thin films," *J Appl Phys*, vol. 99, no. 9, p. 094107, May 2006, doi: 10.1063/1.2196112.

[8] R. Meyer, R. Liedtke, and R. Waser, "Oxygen vacancy migration and time-dependent leakage current behavior of Ba0.3Sr0.7TiO3 thin films," *Appl Phys Lett*, vol. 86, no. 11, p. 112904, Mar. 2005, doi: 10.1063/1.1874313.

[9] Y. Li, Y. Lei, B. G. Shen, and J. R. Sun, "Visible-light-accelerated oxygen vacancy migration in strontium titanate," *Sci Rep*, vol. 5, no. 1, p. 14576, Nov. 2015, doi: 10.1038/srep14576.

[10] P. Mark and W. Helfrich, "Space-Charge-Limited Currents in Organic Crystals," *J Appl Phys*, vol. 33, no. 1, pp. 205–215, Jan. 1962, doi: 10.1063/1.1728487.

[11] A. Many and G. Rakavy, "Theory of Transient Space-Charge-Limited Currents in Solids in the Presence of Trapping," *Physical Review*, vol. 126, no. 6, pp. 1980–1988, Jun. 1962, doi: 10.1103/PhysRev.126.1980.

[12] D. J. Mannion, "Current transient phenomena in silicon oxide resistance switching oxides: characterisation and computational applications," *Doctoral thesis, UCL (University College London).* , Apr. 2022.

[13] D. J. Mannion, A. Mehonic, W. H. Ng, and A. J. Kenyon, "Memristor-Based Edge Detection for Spike Encoded Pixels," *Front Neurosci*, vol. 13, p. 1386, Jan. 2020, doi: 10.3389/fnins.2019.01386.

[14] Y. Demirag *et al.*, "PCM-trace: Scalable synaptic eligibility traces with resistivity drift of phase-change materials," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2021-May, 2021, doi: 10.1109/ISCAS51556.2021.9401446.

[15] R. A. John *et al.*, "Reconfigurable halide perovskite nanocrystal memristors for neuromorphic computing," *Nature Communications 2022 13:1*, vol. 13, no. 1, pp. 1–10, Apr. 2022, doi: 10.1038/s41467-022-29727-1.

[16] A. Mehonic *et al.*, "Intrinsic resistance switching in amorphous silicon oxide for high performance SiOx ReRAM devices," *Microelectron Eng*, vol. 178, pp. 98–103, Jun. 2017, doi: 10.1016/J.MEE.2017.04.033.

[17] A. M. Cowley and S. M. Sze, "Surface States and Barrier Height of Metal-Semiconductor Systems," *J Appl Phys*, vol. 36, no. 10, p. 3212, Jul. 2004, doi: 10.1063/1.1702952.

[18] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices, 3rd Edition - Simon M. Sze, Kwok K. Ng," *Physics of Semiconductor Devices, 3rd Edition.; John Wiley & Sons, Inc.; NJ*, 2007.

[19] M. Hansen *et al.*, "A double barrier memristive device," *Sci Rep*, vol. 5, no. 1, p. 13753, Sep. 2015, doi: 10.1038/srep13753.

[20] M. Buckwell, L. Montesi, S. Hudziak, A. Mehonic, and A. J. Kenyon, "Conductance tomography of conductive filaments in intrinsic silicon-rich silica RRAM," *Nanoscale*, vol. 7, no. 43, pp. 18030–18035, Oct. 2015, doi: 10.1039/C5NR04982B.

[21] H. R. J. Cox *et al.*, "A nanoscale analysis method to reveal oxygen exchange between environment, oxide, and electrodes in ReRAM devices," *APL Mater*, vol. 9, no. 11, p. 111109, Nov. 2021, doi: 10.1063/5.0070046.

[22] S. Vanka, H. Shin, B. A. Davidson, C. Liu, and K. Zou, "Hydrogen Atom Doping—A Versatile Method for Modulated Interface Resistive Switching," *Adv Electron Mater*, vol. 8, no. 10, p. 2200353, Oct. 2022, doi: 10.1002/AELM.202200353.

[23] J. C. Lagarias, J. A. Reeds, M. H. Wright, and P. E. Wright, "Convergence properties of the Nelder-Mead simplex method in low dimensions," *SIAM Journal on Optimization*, vol. 9, no. 1, pp. 112–147, Jul. 1998, doi: 10.1137/S1052623496303470.