Variability sources and reliability of 3D – FeFETs

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***Abstract*—Discovery of ferroelectricity (FE) in binary oxides enables the advent of FE memories and a plethora of novel CMOS compatible building blocks spanning from the logic domain to high-density storage and neuromorphic computing. In this paper we develop the first comprehensive model of vertical Ferroelectric Field Effect Transistor, V-FeFET, to identify sources of variability, understand retention problems, and point a path to improving reliability and enabling high-density storage FE memories with extended endurance.**

***Index Terms*-- V-FeFET, Ferroelectrics, HfOx, IGZO, Modeling, 3D-NAND.**

I. Introduction

The current tremendous pace of data generation requires a shift in focus toward data-centric computing and development of novel high-speed, ultra-high-density energy efficient devices. The first part of this revolution was enabled by the discovery of bit-cost scalable 3D NAND technology [1]. By going vertical to third dimension, 3D NAND Flash technology relaxed the reliability constrains of planar Flash [2] and enabled large densities (even storage of 4-bits/cell [3]) and the industry of wearables. However, the speed (µs and ms range) of program and erase operations (PRG and ERS, respectively) and very high operation voltages (±25V) limit energy efficiency and chip area (dies require additional charge-pumps that increase V_{DD} to enable successful memory operation but at the same time occupy precious area on the chip). Until recently vertical resistive random-access memories (V-RRAM [4-8]) were considered as the only and the major contenders to replace Flash due to its cell fabrication simplicity. However, the stochastic nature and poor physical mechanistic understanding of RRAM are critical obstacles to its high-density integration and are preventing it reaching the maturity level of high-density standalone-memory product.

Stabilization of ferroelectricity (FE) in binary oxides (i.e. doped HfO_x [9-11], HZO [12-17]) and nitrides (e.g, Sc:doped AlN [18]) triggered significant research interest in ferroelectric devices across the memory hierarchy (1) logic/latch: Negative-Capacitance (NC-FETs) [19-24]; (2) Dynamic Random access memory (DRAM) replacement (FeRAM) [25,26]; (3) Ferroelectric FETs – Fe FETs [27-29]; (4) Storage-class V-FeFETs [30,31]; and even applications such as neuromorphic[33-35] and security [36]. Compared to other alternative emerging memories (Phase change memories – PCM, magnetic RAMs – MRAMs and other RRAMs), FE devices and memories can be used in the whole memory hierarchy. They are the only memory that can be programmed and erased using electric field, that results in ultra-low power required for writing the bit (see Table I). The V-FeFET technology is referred to as a potential game changer in storage-class-memory (SCM) domain that would enable low-power storage and analog in-memory computing. Even though 3D-NAND-like V-FeFETs [30] offer a significant increase in speed (1000x) and reduction in operation voltage (4x) they still offer a charge-trapping (CT) NAND like endurance (10^4 cycles), and doubtfully they can offer multi-level-cell (MLC) capability [30] while keeping the low-operation conditions. We utilize a modeling-augmented flow, to understand the defect nature, phase changes, and physical mechanism in FE HfO_x; analyze reliability of V-FeFET and develop a comprehensive reliability model which captures FE-CT entanglement, phase transformations, depolarization-fields and the impacts on stability of the stored states and degradation of V-FeFET.

TABLE I. Direct comparison of NAND Flash and V-FeFET cell

Memory cell property	Memory Device	
	Charge trapping NAND [2]	***V-FeFET [30]***
Energy/bit	< 1nJ	< 1fJ
Endurance [cycles]	10^4	10^4
PRG/ERS PW & PA	100 µs/10ms ±25V	100ns -7/7V
Retention @ 85°C	10 years	10 years
Cell area [µm²]	$0.026/N_{layer}$	$0.026/N_{layer}$
MLC Capable [Y/N]	Yes	limited

The paper is organized as follows: In section II experimental details and modeling framework are discussed. In section III, extraction of the FE, phase and defect properties and development of FE model (with emphasis on wake-up and fatigue) are described. Section IV explains charge-trapping – FE entanglement, its impact on endurance as well as the depolarization field and retention issues of FeFET. Furthermore, potential solutions for endurance and retention issues are discussed. Conclusions are drawn in section V.

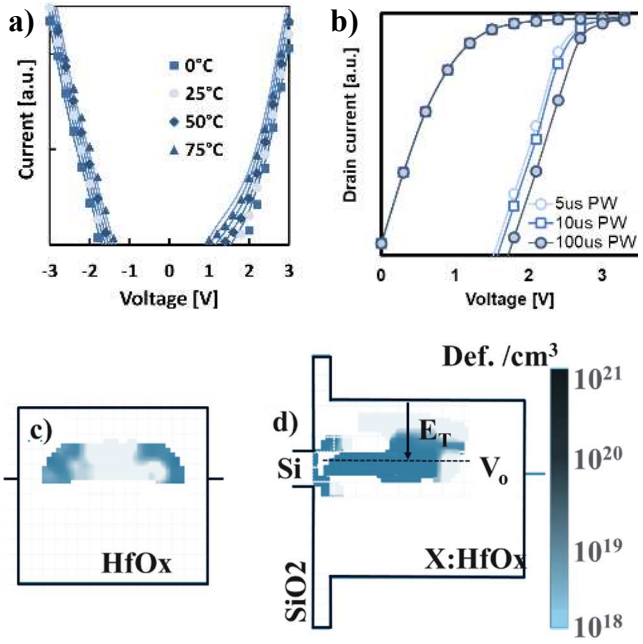

Figure 1. a) I-V of the FE capacitor; b) TSCIS of FeFET and corresponding defect maps of c)FE capacitor and d) FeFET under test.

II. Experimental and Modeling Framework

In this study, to understand the reliability challenges and physical mechanisms, we utilized and extended our commercially available multiscale modeling platform Ginestra® [37]. The modeling framework is comprised of two main interconnected parts, that cover the charge (e/h), and material transport as well as the stress-induced material modifications. All of these are critical to model device aging and the reliability phenomena as well as physics behind it [38-42]. The capability to handle discrete contributions of charge, atomic species, and defects (i.e. interstitial ions and vacancies) is included, as well as the capability to simulate their diffusion and generation processes. The tool also accounts for the FE properties of the film responsible for switching processes and kinetics. The electric potential within the FE-device is calculated by solving the Poisson equation consistently with time dependent Landau-Khalatnikov formalism enriched with the Ginzburg domain interaction and depolarization term [42]. Furthermore, VASP ab-initio modeling software [43] was used for density function theory (DFT) calculations with projected augmented basis sets and appropriate climbing image nudged elastic band method for diffusion characteristics.

For the electrical characterization and defect spectroscopy two main test vehicles are used i.e. ferroelectric FET (FeFET) transistors with Si:HfO_x gate dielectric [42] as well as the metal-insulator-metal (MIM) FE capacitors (FeCAPs) with HfO_2, ZrO_2 and HZO dielectrics are considered. Defect extraction was carried out using temperature dependent leakage current measurements on FeCAPs and transient spectroscopy by charge injection and sensing (TSCIS) [44] as well as charge pumping methodology [45].

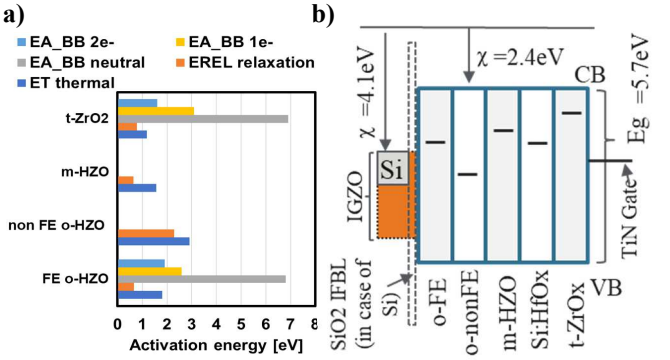

Figure 2. a) Calibrated, extracted HZO and ZrO_2 defect properties and activation energies from capacitors with different phases and defects. b) Constructed band diagram with corresponding defect levels within the bandgap. E_A denotes activation energy, E_{A_BB} denotes bond-breaking energy, E_T denotes thermal ionization energy and E_{REL} relaxation energy of the defects.

III. Ferroelectric Reliability

A. *Ferroelectric layer – defect and phase spectroscopy*

We characterized (Fig.1) three different material stacks i.e. MIM capacitors with TiN electrodes comprising tetragonal (t-) ZrO_2, orthorombic (o-) HZO and monoclinic (m-) HfO_x exhibiting anti-ferroelectric, FE and paraelectric properties, respectively. Applying the defect spectroscopy technique [46] on planar capacitors and TSCIS [44] on FeFET fabricated in 28nm HKMG technology [42], we obtained defect maps (Fig.1c-d). Ab-initio modeling software [43] was used for density functional theory calculations to explore diffusion processes and the impacts of extra electrons on the diffusion characteristics to mimic the influence of field. Our results suggest ferroelectric and monoclinic HZO phases have similar lattice relaxation energy in turn suggesting these phases have similar electronic structure and bonding. In addition, the phase transition between them has a low energy barrier [47]. Three different phases of ZrO_2, (Fig. 2) show similar lattice relaxation energy though the thermal energy or defect level differs between the three phases. Both HZO and ZrO_2 show a 3.5+ eV barrier height reduction for interstitial diffusion when oxygen vacancy is charged compared to its neutral state. A summary of extracted defect properties (thermal ionization energies, vacancy relaxation energies and bond-breaking energy) is given in Fig.2a while the reconstructed band diagram of the FE, with a focus on defect energetics, is shown in Fig.2b.

B. *Ferroelectric layer – reliability model*

Binary oxide ferroelectric materials i.e. HZO and doped HfO_x are polycrystalline and generally defect rich. They are

characterized by two lifetime stages i.e. wake-up and fatigue that correspond to opening and closing the polarization-voltage (P-V) hysteresis, respectively [38]. To model the lifetime of the ferroelectric capacitor, a multidomain and multigrain FE layer with thickness of 10 nm was defined and sandwiched between two TiN electrodes. Calculated and extracted defect properties, summarized in Fig.2 were used to model trapping and define multiple phases within the FeCAP. To explore switching – trapping entanglement further a multidomain time-dependent model was developed (Fig.3) and used to calibrate the switching parameters and model the wake-up effect in addition to extracting defect properties. Using simple analytic equation (that corelates coercive field and polarization to Landau parameters) reported in [48], Landau parameters (alpha, beta) were extracted while the dynamics was captured by tuning the dumping coefficient ρ i.e. the internal resistance of ferroelectric [49]. The model captured domain nucleation and propagation (Fig.3b) and we identified charge and vacancy redistribution and depolarization field (E_{dep}) reduction (phase-transform) as the main drivers of wake-up. The merging of the switching current peaks and corresponding opening of a polarization-voltage (P-V) hysteresis is captured successfully (Fig.3c-d). The merging of the P-V characteristics is a direct consequence of the reduction/diminishing of the local internal bias fields that are superimposed on the external excitation field. This superposition of fields (internal and external) results in local biasing of the domains and creating domain distributions that manifest through the multiple current peaks and pinched P-V hysteresis in the pristine stage of the device. An internal field is generated by the trapped charge on the phase, interphase and grain boundaries as well as by the random phase (FE and non-FE) and oxygen vacancy distribution. Additionally, it should be noted that non-ferroelectric portions of the active layer and any non-switching interfaces result in depolarization fields that may destabilize the domains. This in turn creates sources of variability and can compromise retention and the stability of the state that will be discussed later in the section IV-B. External stress generated by application of electric field on the device results in vacancy redistribution, charge redistribution and phase-transformation that in turn reduces the internal-bias, merging the current peaks and opening the polarization hysteresis loop that can be interpreted as opening the memory window (MW).

Further stressing of the device by PRG/ERS operation results in generation of oxygen vacancies that trap charge and alter the electrostatics of the device. Trapped charge modifies the electric field locally while the degradation and excess generation of oxygen vacancy – oxygen ion pairs can result in large trapping which can pin the domain and practically shut-down part of the active region. This generation degrades the peak current that in turn reduces the remnant polarization, P_r and results in closing of the MW (see Fig.3e). Therefore, we emulated the degradation of FE layer dominated by domain pinning and Frenkel-pair generation (Fig.3e) and found out that domain pinning (Fig. 3f-h) reduced both P_r and MW. Domain pinning by charge trapping is illustrated by injection of charge from different terminals (top and bottom) and by consequent trapping that pins and switches-off top and bottom right portion of the device, respectively (Fig.3f-h).

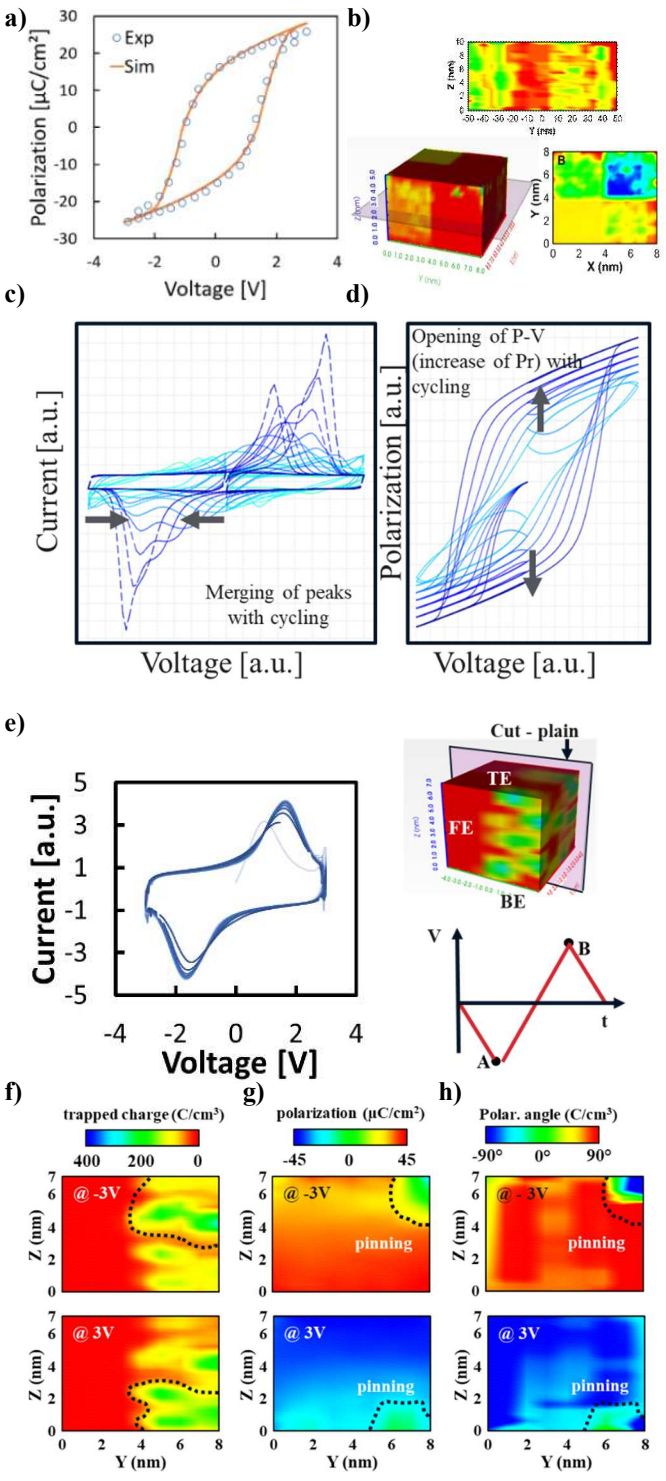

Figure 3. a) P-V loop of calibrated FE device and b) domain nucleation and propagation in the FE device. Modeled wake-up behavior of the ferroelectric material manifested through c) peak merging within I-V characteristics and merging of switching distributions and d) increase of remanent polarization – P_r in P-V characteristics (de-pinching of P-V hysteresis). e) I-V evolution (fatigue behavior) i.e. endurance degradation (drop of the polarization with stress) of modeled FE device with cycling; domain-pinning and impact of the injection side and polycrystallinity on f) trapped-charge; g) polarization; h) polarization orientation at A and B i.e. -3V and 3V applied on top, respectively.

Furthermore, our model elucidated that the significantly lower E_T for t-ZrO2 lowered the probability of electron injection and trapping compared to FE HZO and non-FE HZO which is the key for superior reliability of anti-FE films reported in [50-53]. In FE and non-FE HZO trapping in deep states results in permanent trapping that accelerates bond breakage and reduces device lifetime. In the next section material learning and underlying physics is going to be applied to vertical 3D FeFET devices.

IV. Retention and Endurance of V-FeFET

To properly understand and engineer a novel device, a deep understanding of the material is required to identify all effects occurring in FE region and channel. In the next section we discuss how the polycrystallinity of the channel impacts the memory performance and I_D-V_G.

A. Channel materials and voltage divider

To capture the mobility degradation and scattering on grain boundaries (GBs) of the polySi channel we reconstructed a highly granular material with DFT-derived properties of polySi grains, i.e., bandgap (E_g) and the energy barrier for motion between grains (Table II) and combined it with a developed model of the FE layer. I_D-V_G degradation increases with increasing grain-to-grain barrier (Fig.4a-b). The summation of these effects, on the first sight, do not provide the significant read margin that would be needed for intermediate states, between the high and low V_{TH}, the required window for enabling MLC capability (Fig.4c). Nonetheless, optimization target algorithms may be used to squeeze multiple states and enable usage as a synaptic element or high-density storage with multiple states between the high and low threshold voltage [55]. Still, the stability of those states remains questionable.

TABLE II. Polysilicon Channel Grain Properties

Grain boundary details	Grain Boundary properties	
	Eg [eV]	*Barrier [eV]*
(111)	0.57	0.02
(1-12)	gapless	0.17
(120)	0.92	0.072
(130)	0.97	0.21
(1-1-3)	0.54	0.12

Beside the Si and polySi channel materials, oxide semiconductors and materials like IGZO may be used to improve performance and reliability. A semiconducting oxide channel enables direct growth of FE on top of IGZO channel, thus reducing the voltage drop over the interface (Fig. 4d-e) and in turn may improve device lifetime. In our previous studies [39, 42, 49] we show that a high-operation field results in a high field drop across the low-k interface yielding a much higher generation of defect states within the interfacial layer. This interface defect generation can initially help the switching, stabilize and open-up the MW of FeFET [42]. For this purpose, we simulated the behavior of the gate-current that directly manifests the switching domain dynamics depending on the presence or absence of defects and trapped charge. In [42] we showed that, in a device with charge trapping effects included (Fig. 5), trapping pins the field at the interface, inducing a stronger change in the field across the FE:HfO_2, that forces an earlier onset of FE switching (domain 1) enables reaching previously inactive "slow" domains (domain 2 and domain 3) compared to the reference device (without defects and charge trapping). However, with further cycling this increased field and repeatedly tunneling of charge, back and forth, through the interfacial buffer layer results in destruction of the interface and generates defects in the bulk of the high-k of the device. Finally, this degradation increases leakage current. The defect generation and consecutive trapping pins the domains and closes the MW of FeFET [42].

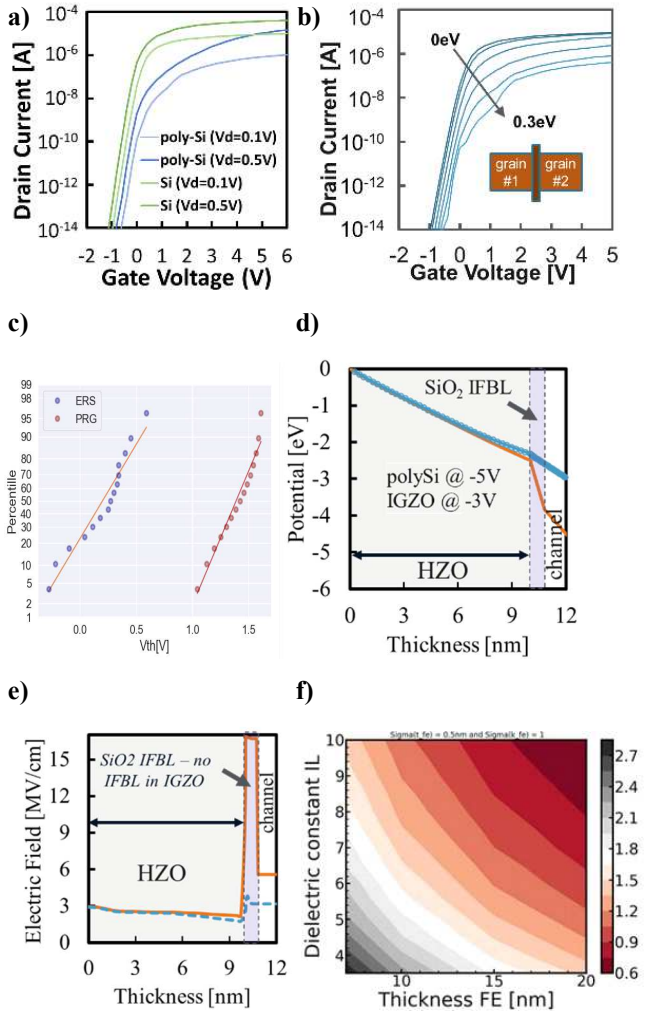

Figure 4. a) Si and polySi channel performance and b) degradation of I_D-V_G with increase of barrier between the grains of polySi channel. c) Variability of the V-FeFET due to the polycrystalline nature of the channel and FE. Comparison of d) potential, e) electric field distribution (PolySi vs. IGZO channel) with and without IFBL (that takes majority of electric field and increase operation condition). f) Depolarization field design rule.

B. *Charge trapping, Depolarization field and rentetion of MLC*

As previously mentioned, introduction of the interfacial buffer layer (IFBL) generates not only a voltage divider but also increases the depolarization field that consequently reduces the P_r and shrinks the MW. The depolarization field represents one of the biggest challenges for retention of a bilayer structure comprising an active, FE switching and a passive, non-switching layer (e.g., an interfacial buffer layer). The depolarization field represents a field in an opposite direction to the polarization state that tends to destabilize and flip the stored state of the device. It is one of the main causes of retention loss in these devices.

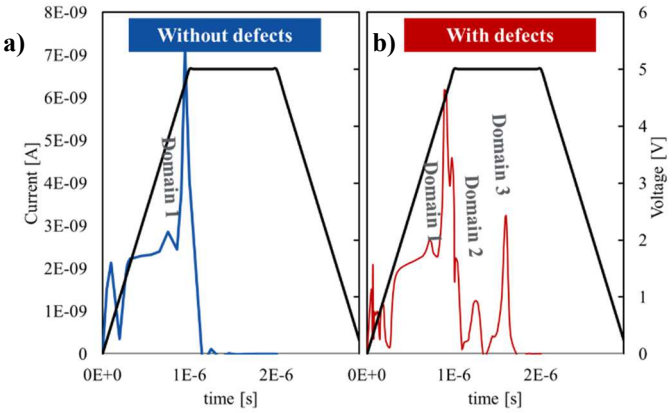

Figure 5. Simulated switching kinetics of the 3-domain based FeFET depending on its interaction with interface and bulk defects. Upon application of the positive voltage gate current results in a) single domain and b) three-domian switching without and with defects (and trapped charges) included, respectivelly.

The ability to directly grow the FE layer on top of the channel is of high importance since the IFBL generates E_{dep} that tends to destabilize the FeFET retention especially if the device is operated in subloop (intermediate states) with domains partially switched. For this purpose, we construct a 3D-NAND like V-FeFET string with 3-tiers (gates) as shown in Fig.6a. Similarly, to classic 3D NAND device, as a channel material polycrystalline Si was used, while on the place of the tunneling layer, in FeFET 0.8nm SiO_2 thick interfacial buffer layer was implemented. Instead of the trapping nitride layer, that can be found in the CT 3D NAND devices, an 8 nm thick FE:HfO_x layer was used. Furthermore, to account for the highly gradual nature of FE:HfO_x, under each of the three gates of our V-FeFET multigrain FE:HfO_x (with 4 grains) was defined. As an example, a 3-tier V-FeFET device (Fig.6a) is set in different polarization states to emulate MLC behavior (Fig. 6c-e). In Fig.6e, gate 3 (G3) was partially programmed and domain stability was analyzed in detail. In the Fig.6f 4-grain FE:HfO_x polarization orientation under the Gate 3 is represented. Even though the partially programmed (PRG) gate yielded reversal of FE polarization and a significant channel conductance change, over the short time scale, a sudden collapse of domains (due to E_{dep}) and accompanying channel potential change are observed. This result compromises the MLC reliability of the V-FeFET. It can be concluded that removal or reduction of IFBL (or increase of k-value) is essential to enable a reliable MLC V-FeFET. Removal of the IFBL (by using an IGZO channel and direct growth of FE on top of channel material) results in strong reduction of E_{dep} to guarantee retention of the intermediate states (Fig. 7a).

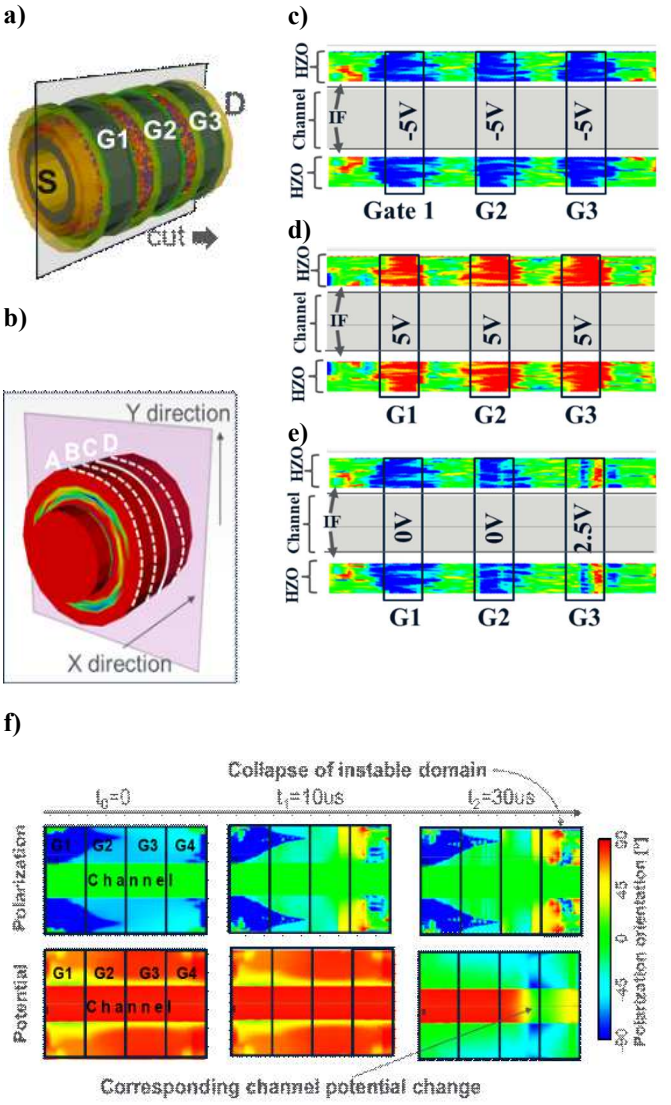

Figure 6. a) Multi-grain V-FeFET with polySi channel and corresponding b) x-cut of polarization change with application of c) ERS, d) PRG and e) intermediate PRG required for MLC. f) Multigrain-nature of FE within the single gate/tier of the V-FeFET string and collapse of the instable domain due to the IFBL induced depolarization and polycrystalline nature of FE material.

In addition, removal of the IFBL would result in reduction of PRG and ERS voltages by 40% to approximately 3V, enabling ultra-low memory operation. Furthermore, switching to an interface-less, IGZO-channel FeFET eliminates accelerated degradation and breakdown of IFBL and extends the endurance to be comparable to a capacitor-based FeRAM. Transition to interface-less IGZO channel, reduces trapping and eliminates the possibility of IFBL destruction and degradation the FeFET operation through closing the FE MW,

in turn enabling FE-limited endurance (>10^{10}) compared to IBFL-limited (Fig.7). Still, a novel integration and encapsulation techniques are required to prevent H damaging the IGZO-channel which would in turn compromise the device performance.

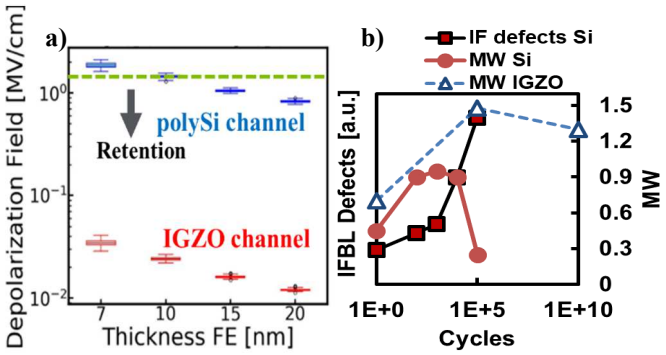

Figure 7. a) Introduction of IGZO channel reduces depolarization field tremendously and stabilizes retention behavior enabling the MLC behavior. b) Endurance degradation due to the interface destruction (poliSi-channel case), its corelation with defect generation at SiO_2 IFBL and MW prediction of IGZO-channel based V-FeFET.

V. Conclusions

In this study we report a multiscale model that captures the multigrain nature of ferroelectric HfO_x, phase-transitions defect interaction, charge trapping, ferroelectric switching and its entanglement inside the FeFET. Using the developed model, we explain wake-up and fatigue (defect generation and domain pinning); identify combination of multi-grain/phase nature of ferroelectric and polySi channel as the main variability sources of 3D NAND-like V-FeFET. We show that the endurance degradation and retention instabilities of intermediate states are the most impacted by depolarization field. Based on the understood endurance and retention dynamics we predict the endurance of V-FeFET with an oxide channel (IGZO) with reduced operation voltages 2-3x vs. conventional (poly)Si-channel FeFETs that prevents early endurance failure due to interface buffer-layer breakdown.

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