Towards a wireless micropackaged implant with hermeticity monitoring

Arthur Jaccottet*†‡, Peilong Feng*†, Katarzyna M. Szostak-Lipowicz*†, Lewis Keeble*†, Timothy G. Constandinou*†¶
*Department of Electrical and Electronic Engineering, Imperial College London, SW7 2BT, UK
†Centre for Bio-Inspired Technology, Institute of Biomedical Engineering, Imperial College London, SW7 2AZ, UK
‡Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
¶Care Research & Technology Centre, UK Dementia Research Institute, UK
Email: {arthur.jaccottet22, peilong.feng14, k.szostak, l.keeble18, t.constandinou}@imperial.ac.uk

***Abstract*—The development of reliable hermetic chip-scale micropackaging is one of the major challenges in the miniaturization of implantable medical devices. Protecting the patient from the implanted foreign body and the implant itself from the biological environment is crucial. This paper presents an implantable micropackaging concept to protect a microelectronic system-on-chip. A hermetic chamber is formed by bonding the active CMOS chip to a silicon cover using a gold-tin eutectic sealant. The cover's fabrication method and the die's post-processing steps are presented. A humidity sensor inside the chamber monitors the humidity to assess permeability. To power the sensor and read its data, interconnections in the CMOS chip have been designed; these metal tracks pass underneath the cover and thus create a connection between the inside and the outside of the cavity. As an alternative to these connections, an on-chip wireless power management and data communication system is presented with simulated results.**

I. Introduction

Thanks to advances in microtechnology and integrated circuit design, miniaturized implantable medical devices (IMDs) are becoming increasingly sophisticated and compact, offering new perspectives on medical monitoring and treatment [1]–[3]. However, the packaging of IMDs is still a significant challenge and remains relatively under-researched. These micropackages must be compact and biocompatible but also protect the implant from the human body environment. In particular, the active electronics of the implant must be hermetically sealed to prevent failure due to bodily fluids. An interesting approach, when the implant electronics consists of a single chip, is to use the chip itself as the packaging base and to protect the circuit with a cover, typically made of silicon or glass, to obtain a chip-scale hermetic packaging [3], [4]. There are several methods of sealing the cover and base; the well-established eutectic bonding is one of the most suitable for IMDs containing CMOS integrated circuits, particularly, gold-tin-based eutectic, which has been successfully used in various microelectromechanical systems packaging [5], [6].

Although hermetic packages protect and isolate the active microelectronics on-chip, electrical signals must be able to enter and exit. This is typically required for IMDs with actuators/sensors such as cochlear implants [7] or neural implants [8]. The design of these feedthroughs is a challenge as they create direct links between the inside and outside of the package and, therefore, potentially facilitate the penetration of moisture to the active electronic [9].

To reduce the number of feedthroughs, the implementation of wireless communication with the electronics inside the cavity is very promising. The electromagnetic wireless interfaces for hermetical implants are the most popular solution, particularly near-field inductive coupling [10]–[12]. Many coil coupling schemes exist. 2-coil, 3-coil, and 4-coil schemes are good at powering up a few implants with limited power coverage. Coil array schemes could supply power for many implants with a uniform power coverage [13], [14].

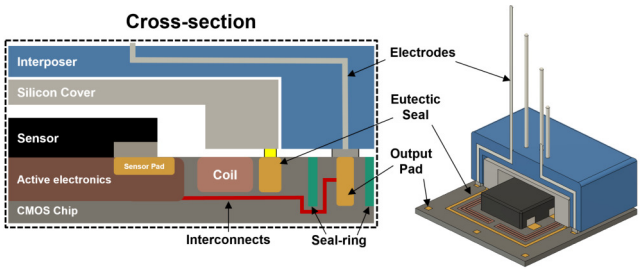


Fig. 1. Hermetic-packaging concept showing the silicon cover, humidity sensor and CMOS chip, as well as an interposer for potential connection to electrodes. Illustration not to scale.

Several approaches are possible to assess the hermeticity of packages with very small cavity volumes [15]. Using a humidity sensor is particularly interesting to have a quantitative and continuous analysis of the chamber condition and thus allow early detection of packaging failure.

This paper presents the progress to date towards a chip-scale hermetic package formed by a silicon cover bonded to a CMOS chip with an Au:Sn eutectic seal and an on-chip electromagnetic wireless interface. The micropackage has been designed to accommodate a humidity sensor, as shown in Fig. 1, to estimate its moisture permeability. The package is intended to protect microelectronics in IMDs, particularly in distributed neural implants.

II. System overview

The silicon cover and the die are assembled to form a sealed compartment using gold-tin eutectic bonding. This low-footprint sealing method was chosen because it is CMOS-compatible (processing temperature below 350 °C), biocompatible, stable, and provides good seal hermeticity [16]. The gold and tin are electroplated onto the silicon cover, while electroless deposition is used for gold on the chip after it has been post-processed.

Metal interconnections buried in the CMOS chip provide channels from the inside to the outside of the hermetic cavity. They could be used to connect multiple electrodes or have

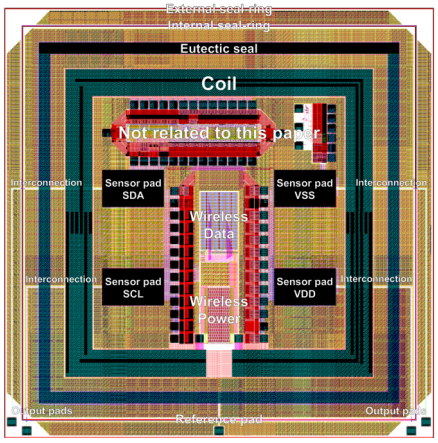


Fig. 2. CMOS chip layout with sensor pads, output pads, eutectic seal, double seal-rings, receiving coil, wireless power, and data management circuits.

external debugging ports for microelectronic systems inside the cavity. In addition, a wireless circuitry inside the package aims to supply energy and collect data from integrated microelectronic systems after devices are implanted into biological environments. The coil on the CMOS chip inductively couples electromagnetic energy from an external power transmitter.

The humidity sensor inside the package constantly monitors the working condition of the implanted microelectronic circuits or components. The buried metal tracks currently supply power and communication; in the future, the on-chip wireless system will be used for this purpose.

III. System implementation

A. CMOS chip design

The CMOS chip has been implemented in TSMC 0.18 µm CMOS technology. The annotated layout is shown in Fig. 2; overall chip dimension is $3.5 \times 3.5\,\mathrm{mm}^2$.

The sealed area is defined by a 90 μm wide pad opening (*Eutectic seal*) that surrounds the central part of the chip to be protected. This pad opening is required so the cover can be bonded with the eutectic sealant to the exposed uppermost metal. This exposed metal is connected to three metal layers underneath to ensure adhesion. In this sealed area, the chip has been designed to house the four-pin humidity sensor (*Sensirion SHT41*). Also inside the eutectic seal is the wireless power transfer and data communication microelectronic system.

In the non-protected region, outside the eutectic seal, are two seal-rings. The external seal-ring encloses the entire chip as TSMC's design rules require for the 0.18 µm technology. The inner seal-ring is an additional protection to the eutectic seal, as seal-rings can prevent unintended stress cracks during the dicing process and block moisture penetration into dies. The output pads, where the chip can be wire bonded to a printed circuit board (PCB) or connected to electrodes, are located between these two seal-rings.

There are various ways to connect these output pads and the active electronics in the chamber [3], [9], but at the chip-scale level, two methods are particularly relevant: through-silicon vias (TSVs) or interconnections in the CMOS itself. In this work, the second option is explored as the technology used to manufacture the dies does not provide TSVs and their implementation after the CMOS chip fabrication is laborious [6]. The interconnections are made of three different metal layers because they must run below the coil, the eutectic seal, and finally, the inner seal-ring (see *Cross-section* of Fig. 1).

B. CMOS chip post-processing

Back end of line (BEOL) metallization used in the chosen technology is an alloy of aluminum and copper. Aluminum surface naturally has an oxide layer of 2-3 nm, which prevents other metals from adhering to the surface [17], [18]. This native oxide must therefore be removed and prevented from reforming by plating the aluminum with gold or tin to ensure good adhesion and sealing during the eutectic bonding of the cover. A possible approach is to perform a zincate treatment, where the oxide is etched and replaced by a thin layer of zinc, followed by an electroless nickel immersion gold (ENIG) process, where nickel and gold are deposited successively [18]–[23]. This is a cost-effective and well-established solution; however, its impact on complex ICs has been studied little. Other methods are possible, such as using a sputtering system (plasma oxide removal followed by gold sputtering), using a nickel displacement bath instead of a zincate treatment [24], or electroplating gold directly onto aluminum after activation by anodizing [25]. However, these methods are not yet mature and more complicated; e.g., the first two require photolithography. Zincate/ENIG methodology is tested for the first time on the selected 0.18 μm CMOS technology to assess whether it is the best approach to prepare the chip for eutectic bonding.

The process flow is shown on the right-hand side of Fig. 3: the chip is first ultrasonically degreased in acetone, then isopropanol. The oxide layer is etched by a 5 % sodium hydroxide (NaOH) solution for 5 s then in a 50 % nitric acid (HNO_3) solution for 5 s. The deposition of zinc is performed by immersing the die in a ready-to-use solution (*Techni EN Zincate*) for 150 s. For better coverage and uniformity, a double zincate treatment is carried out [19]–[21], i.e., the first zinc layer is etched away in 50 % HNO_3 for 3 s, and a second layer is then deposited (immersion in *Techni EN Zincate* for 50 s). After that, nickel and gold can be deposited successively by dipping the chip in two commercially available solutions: *Technic EN AT 6500* (18 min) and *SuperMex 250* (25 min).

C. Silicon cover

The covers are made from 800 µm thick 4-inch silicon wafers; a simplified process flow is shown on the left-hand side of Fig. 3. After an RCA clean, the substrate is coated with 320 nm of silicon dioxide by plasma-enhanced chemical vapor deposition. A 20 nm titanium adhesion layer is then deposited, followed by a 100 nm gold layer (seed layer for subsequent electrodeposition), both by sputtering. In the next step, 1.8 μm of *MICROPOSIT S1818 G2*, a thin positive photoresist, is deposited and patterned to obtain an array of square-shaped openings corresponding to the cover cavity. The gold seed layer is first etched using a potassium iodide (KI) solution. Then, both the adhesion titanium and silicon oxide layers are etched in a hydrofluoric acid (HF) solution. After stripping the photoresist with dimethyl sulfoxide (DMSO), a second photolithography step is performed using the same mask, but a thicker photoresist; 9 μm of *MEGAPOSIT SPR220* is coated and patterned to withstand the deep reactive-ion etching

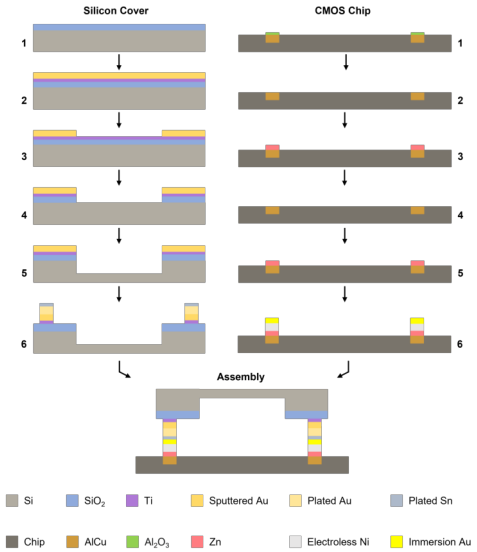


Fig. 3. Process flow for the cover fabrication and CMOS chip post-processing. Silicon cover: (1) Oxidation; (2) Ti/Au sputtering; (3) Au wet etching; (4) Ti/SiO_2 wet etching; (5) Si DRIE etching; (6) Eutectic stack electrodeposition and Ti/Au etching. CMOS chip: (2) Oxide removal; (3) 1st zincate; (4) Zn wet etching; (5) 2nd zincate; (6) Ni/Au deposition. Assembly: Eutectic bonding. Sketch not to scale.

(DRIE) of the cavity in the silicon. DMSO is used to remove the remaining resist. An array of openings in the shape of the eutectic seal is then photographically patterned in 10 μm of *AZ 15nXT (450 CPS)*, a thick negative photoresist. The eutectic stack is obtained by successive electrodeposition of gold and tin. The parameters of these electrodeposition steps are based on previous work [16], [26]. Afterward, the photoresist is stripped using *MICROPOSIT Remover 1165*. Finally, the seed and adhesion layer not protected by the eutectic stack are etched using respectively a KI solution and an HF solution.

D. Assembly

The humidity sensor is bonded to the post-processed die using a silver conductive epoxy adhesive. The cavity is then closed by bonding the cover and the chip together using a die bonder (*Lambda Fineplacer*, *Finetech*, Germany). The two parts are brought together, and a force is applied (10-40 N) before the assembly is heated. On both sides, the temperature is raised at a rate of 20 K/s until 320 °C, where the temperature is held for 10 minutes. Next, the sample is allowed to cool to room temperature [16]. Finally, the assembly can be glued and wire bonded to a PCB to interface with the sensor.

E. Wireless interface

The on-chip wireless power management and data communication system consists of a 3 $\times$ 3 mm^2 single-turn on-chip coil, an autonomous wireless power management unit, and a wireless data transmitter, as shown in Fig. 2. The power management unit and data transmitter with 26 test pads occupy 1.14 mm^2 on silicon. The on-chip coil is implemented to inductively couple electromagnetic energy from an external power transmitter. The same coil is utilized to establish communication with an external data receiver by detecting its backscattered energy. The simplified architecture of the on-chip wireless power management and data communication system is shown in Fig. 4. It contains three main

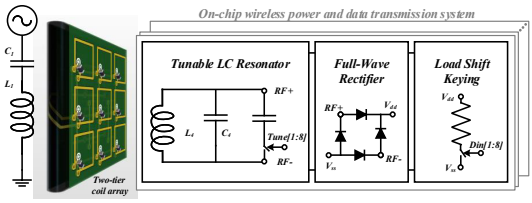


Fig. 4. Simplified schematic of on-chip wireless power management and data communication system.

blocks: tunable LC resonator, full-wave rectifier, and load shift keying circuits. The tunable LC resonator is responsible for adjusting the inductively coupled energy to achieve the best power transfer efficiency using an 8-bit digital control signal $Tune[1:8]$. The full-wave rectifier based on Schottky diodes converts differential AC voltage $RF-/+$ to a DC supply voltage V_{dd}. The data transmission performs in load shift keying circuits with an 8-bit binary-weighted resistor array to backscatter energy according to load variations.

F. Digital humidity sensor

The off-shelf humidity sensor was chosen according to several criteria. Primarily its footprint, to minimize the size of the CMOS chip, and its height, to minimize the amount of silicon to be etched in the cover. Secondly, its accuracy in terms of humidity sensing. Finally, the maximum temperature that the sensor can withstand before being irreversibly damaged since the latter must be able to tolerate the 320 °C required for the eutectic bonding of the cover and the CMOS chip.

The *Sensirion SHT41* digital humidity and temperature sensor with a footprint of 1.5 x 1.5 mm^2 and a height of 0.5 mm has been selected. The sensor relative humidity (RH) accuracy is $\pm$1.8 %RH, and an I^2C interface, via its four pins, allows easy communication. The only point of uncertainty was the *SHT41* low maximum operating temperature (125 °C).

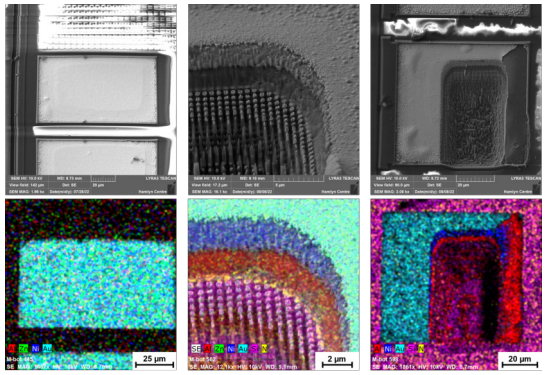
IV. Preliminary Results

A. CMOS chip post-processing

The zincate and ENIG treatment experiments were performed on test chips manufactured with the same technology as the layout presented in this work. Scanning Electron Microscopy (SEM) images with Energy Dispersive X-Ray (EDX) analysis of these tests are shown in Fig. 5.

After the entire process, a thin layer of gold was obtained on all chip pads with excellent selectivity (Fig. 5(a)). Nickel is also found after the whole process, while the zinc dissolved in the EN solution, activating the aluminum surface for nickel plating (Fig. 5(b)). The aluminum surface of each pad is gold coated, but the coating appears thicker and smoother in the middle compared to the edges. This observation can be explained by the nickel underneath the gold not extending to the edges of the pads. This issue has led to adhesion problems of the gold layer during tape adhesion tests (Fig. 5(c)). Additionally, the gold peeled off from the nickel, indicating adhesion issues at the gold-nickel and gold-aluminum interfaces. However, no Au-Ni delamination occurred without Au-Al delamination on the edges of the pads, suggesting delamination propagation from the nickel-free regions. Hence, nickel deposition must be improved as a priority.

This lack of nickel coverage on the contacts' edges is due to



(a) (b) (c)

Fig. 5. SEM images and EDX analysis of gold-plated pads and cross-sections.

greater mass transport of the stabilizers (additives to improve solution stability and plating selectivity) contained in the EN solution in these areas. Indeed, surface edges are subject to nonlinear diffusion in addition to linear diffusion on the entire surface. The increased presence of these catalytic inhibitors at the pads' edges prevents nickel deposition [27]–[29]. Optimizing their concentration should lead to better coverage.

In addition to the coverage, the thickness of nickel deposited must be increased. Surface profile measurements (*Veeco Dek-Tak 6M*) showed approximately 1.1 μm of metal deposited in total. A thickness of 2 μm is needed to obtain a gold layer above the passivation layer and hence avoid contact between the chip and the cover during bonding. On the other hand, the process did not damage the passivation layer or increase the electrical resistance of the contacts.

Overall, these results are encouraging and suggest that a good, uniform gold layer can be obtained after optimization.

B. Wireless power management

The inductive link, which contains a transmitting coil L_1, a two-tier coil array, and a receiving coil L_4, has been simulated in HFSS within a six-layer human model under various distances and misalignment scenarios between the transmitting and receiving coil. The distance from scalp to cortex is 12-20 mm [30]. Therefore, a wider distance range of 2-20 mm was applied in the electromagnetic simulations to verify that the implants could receive sufficient power in the best and worst operating situations.

Fig. 6(a) shows the power delivered to load (PDL) after AC-DC voltage rectification. The central frequency for power transfer is 433 MHz. The maximum and minimum PDL are 2.596 mW and 11.19 µW, respectively for 2 mm and 20 mm distances between L_1 and L_4. For a typical human scalp-to-cortex distance of 12 mm, the delivered power is 952.4 µW, which is safe and enough to supply energy to the humidity sensor *SHT41* working at 7.8 µW. The remaining energy budget could be used in 8-channel recording analog front-end circuits [31]. The simulated quality factor of Rx coil at 433 MHz is 8.64. Fig. 6(b) shows the power transfer efficiency (PTE) of the entire inductive link with misalignment on the X and Y axes. The maximum and minimum PTE are 12.58% and 6.38%, respectively. The average PTE over 16 mm × 16 mm is 9.81% with 4.3% power distribution deviation. This simulated power coverage is based on a 20 mm × 20 mm scalable two-tier coil array. The power coverage is expected to be extended with a scale-up coil array; however, the average PTE will slightly decrease as electromagnetic energy spreads to a larger area.

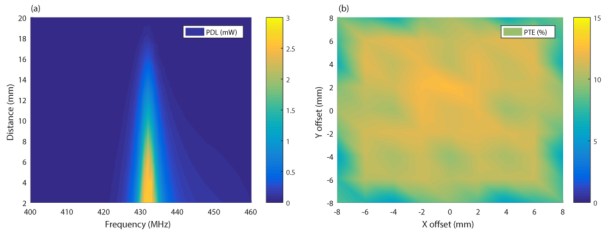


Fig. 6. Simulated PDL and PTE: (a) PDL at various frequencies and coupling distances; (b) PTE with X and Y axes misalignment.

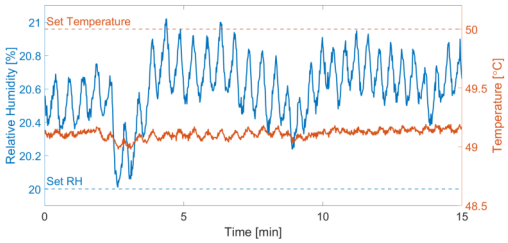


Fig. 7. Humidity and temperature measurements conducted with a sensor preheated for 10 minutes at 320 °C.

C. Digital humidity sensor testing

Tests have been carried out on the humidity sensors to ensure that they would still operate correctly after 10 minutes at an elevated temperature of 320 °C. Heated and non-heated sensors were placed in an environmental chamber (*ESPEC SH-221*) for 15 min at different temperatures (25-75 °C) and relative humidities (20-80 %). Measurements made with the heated sensor are shown in Fig. 7. The measurements of both sensors were comparable in accuracy and deviation. Additionally, despite the oscillations, the signals' average values were always close to the set conditions in the chamber. Thus, the selected sensor can withstand the temperature required to bond the cover and is suited to this application.

V. Conclusion

This work has presented the ongoing implementation of a hermetically sealed micropackage protecting the electronic circuit of a CMOS chip destined for distributed neural implants. Zincate/ENIG treatment on the chosen CMOS technology has successfully deposited gold for package assembly, but adhesion problems remain. Two ways of powering and extracting data from a humidity sensor placed in the sealed cavity have been implemented and will be further investigated. The most promising is wireless telemetry. In this work, an on-chip coil and its circuitry have been implemented. The second method, which consists of metal tracks buried in the CMOS chip, is potentially more detrimental to the hermeticity of the chip. However, it is essential to implement and test this wired approach as it is necessary for several IMDs to interface with, e.g., electrodes external to the housing [8]. Cover fabrication, post-processing optimization, and assembly are still in progress; they will be presented and discussed in more detail in subsequent publications.

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