Growth of Group IV and III-V Semiconductor Materials for Silicon Photonics: Buffer Layer and Light Source Development

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I, Hui Jia confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Signed: Hui Jia

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Abstract

High data transmission speeds, high levels of integration, and low manufacturing costs have established Si photonics as a crucial technology for next-generation data interconnects and communications systems. It involves a variety of components including light emitters, photodetectors, amplifiers, waveguides, modulators, and more. Because of its indirect bandgap, silicon is unable to serve as an efficient light source on a chip, hence this has been one of the formidable challenges. Within the framework of the monolithic approach, this thesis presents the study of two essential aspects of this challenge, the optimisation of buffer layers and development of light sources, by incorporating and improving different systems of Group IV thin films and III-V quantum dots (QDs) semiconductor materials.

The monolithic approach focuses on the direct epitaxial growth of highly efficient light sources, usually by the epitaxy of III-V semiconductors lasers on a single Si chip. However, because of the material dissimilarities between III-V materials and Si, during the heteroepitaxy, a high density of crystalline defects such as threading dislocations (TDs), thermal cracks and anti-phase domains are introduced, severely impeding the performance and yield of the laser. For instance, TDs act as non-radiative recombination centres, while thermal cracks cause issues with the efficient evanescent coupling of the emitted light with Si waveguide. To address these defects, typically complex buffer growth techniques with micron-scale thickness are employed.

The research in this thesis is divided into two parts, namely buffer layer optimisation and light source development. Each part outlines alternative strategies for overcoming the above-mentioned hurdles for monolithic growth. The first part highlights the optimisation of buffer layer growth to reduce threading dislocations for the monolithic integration of high-performance direct-bandgap III-V and group IV light sources on Si.

The growth optimisation of low defect-density Ge buffer layers epitaxially grown on Si was first investigated. Defect elimination in Ge buffers with doped and undoped seed layers of increasing total thickness is studied under a variety of growth regimes, doping techniques, and annealing processes. This study demonstrates that a 500 nm thin Ge achieves the same defect level (1.3×10^8 cm $^{-2}$) as 2.2 μm GaAs grown on Si, which greatly increases the thickness budget for the subsequent dislocation filter layers (DFLs) and laser structure growth before the formation of thermal cracks.

Meanwhile, a low threading dislocation density of 3.3×10^7 cm $^{-2}$ is obtained for 1 μm Ge grown on Si.

The second part places emphasis on the development of light sources in the near-infrared wavelength range for Si photonics.

1) The development of GeSn, an emerging direct bandgap light source for Si photonics, is shown, which has wide bandgap tuneability and full compatibility with Si complementary metal-oxide semiconductor (CMOS). Growing the high Sn composition of GeSn required for efficient light generation is challenging and its growth generally severely affected by large surface roughness and Sn segregation. In this work, first, ex-situ rapid thermal annealing for the grown GeSn layer is investigated, showing that by proper annealing the strain can be relaxed by 90% without intriguing Sn segregation. This method shows its potential for both material growth and device fabrication. Besides, strain compensated layer and in-situ annealing techniques have been developed. Significantly improved surface quality has been confirmed by in-situ reflection high-energy electron diffraction (RHEED) observations and atomic force microscopy (AFM) images. Transmission electron microscopy (TEM) results reveal the high crystal quality of the multiple quantum wells (MQWs) grown on such buffer layers.
2) The final section details the development of InAs/InP QDs emitting near the strategic 1.55 μm, the lowest optical fibre loss window. The InAs/InP QDs growth is prone to inhomogeneous quantum dash morphologies which broaden the photoluminescence (PL) spectra and degrade the carrier confinement. Research has been conducted on growth parameters and techniques including deposition thickness, growth temperature and Indium-flush technique is applied to improve the uniformity of the dots, and narrow room temperature PL linewidths of 47.9 meV and 50.9 meV have been achieved for single-layer and five-layer quantum dot samples, respectively. The structures enable the fabrication of small footprint microdisk lasers with lasing thresholds as low as 30 μW.

Impact Statement

Research on Group-IV thin films and III-V QD semiconductor materials presented in this thesis has enabled establishment of optimal material parameters for the monolithic integration of efficient light sources on Si for Si photonics. Si photonics is the key for achieving optical interconnections. The very-large-scale-integration in Si photonics allows the integration of both electronic and photonic devices on a single chip, featuring low-cost and mass production. Multifunctional photonic devices can be integrated on a single chip by utilising resources of well-established Si microelectronics industry.

The research in this thesis would have a significant impact on the monolithic integration of Si photonics. The realisation of thin low-defect-density Ge/Si provides a feasible platform for both III-V and Group-IV-based semiconductor devices to be integrated on Si. The thin buffer layer thickness potentially avoids the formation of thermal cracks fatal to device performance and allow for more space for the growth optimisation of upper active region material. The investigations of the thermal stability and the novel growth technique developed for GeSn will have an impact on the development of all-Group-IV optoelectronic devices integrated on Si. GeSn is an important material for Si photonics because it can be a direct-bandgap material and the bandgap can be tuned into mid-infrared (mid-IR) range by composition or strain variation, allowing plenty of manipulation potential. Availability of low-cost, high - performance mid-IR lasers and photodetectors would have important impact on developments in materials processing, biochemical, chemical industries. The realisation of highly-uniform C-band InAs/InP QDs presents outstanding advantages on carrier confinement, temperature stability and tolerance to defects, and will find wide range of applications in long-haul communication, eye-safe LiDARs for automotives and sensing applications. The demonstrated long-wavelength lasers with a low threshold and ultracompact footprint can impact in integrated gas detection and highly localized label-free biological and biochemical sensing.

List of publications

1. Yu, Xuezhe, **Hui Jia**, Calum Dear, Jiajing Yuan, Huiwen Deng, Mingchu Tang, and Huiyun Liu. "Optically Enhanced Single-and Multi-Stacked 1.55 μm InAs/InAlGaAs/InP Quantum Dots for Laser Applications." *Journal of Physics D: Applied Physics* 56, no. 28 (2023): 285101.

2. **Jia, Hui**, Xuezhe Yu, Taojie Zhou, Calum Dear, Jiajing Yuan, Mingchu Tang, Zhao Yan, Bogdan-Petrin Ratiu, Qiang Li, and Alwyn Seeds. "Long-Wavelength InAs/InAlGaAs Quantum Dot Microdisk Lasers on InP (001) Substrate." *Applied physics letters* 122, no. 11 (2023): 111108.

3. **Jia, Hui**, Junjie Yang, Mingchu Tang, Wei Li, Pamela Jurczak, Xuezhe Yu, Taojie Zhou, Jae-Seong Park, Keshuang Li, and Huiwen Deng. "The Epitaxial Growth and Unique Morphology of InAs Quantum Dots Embedded in a Ge Matrix." *Journal of Physics D: Applied Physics* 55, no. 49 (2022): 494002.

4. **Jia, Hui**, Pamela Jurczak, Junjie Yang, Mingchu Tang, Keshuang Li, Huiwen Deng, Manyu Dang, Siming Chen, and Huiyun Liu. "Impact of Ex-Situ Annealing on Strain and Composition of MBE Grown GeSn." *Journal of Physics D: Applied Physics* 53, no. 48 (2020): 485104.

5. Hou, Yaonan, Ilias Skandalos, Mingchu Tang, **Hui Jia**, Huiwen Deng, Xuezhe Yu, Yasir Noori, Spyros Stathopoulos, Siming Chen, and Huiyun Liu. "Surface/Interface Engineering of Inas Quantum Dot Edge-Emitting Diodes toward III-V/SiN Photonic Integration." *Journal of Luminescence* 258 (2023): 119799.

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InAs/InAsSb Type-II Superlattices Grown on Silicon by MOCVD." *Journal of Crystal Growth* 598 (2022): 126860.

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8. Hou, Yaonan, **Hui Jia**, Mingchu Tang, Aleksander Buseth Mosberg, Quentin M Ramasse, Ilias Skandalos, Yasir Noori, Junjie Yang, Huiyun Liu, and Alwyn Seeds. "A Thermally Erasable Silicon Oxide Layer for Molecular Beam Epitaxy." *Journal of Physics D: Applied Physics* 55, no. 42 (2022): 424004.

9. Yang, Junjie, Keshuang Li, **Hui Jia**, Huiwen Deng, Xuezhe Yu, Pamela Jurczak, Jae-Seong Park, Shujie Pan, Wei Li, and Siming Chen. "Low Threading Dislocation Density and Antiphase Boundary Free Gaas Epitaxially Grown on on-Axis Si (001) Substrates." *Nanoscale* 14, no. 46 (2022): 17247-53.

10. Yu, Xuezhe, Keshuang Li, Junjie Yang, Ying Lu, Zizhuo Liu, Mingchu Tang, Pamela Jurczak, Jae-Seong Park, Huiwen Deng, and **Hui Jia**. *Inversion Boundary Annihilation in GaAs Grown on on-Axis Silicon (001) Via Molecular Beam Epitaxy*. Vol. 11880. Emerging Applications in Silicon Photonics II: SPIE, 2021.

11. Li, Keshuang, Junjie Yang, Ying Lu, Mingchu Tang, Pamela Jurczak, Zizhuo Liu, Xuezhe Yu, Jae-Seong Park, Huiwen Deng, and **Hui Jia**. "Inversion Boundary Annihilation in GaAs Monolithically Grown on on-Axis Silicon (001)." *Advanced Optical Materials* 8, no. 22 (2020): 2000970.

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Chapter 1.

Introduction

1.1 Silicon Photonics

The worldwide internet penetration and network capacity have expanded exponentially over the last years. It is predicted that by 2023, nearly two-thirds of the global population will have Internet access and half of all connected devices will be used for Machine-To-Machine (M2M) applications, with connected home applications accounting for the largest share, and connected car applications growing at the fastest rate [1, 2]. An extraordinary amount of nearly a thousand zettabytes data will be generated by all people, machines, and things per year [3]. Under this development of the unprecedented expansion in demand for the data transmission, traditional copper interconnects will be no longer sufficient to fulfil the requirements of data throughput from the essence of copper's inherent limitation that can only transmit the information carried by the movement of electrons. In copper interconnects, the presence of cross-talk, frequency-dependent propagation loss, and return loss significantly impedes the data transmission rate and scaling flexibility [4]; moreover, power dissipation through heat generation is inevitable, which on the one hand increases the power consumption in the data centres, and on the other hand introduces additional cost for energy loss and requires more space for cooling systems. In contrast, optical interconnects entail

the development of optoelectronic transceivers for generating data for transmission, receiving or converting them to electronic data for storage in the chip or processing [5] with a very low loss [4]. To some extent, this could be perceivable from the fact that the loss for a single-mode fibre is merely ~ 0.4 dB/km and 0.25 dB/km at 1.3 μm and 1.55 μm, respectively [4]. In addition to minimal signal loss, optical interconnect is also intrinsically appropriate for multiple channel data transmission thanks to the wealth of information types that light can convey within a single optical fibre, such as different wavelengths, modes, and polarisations. With the help of wavelength division multiplexing and de-multiplexing, coexistence of multiple channels can be supported within the same fibre, allowing for channel-specific material savings while concurrently enhancing data throughput. High-speed modulation is another advantageous feature of optical interconnects realised by the ultra-low carrier recombination lifetime [6]. As a result, optical fibres that link chips, data centres, core networks, public clouds and mobile access points across local areas have become the backbone of the today's communication network infrastructure.

However, as opposite to the well-established Si-based electronics technology that can streamline billions of cells into a single chip, photonic devices are usually discrete components that requires sequences of fabrication. To fully capitalise on the optical interconnects as well as the maturity of the Si-based electronics mass-production platform, Si photonics has emerged and is rapidly developing [7, 8]. Si platforms not only present commercial benefits in terms of large wafer size, volume throughput and cost reduction, but they are also advantageous in their native oxide SiO_2, which provides excellent refractive index contrast and high-quality interface, essential for the strong optical confinement [9]. Additionally, Si substrates are superior in heat dissipation.

The term "Si photonics" refers to the practise of integrating different photonic components such as light emitters, photodetectors, amplifiers, waveguides, modulators, and more, all on a single silicon-on-insulator (SOI) platform partially or as a whole, where the fabrication infrastructure is highly accurate, robust and compatible with CMOS technology [8]. Indeed, the high data transmission rates, high levels of integration, and low manufacturing costs have established Si photonics as a crucial technology for next-generation data interconnects and communications systems [6].

As the surge of interests in Si photonics being driven by both academia and industry, the past three decades have witnessed its significant advancement in the majority of

the discrete critical components, including high-bandwidth photodetectors [10], ultra-fast modulators [11] and low-loss waveguides [12]. The viability of commercial solutions, such as 100Gb/s transceiver, have been successfully proven by pioneering companies [13]. However, an efficient electrically pumped Si-based light source remains the last missing piece in Si photonics, which is a challenging gap to fill given the indirect-bandgap nature of the widely used Si and Ge in integrated circuits. As indirect bandgap materials, the conduction band minimum is not aligned with their valance band maximum. In this case, when generating a photon by carrier recombination, an extra particle is needed to carry the excess momentum from the perspective of momentum conservation law, rendering the process inefficient. To achieve efficient, integratable Si-based on-chip light sources, mainly two key types of attempts have been made:

1. Manipulating the methods of light-generation of the significant group-IV semiconductor Si and Ge. Both have been used extensively in photonic integrated circuits (PICs). In particular, the lowest energy L-valley of Ge is only 136 meV lower than its Γ-valley, hence research on the latter has concentrated on band structure engineering. In this vein, successful demonstrations include Si Raman lasers, Ge and GeSn lasers. Although an electrically pumped Ge laser has been realised on Si *via* heavy n-type doping, it presents a high lasing threshold of 280 kA cm^{-2} owing to losses imposed by free carriers at high doping level and also driven by interactions with electrical contacts [14]. Alloying with Sn to achieve direct bandgap is another promising approach for realising efficient light emitters on Si. Followed by the first demonstration of GeSn laser in 2015, which has a high lasing threshold of 325 kA cm^{-2} [15], soon in 2020, a successful demonstration of electrically-pumped GeSn laser could operate at 100 K with a three orders of magnitude decrease of lasing threshold of 598 A/cm^2 at 10 K compared with that of the first Ge laser [16]. Although the laser performance is not yet at the level required for the practical applications in PICs, the emergence and development of these group-IV lasers opens a new pathway towards low-cost, monolithically integrated, Si-based optical components with a wide scope for advancement. A detailed literature review on group-IV lasers will be presented in section 1.3.

2. In stark contrast to Si and Ge, direct-bandgap III-V compound semiconductor materials such as InAs, GaAs and InP, show inherent superiorities in light generation. Consequently, the employment of III-V light sources for Si photonics is a natural

consideration for academia and industry. So far, a number of approaches have been implemented to achieve high performance of monolithic integration of III-V materials on Si platform with a capability of low-cost and high scalability. One of the earliest and relatively well-developed approaches is photonic integration on a silicon-on-insulator (SOI) platform, where an external III-V laser is coupled to the photonic chip and interacts with other devices created from Si device layers, for instance, with selectively grown Ge functioning as photodetectors [17]. Numerous foundries have been able to deliver rather complete suites of technologies established on this platform, including IMEC, AIM Photonics, Global Foundries, etc. [18]. Such monolithic Si photonic integration with an external light source features high-performance passive devices as well as laser sources, presenting a sophisticated level of integration with a high yield, and benefiting from the testing and packaging of Si PIC. Simple photonic packaging design kits have already been adopted at a software level and the packaging design rules are expected to be extended and formalised into standards and rolled in to the design rule checking at Si-foundries over time [19]. However, the overall performance is not only dependent on the individual components. Even if a decent die can be applied as a light source, coupling losses can significantly impede the circuit efficiency in general. Taking into account the laser-to-fibre losses and fibre-to-SOI coupling losses, a typical value of 2 – 8 dB will be introduced for off-chip lasers connected to Si photonic chips, which is significantly higher than on-chip light sources such as heterogeneously integrated lasers *via* wafer bonding or transfer printing, as well as III-V lasers grown epitaxially on Si [18]. In addition, the separate processes for PICs and laser, redundant testing before and after the attachment of the off-chip laser, and the requirement of hermetic packaging and isolator make this solution less favourable in the long term.

On-chip light sources made possible *via* a variety of bonding processes and transfer printing represent alternatives, each with its own benefits and shortcomings. This approach, also known as heterogeneous integration, entails the epitaxial development of highly efficient III-V lasers on their native substrates, followed by the transfer of the lasers, detached from the native substrates, and attached to SOI or Si (by bonding or transfer printing). The implementation of wafer-bonding to realise Si-based lasers dates to early times. Initially, the roadblock of wafer bonding is the adhesion issue in a regime where the thermal budget for integration process should not exceed 400 °C considering the compatibility with very-large-scale integrations (VLSI). Therefore, it

was not until 1996 that continuous-wave CW electrically-pumped InGaAsP lasers were successfully built on Si substrates *via* direct wafer bonding with improved adhesion brought by pressure-assisted low temperature annealing [20]. In 2005, nine years later, the first evanescently coupled optically pumped C-band laser was enabled in SOI substrate by low temperature oxygen plasma assisted wafer bonding [21]. The cross-sectional device structure is shown below in Figure 1-1 (a). The optical gain of the InAlGaAs quantum wells (QWs) is primarily preserved by the low temperature annealing process and, owing to the reduced vertical distance between the QWs and Si waveguide, the light lasing from former can be evanescently coupled to the latter. Only one year later in 2006, the first electrically pumped evanescent AlGaInAs continuous-wave laser was integrated on Si by the same group, as shown in Figure 1-1 (b) [22]. With laser cavity solely defined by the Si waveguide, hundreds of electrically driven lasers can be bonded to the Si substrate with a single bonding step. Developed lately, transfer printing is a micro-manipulation technique employed for heterogeneous integration [23]. This technique essentially necessitates the pre-processing of the III-V components, *i.e.* the naming of “coupons”, which are then picked and placed on the target substrate by an elastomeric stamp [23, 24]. There is a direct correlation between the rate with which the stamp is removed from the coupon, and the strength of the adhesion formed between the two. The faster the movement, the stronger the bond [24]. The illustrative diagram for a typical transfer printing technique of an III-V coupon integrated onto an SOI substrate is presented in Figure 1-2. Thanks to the capability of the transfer in parallel and the flexibility of in-plane movement, III-V lasers can be aligned directly on the Si window of the SOI substrate to ensure superior thermal dissipation. The coupon is generated by processing the lasers on native III-V substrates, which allows for a significant reduction in the amount of source material. On the other hand, it is conceivable to systematically integrate a range of active or passive components from many substrate sources onto the same target substrate. However, in general, heterogeneous integration suffers from two main issues that offset its benefits: (1) The implementation of III-V wafer dicing and bonding raises the total cost; (2) the throughput of the bonding lasers affects the entire package [18].

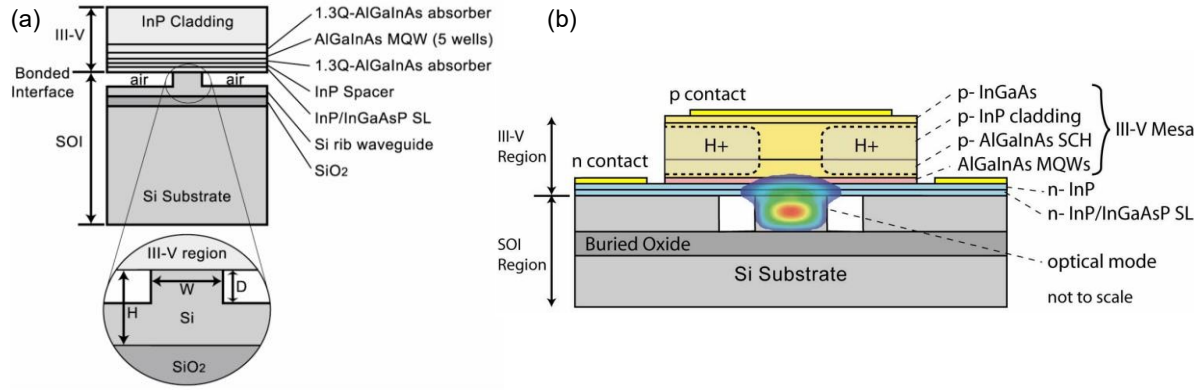

Figure 1-1 (a) Cross-sectional device structure of evanescently coupled laser on SOI substrate enabled by wafer bonding [21]. (b) Schematic illustration of the electrically-driven hybrid laser structure achieved by wafer bonding with the optical mode superimposed [22].

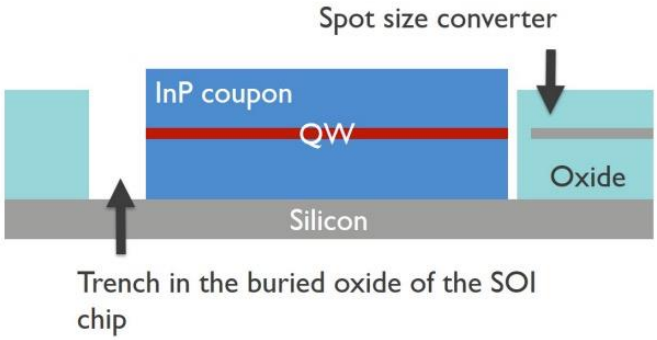

Figure 1-2 Cross-sectional illustration of III-V coupons transfer printed directly on the Si window in the SOI substrate [24].

A potential solution to the aforementioned challenges is epitaxial growth of III-V on Si or SOI substrates, which offers the advantages of cost-effectiveness and comparable or even better device performance. When compared to bonding (or transfer printing) approach, it further benefits from the following: 1) it eliminates the active-passive coupling loss inherent in the complex bonding fabrication and alignment processes in heterogeneous integration; 2) the cost of Si wafers is an order of magnitude less than that of their III-V counterparts; 3) silicon has a larger wafer size that facilitates scaling demands, both shown in Figure 1-3. SOI substrate is approximately ten times more expensive than Si substrate, but the advantage lies in that it provides a solution for the efficient, on-chip light coupling with the Si waveguide and high-density integration. Furthermore, the thermal dissipation can be improved by depositing the III-V laser on the Si window of the SOI substrate. Over the last two decades, the efficiency and reliability of Si-based epitaxial lasers have improved considerably [14, 25]. More recently, researchers have shifted their focus further forward to the III-V lasers on Si coupling with Si-based waveguides for future scalable,

low-cost, and high-density photonic integration. Figure 1-4 shows a cutting-edge electrically pumped III-V laser that was epitaxially built on a SOI substrate with edge butt-coupled waveguide for efficient light coupling [26]. It is foreseeable that, as a result of these research advances, the epitaxial growth of III-V on Si substrates is likely continuing to thrive in terms of device performance and large-scale integration.

Approximate growth substrate minimum cost and maximum size

	InAs	InP	GaAs	SOI	Si
Minimum Growth Substrate Cost ($/cm^2)	18.25	4.55	1.65	1.30	0.12
Maximum size (mm)	76	150	200	450	450

Figure 1-3 A comparison of substrate costs and maximum available sizes [27].

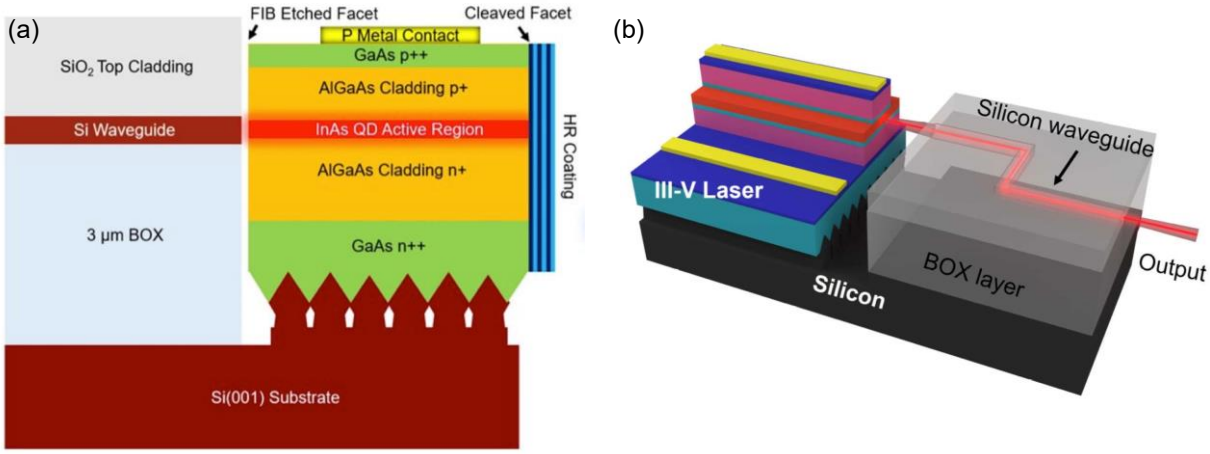

Figure 1-4 (a) Epitaxial structure of the III-V laser; (b) Schematic diagram of the III-V laser edge-coupled with Si waveguide on a SOI substrate [26].

1.2 The heteroepitaxy of III-V Materials on Si

1.2.1 Overview of challenges of growing high-quality III-V materials on Si

The epitaxial growth of III-V material on Si remains challenging because of the material dissimilarities between them, mainly: 1) the growth of a polar material on a non-polar substrate, which can generate antiphase boundaries (APBs); 2) the large

lattice mismatch between Si and III-V materials, which leads to the formation of high density (in the range of 10^{10} cm^{-2}) threading dislocations (TDs); 3) different coefficients of thermal expansion that lead to the accumulation of thermal stress during the warm-up and cooling processes of the growth, which may ultimately result in the formation of micro-cracks. These crystal defects will act as non-radiative recombination centres depleting carriers for lasing, and therefore should be diminished to the largest extent for the development of high-performance III-V devices on Si. The formation of these crystal defects as well as methods to eliminate them are included in the following parts of section 1.2.

1.2.2 Antiphase boundaries

APBs are planar crystal defects appeared in the heteroepitaxial growth of III-V materials on Si, which originate from the polar growth on nonpolar substrates in essence. For Si atoms in a crystalline Si structure, the most stable state is achieved when each Si atom is boned to four other Si atoms with two above and two below itself. However, surface Si atoms are not in the most energetically favourable state as they lack two atoms above to bond. Adjacent Si atoms thus bond with each other to reduce the number of unfulfilled bonds. They are pulled towards each other and leave the diamond lattice positions during the dimerisation. Rows of Si atom pairs on the surface are called dimer rows. For an exact Si (001) substrate surface, it generally reveals a mono-atomic stepped (also called single-layer steps) morphology because it has the lowest formation energy [28]. Because of the symmetry of the diamond structure, the terraces consist of alternating A-type straight steps and B-type ragged steps, running perpendicular and parallel to the dimer rows of the upper terrace, respectively, and corresponding to the different sublattices of the diamond structure [29, 30]. An illustrative demonstration of the two types of single-layer step is shown in Figure 1-5. Open circles denote Si atoms with unfulfilled bonds and shaded circles are fully fulfilled Si atoms. Atoms from the upper terrace are assigned with larger circles. Figure 1-5 (a) represents the configuration of A-type single-layer step (S_A), where the step edge is perpendicular to the dimer row in the upper terrace. This dimer row alignment is called a (2 × 1) dimerisation. Figure 1-5 (b) depicts B-type single-layer step (S_B) with step edge parallel to upper terrace. This is called a (1 × 2) dimerisation. An AFM image of an on-axis Si (001) surface presenting alternative straight S_A and meandering S_B single steps is shown in Figure 1-5 (c). The schematic diagram of 2 × 1 and 1 × 2 dimerisations on S_A and S_B terraces are shown in Figure 1-5 (d).

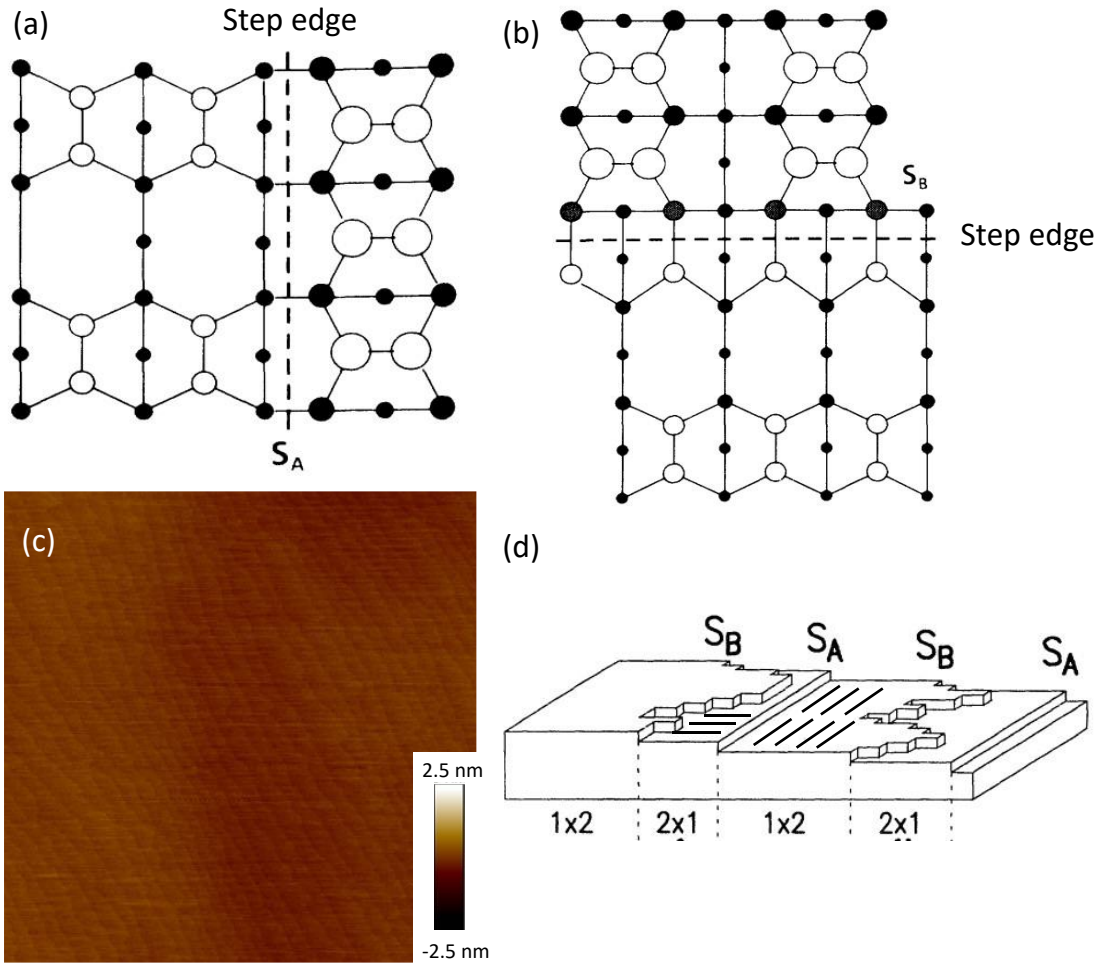

Figure 1-5 Illustrative top views of A-type (a) and B-type (b) singles steps. The dashed lines label the step edges. Open circles denote atoms with dangling bonds [28]. (c) AFM image of an on-axis Si (001) surface presenting alternative straight S_A and meandering S_B single steps. (d) A schematic diagram of 2 × 1 and 1 × 2 dimerisations on S_A and S_B terraces, respectively [31, 32].

On the other hand, zinc-blende structure III-V materials such as GaAs and InP are two atom systems where the sublattices are occupied by different atoms. At the step edges, the change in atom arrangement results in the initialisation of APBs. An illustrative figure showing the formation of APBs of GaP grown on Si (001) substrate as an example can be seen in Figure 1-6(a). APBs consisting of III-III bonds and/or V-V bonds formed in the {111} and {110} are commonly found in III-V heteroepitaxy on non-polar substrates, although the formation of these bonds are energetically unfavourable [30]. Therefore, the generation of APB usually happens when depositing polar III-V materials on non-polar Si or Ge (virtual) substrates, not necessarily the other way around. The APB annihilation is possible when two APBs in the {111} plane cross each other, as can be seen in Figure 1-6(a). In other cases APBs can also propagate in the original {110} plane or higher index planes such as {112} and {113} planes [33] in the mid-temperature and high-temperature growth stage, then either annihilate or

reach the surface. The surface morphology of APBs terminating at the surface characterised by AFM is shown in Figure 1-6(b). It demonstrates that the surface is divided by different domains enclosed by APBs, where these domains are called antiphase domains. In figure 1-6(c), the cross-sectional TEM image shows self-annihilated and propagating APBs to the surface in a 1 μm thick GaAs grown on exact Si (001). The III-III and V-V bonds in APBs are electrically charged crystal defects that act as electric leakage path, therefore is extremely detrimental to the device performance. Indeed, the existence of APBs potentially prevents the function of the devices decisively.

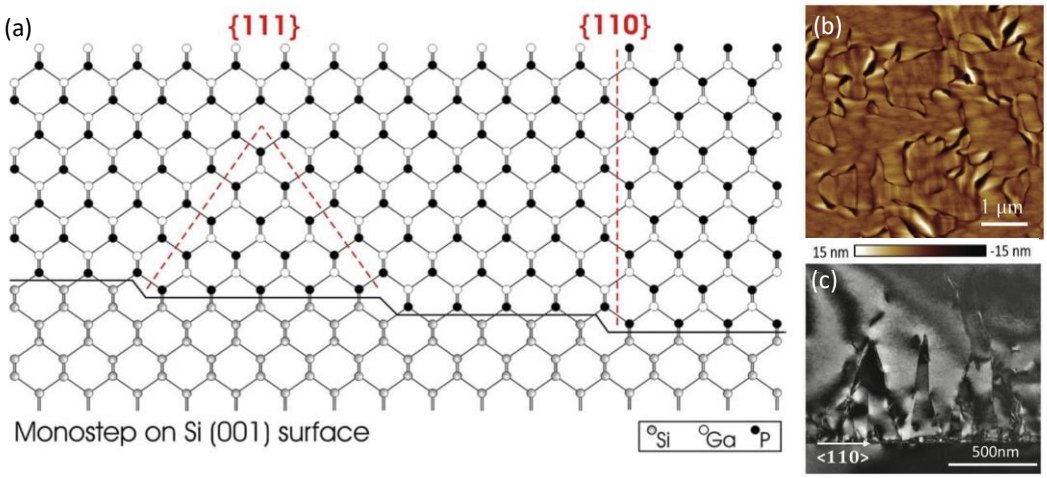

Figure 1-6 (a) An illustrative image of the formation of APBs on mono-stepped Si (001) substrate [29]; (b) 5 μm × 5 μm AFM image of 500 nm GaAs grown on exact Si (001) substrate, showing APB morphology reaching the surface and (c) Cross-sectional TEM image of 1 μm GaAs grown on exact Si (001) substrate, revealing the annihilated and propagating APBs towards the surface [34].

To avoid the formation of APBs, misoriented-Si substrates with an offcut angle of 4° or slightly larger are implemented widely, as single domain double-atomic steps are energetically favourable to be reconstructed on the offcut surface [28], which is primarily effective in APB annihilation. High performance III-V lasers have been successfully demonstrated on such offcut Si substrates [25, 35, 36]. However, exact Si (001) substrates are preferred technologically over offcut substrates as they are CMOS compatible and standard for photonic integration [37]. As a result, recent years have witnessed the growing research interest in realising high quality III-V materials grown on on-axis Si (001) substrates. Most recently, Li *et al* has developed a high-temperature-annealing-induced periodic straight and meandering single atomic height steps Si buffer layer effective for the annihilation of APBs based on which electrically pumped quantum-dot (QD) laser has been successfully demonstrated with a maximum operation temperature of 120 °C [34]. Shortly after that, the mechanism

behind the APB annihilation of this method with improved growth procedures was introduced by Yang *et al* [38]. Apart from the high-temperature-annealed Si buffer layer, a low-temperature AlGaAs nucleation layer and a temperature-ramp GaAs growth procedure are performed to help further enhance the annihilation process. The temperature increase during the GaAs growth encourages the neighbouring high index plane APBs to move towards and then annihilate with each other because of the different growth rates of the distinct GaAs phases [38].

1.2.3 Micro-cracks

Another common type of crystal defect in heteroepitaxy is thermally induced micro-cracks Because of the huge thermal expansion coefficient mismatches between the deposited material and the substrate, e.g., 5.73×10^{-6} °C^{-1} and 2.60×10^{-6} °C^{-1} for GaAs and Si, respectively, thermal strain will be generated and stored in the epilayers during the cooling process, and eventually lead to the formation of micro-cracks. These micro-cracks generate new surfaces and greatly relax the local thermal stress in the epitaxial film [39]. Figure 1-7 (a) and (b) show the plan-view electron channelling contrast images (ECCI) of a typical InAs/GaAs quantum dot laser structure grown on a Si substrate with GaAs buffer layers and dislocation filter layers of a total thickness of 5.8 μm. Orthogonal microcracks can be easily observed across the surface with spacings of several tens of microns. These microcracks penetrate the whole active region vertically, depleting carriers for lasing and therefore are fatal to device performance.

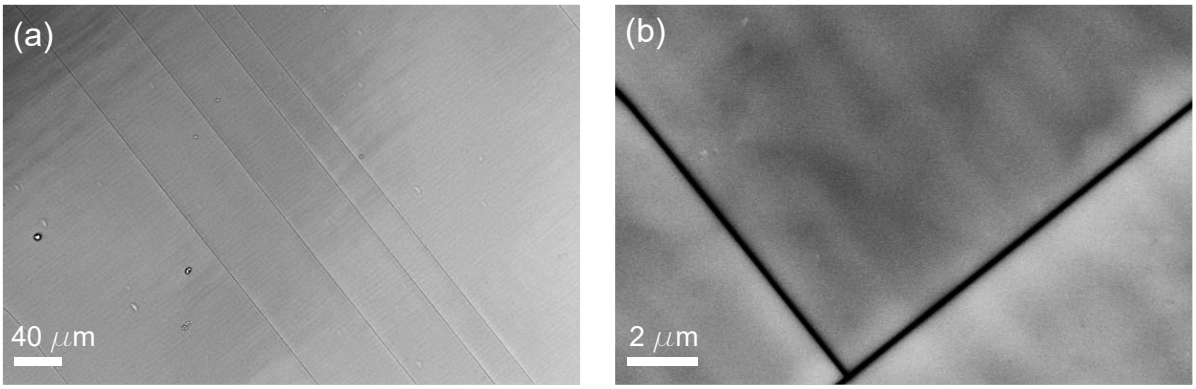

Figure 1-7. An example of cracks formed in a typical InAs/GaAs quantum dot stack including GaAs buffer layers and dislocation filter layers on Si. The total thickness is 5.8 μm. (a) and (b) are lower and higher magnification ECCI images of such surfaces.

As the critical thickness for thermally driven micro-crack formation is closely related to the extent of thermal mismatch, from the theoretical and experimental work previously, the critical value for GaAs growth on Si is around 5 μm. The epitaxial

structure design for the buffer layers and optoelectronic devices therefore has to control the overall thickness to avoid the micro-crack formation [40]. In addition, reducing the cooling rate from the growth conditions can potentially dilute the concentration of stress. Other methods such as growing strain-balance buffer layers have also been attempted and gained some success, but not well explored so far [41].

1.2.4 Misfit Dislocations and Threading Dislocations (TDs)

1.2.4.1 The Formation and Interaction of TDs

In the heteroepitaxy of lattice mismatch materials, the existence of dislocations originates from the periodic nature of the crystalline structure as the overlying epilayer replicating the crystal structure including any defects that cross the original surface of the layer [42]. When a crystalline material different from the substrate is grown, within a certain thickness, which is named as 'critical thickness', the deposited material is coherently strained to match the substrate lattice parameter as it has insufficient elastic strain energy to produce any dislocations, as schematically shown in Figure 1-8 (a). However, above this critical thickness the formation of misfit dislocations is energetically preferential to relax some of the misfit strain in the layer (Figure 1-8 (b)). The most common two types of misfit dislocations are 60° dislocation and pure edge dislocation. As the name suggests, 60° dislocations have a Burgers vector lying at 60° to the <110> line direction and pure edge dislocations have Burgers vector lies in the interface at a right angle to the dislocation line direction. Once the dislocations are formed, climb and glide are the two ways for them to move [42]. Climb involves the addition or removal of atoms at the dislocation core and only happens to a significant extent at temperatures close to the melting point of the material. In contrast, glide conserves the lattice and takes place on planes containing the Burgers vector, and can happen at relatively lower temperatures, therefore is more important in the growth of strained semiconductor layers. In addition, because of the strongly directional bonding between atoms, there exists a barrier (Peierls barrier) for dislocations to glide, resulting in the frequent occurrence of certain dislocation line directions, such as <110> or <112>, as few bonds need to be broken per unit length of dislocation. In semiconductor materials with a face-centred-cubic lattice, usual glide planes are {111} planes. The (a/2) $[0\bar{1}1]$ components of the 60° dislocations can easily propagate with a threading segment on {111} plane, therefore are called glissile dislocations. The threading segments of 60° dislocations are called TDs. For pure edge dislocations whose Burgers vector are not aligned in {111} plane, the Peierls barrier is so high that

except for moving through climb they may be regarded as sessile dislocations. This also means pure edge dislocations are favourable for heteroepitaxial growth as they can partially relax the misfit strain and will not affect the active region.

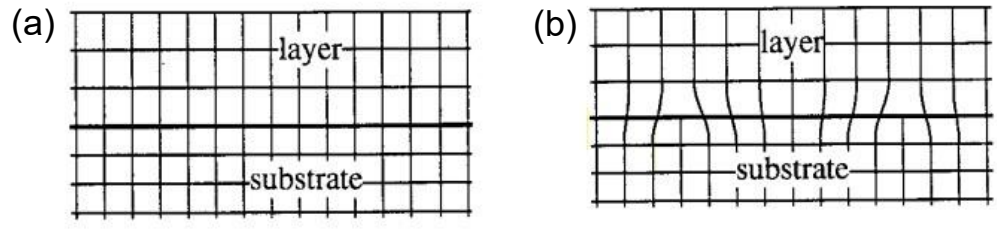

Figure 1-8. Schematic illustration of an epitaxial layer on a substrate of different material under compression: (a) a pseudomorphic (fully strained) layer and (b) a partially relaxed layer through the generation of misfit dislocations [42].

Apart from the original dislocations either duplicated from the substrate dislocations, or generated through the impurities from the chamber or imperfections of the substrate surface or nucleated during growth from the misfit strain between the layers, dislocation interactions provide another major source of high dislocation densities [43]. Once the misfit dislocations are generated, they cannot terminate inside the crystal, instead, they must either run out to the very edges of the layer or have threading segments that end up at the surface or the interface or form a closed loop. In a system where substantial misfit dislocations are forming, 60° dislocations owning the same-sigh Burgers vector will repel each other during the generation process resulting in two free-ended TD segments which can glide to create additional misfit dislocation length in the interface. In addition, if these two 60° dislocations are from different planes, their intersection can induce the formation of two angular dislocations and the decomposition of which promotes the TD multiplication [44]. While on the other hand, opposite-sign Burgers vector 60° dislocations can attract each other and either result in an annihilation or the generation of a new TD. In diamond and zinc-blende structures, this new TD can be an edge dislocation which retarding the threading segments from reaching a free edge. Among all these TD interactions, it can be concluded that the most beneficial encounter of TDs is the annihilation type. If the defective heteroepitaxial interface is less important for the subsequent growth, then generating a new edge dislocation is also a desirable approach.

1.2.4.2 Methods for Reducing TD Density

TDs are considered as the most detrimental factor for the performance and reliability of laser devices [45]. They act as nonradiative recombination centres depleting

carriers for lasing and penetrate through the whole epitaxial layers. A quantitative example is given that the lifetime of the MBE grown InAs QD lasers can be increased from 800 hours to 10000000 hours at room temperature by eliminating the TD density from $3 \times 10^8 cm^{-2}$ to $7 \times 10^6 cm^{-2}$ [46]. As the TD density in epitaxially grown III-V layers on Si substrates is in the range of 10^9 ~ 10^{10} cm^{-2}, which is much higher than that of the native substrates, usually being between 10^3 and 10^4 cm^{-2}, TD density has to be reduced for saving the device performance. The strategies for eliminating TD density fall predominantly into three categories: reducing the formation of TDs, enhancing the TD annihilation, and changing the direction of TD propagation. As TDs are formed at thicknesses exceeding the critical thickness, which are the very initial stage of the growth, special considerations must be paid to avoid their formation. Two-step growth is usually used for heteroepitaxy, where a low growth temperature is used for the initial nucleation layer to suppress the formation of three-dimensional islands, whose relaxation will lead to the formation of TDs, for example, the growth of GaAs [47] and Ge growth [48] on Si substrates. The TD density can also decrease with increasing growth thickness due to the annihilation or combination event, however, the probability of self-annihilation will decrease as the TD density decreases, and therefore reaching a minimum TD density in an epitaxial film [43]. Introducing thermal annealing or annealing cycles can stimulate TD motion hence increasing the chance of self-annihilation [48]. Methods to bend TDs and suppress their propagation towards the active region include the insertion of strained layer superlattices that act as dislocation filter layers (DFLs) [49]. More importantly, the application of DFLs also breaks the limit for TD self-annihilation by encouraging the movement of TDs in response to misfit strain thus can provide further improvements on TD density [50]. By carefully designing the composition and thickness of the DFLs, low TD density in the range of 10^5 ~ 10^6 cm^{-2} [51, 52] are possible. Methods for threading dislocation reduction discussed above are generally used in combination to achieve a low-defect-density platform (in the range of ~ 10^6 cm^{-2}) for subsequent laser structure growth, which in turn results in a large buffer thickness (> 2.5 μm) that renders the generation of micro-cracks. Moreover, the increased vertical distance caused by the thick buffer layer results in reduced coupling efficiency to waveguides for evanescently coupled lasers. The aspect ratio trapping method using patterned Si substrate can reduce the defect density without significantly increasing the total buffer thickness, but it will add

a fabrication burden and address extra difficulties for growths by MBE where the surface cleanliness is dispensable.

On the other hand, partially replacing the thick GaAs buffer layer on Si with Ge/Si accommodates the large lattice and thermal mismatches between GaAs and Si, leaving a low-defect-density surface without significantly increasing the total thickness. Besides, the heteroepitaxy of Ge on Si is also fundamental to group-IV optoelectronic devices such as GeSn lasers, Ge transistors and Ge photodetectors [53] on Si. It has been reported that by growing only 270 nm Ge on Si substrate, the threading dislocation density (TDD) (6.1×10^8 cm^{-2}) can be reduced to the same level of 1300 nm GaAs on Si [54]. A high operating temperature of 130 °C has also been demonstrated for InAs/GaAs QD laser grown on such GaAs/Ge/Si templates [55]. Moreover, as the TDD of 270 nm Ge on Si is still in the 10^8 cm^{-2} range and the TDD difference after the third and the fourth DFL layer is not obvious [55], more effective ways of leveraging beneficial effects of Ge buffer and DFLs to enable lower surface TDD and total buffer thickness are possible.

1.3 Development of group-IV lasers on Si

1.3.1 Si Raman lasers

The occurrence of Si Raman lasers circumvents the indirect-bandgap nature of Si and enables the manipulation of lasing wavelength by ingeniously using stimulated Raman scattering (SRS) process. When an input photon enters a medium, its energy can be reduced to enable lattice vibration so that the output photon will have less energy and shifted frequency, which is called a Stokes wave. This process is called spontaneous Raman scattering. Under intense pump field, nonlinear process SRS can take place where Stokes wave grows rapidly inside the medium and the pump decreases gradually as the pump energy is transferred to the transition [56, 57]. The initial growth of the Stokes wave is related to the Raman-gain coefficient and pump intensity. The Raman-gain coefficient is associated with the imaginary part of a third-order nonlinear susceptibility and is the most important factor describing SRS. As long as the pump frequency is within the bandwidth of Raman-gain spectrum (a function of the frequency difference between the pump and the Stokes wave), it will be amplified by spontaneous Raman scattering. However, the frequency component for which Raman-gain coefficient is maximum builds up fastest and can grow almost exponentially upon reaching certain threshold pump power. As the lattice vibrational frequency is unique and certain for each element, the emission wavelength of Raman

lasers using stimulated Raman scattering mechanism is theoretically tuneable in a wide range upon careful selection of the pump source. This feature is attractive and foresees the applications of Raman lasers in many fields such as in the ultra-violet range for biological agents and explosive detection, fluorescence imaging or remote sensing, and in the visible range for biomedicine and ophthalmology [57], etc. More importantly, for Si photonics, the occurrence of Si Raman lasers provides a potential for realising Si-based low-cost, monolithically integrated optical component.

The main limitation that hinders the generation of net Raman gain is the two-photon-absorption (TPA)-induced free carrier absorption (FCA), which is also the predominant loss mechanism that causes the pump depletion and increases the optical loss for Raman signal. Two-photon absorption happens to a significant extent only in high optical intensities, where two photons with at least half of the bandgap (and usually with the same energy) are absorbed at the same time and excite an electron to a higher state with the energy increase equal to the sum of the two photon energies. This means more free carriers which are incapable of being created originally (due to lack of energy) are generated and will absorb more photons due to the free-carrier absorption subsequently. Methods to eliminate the losses include extending the waveguide in the lateral dimension as the effective length will be reduced due to losses. Another method is to use pulse laser excitation with pulse width much less than the lifetime of free carriers [58], so that after the TPA process the pump pulse has ceased, thus unable to complete the FCA process. Based on these two methods, the first demonstration of Si Raman laser was achieved in an 8-meter-long fibre ring configured cavity under pulsed pumping in 2004 [58]. Later in 2005, compact all-silicon rib waveguide cavity Si Raman laser was realised by adopting a reverse-biased p-i-n diode structure [59]. Under applied electric field, the reversed biased p-i-n rib waveguide can sweep away the TPA-induced free carriers from the active region thus significantly reduces FCA loss. In the same year, continuous-wave Si laser was successfully presented with reverse-biased p-i-n and carefully designed low-loss cavity [60]. The schematic configuration is shown below in Figure 1- 9 (a). The laser cavity was established from a silicon-on-insulator (SOI) rib waveguide whose front and back facets were coated with dichroic and broadband high-reflectivity coatings, respectively. Theses dielectric coatings will first enable the pump beam to enter the waveguide, after reaching the back facet, both the pump beam and generated Stokes wave will be reflected. Then the reflected pump beam will exit the cavity, but Stokes

beam can keep travelling inside the waveguide and stimulate more Stokes transition. The p-i-n structure was defined with standard photolithography and reactive ion etching and doped heavily by ion implantation in the different sides of the slab, as shown in the blue and pink colours in Figure 1-9 (a) and in the cross-sectional scanning electron microscopy (SEM) image in Figure 1-9 (b) [60]. The free carrier lifetime can be effectively reduced with the increase in applied electric field, thus suppressing the TPA-induced FCA loss. This design is vital to achieve net Raman gain for lasing.

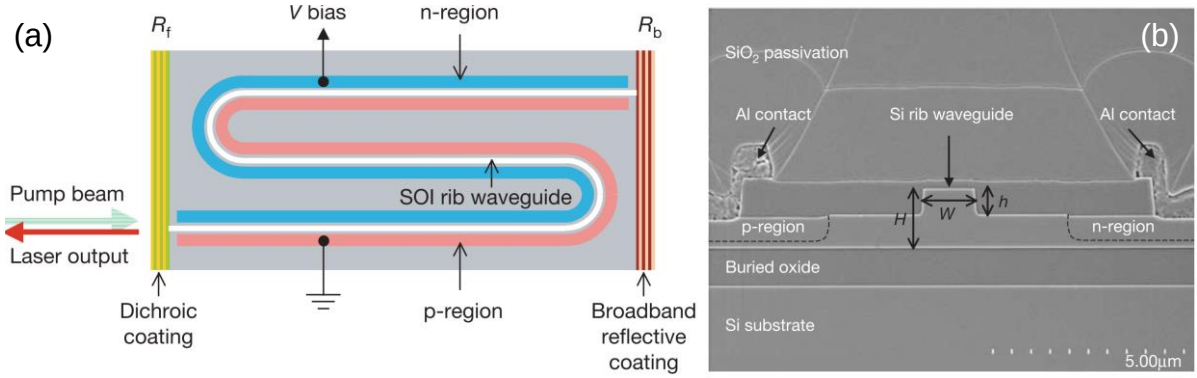

Figure 1-9 (a) The schematic configuration of the Si waveguide laser cavity with a p-i-n diode structure and multi-layer dielectic coatings at both front and back facets. (b) Scanning electron microscopy image of the cross section of the Si Raman laser, showing the p-i-n diode structure along the Si rib waveguide. These figures are from reference [60].

Later in 2008, the first cascaded Si Raman laser was demonstrated, which further extended the lasing wavelength to 1848 nm from second-order cascaded lasing by using a 1550 nm pump source, showing great potential for achieving compact, low-cost and room-temperature lasers operating at longer wavelengths that are not easily accessible for conventional lasers [61]. Another reason for the realisation of cascaded Si Raman laser is the absence of nonlinear optical loss TPA-induced FCA beyond 2.2 μm for Si [62] as the minimum photon energy required to lead to TPA is half of the Si bandgap, which is 0.55 eV. The working principle of cascaded Si Raman laser is that under intense pump field, the generated first-order Stokes wave still has high energy to excite the second-order Stokes transition, so that the pump energy can transfer continuously from first order to higher-order Stokes waves. Bragg mirrors pairs and micro ring resonator configurations have been proposed to selectively reflect different orders of Stokes waves to achieve cascaded lasing [63]. The first-achieved cascaded Si Raman laser used a directional coupler, and the schematic illustration is shown in Figure 1-10. A straight bus waveguide is connected to the racetrack ring-shaped cavity

through a directional coupler, from which the pump and generated Raman signals can be guided in and out of the laser cavity [61]. The bottom part of Figure 1-10 shows the cascaded lasing process where the solid lines represent the pump and different order Stokes process wavelengths, and the dotted lines indicates the wavelength tuning by changing the input pump wavelength. The major challenge of designing a cascaded Raman laser is the selection of the coupling coefficients to assure (1) the coupling is close to the pump wavelength to leverage the cavity enhancement effect; (2) the coupling for first-order Stokes wavelength should be close to zero so that the generated first-order Stokes waves can be confined inside the cavity and build up with increased pump power thus generating second-order Stokes waves (or desired higher-order Stokes); (3) low coupling for second-order (or desired higher-order) Stokes wavelength to ensure sufficient output power extraction and low lasing threshold [61].

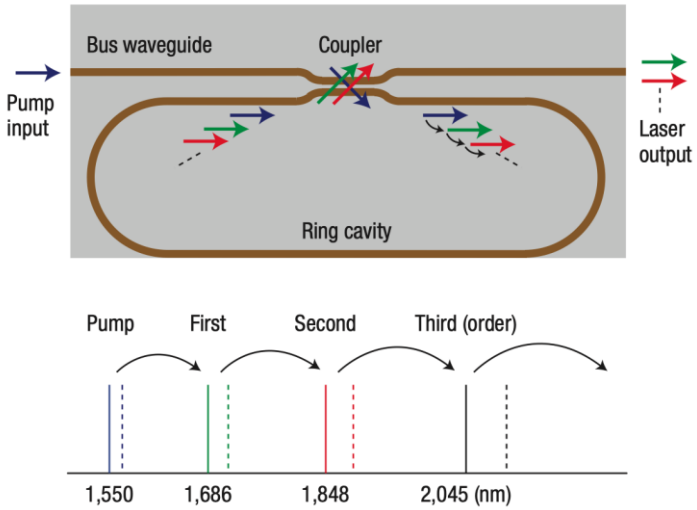

Figure 1-10 The schematic structure of cascaded Si Raman laser. A bus waveguide is connected to the racetrack ring cavity by a directional coupler. The input pump as well as Raman lasing signals are coupled in and out of the ring cavity through the coupler. The bottom figure shows the cascaded lasing process where the solid lines represent the pump and different order Stokes process wavelengths, and the dotted lines indicates the wavelength tuning by changing the input pump wavelength. This figure is from reference [61].

Moreover, as Raman gain is inherently small compared to that of radiative recombination from direct bandgap semiconductor materials, device structural design and fabrication need to be optimised to reduce the lasing threshold. Improvements of the lasing threshold can be achieved by optimising the cavity quality factor and increasing the pump efficiency so that low pump power will be required to obtain Raman gain for lasing [64]. Moreover, low lasing threshold is also accessible by using micro- or nano scale cavities because the light-matter interactions strength is

positively dependent on the ratio of quality factor to the cavity volume [65]. A continuous-wave Raman laser based on photonic crystal cavity with a low lasing threshold of 1 microwatt has been reported, and ascribed to the extraordinarily high quality factors of both the even nanocavity mode and odd nanocavity mode [65]. Such micro- to nano-scale devices are promising for the large-scale integration of optical sources on photonic circuits.

However, although Si Raman lasers have developed rapidly since its first demonstration, fundamental issues remain: First, it must be optically pumped. This significantly obstructs the practical applications of Si Raman lasers as on-chip light sources. Second, external electric field is desirable for the reduction of TPA-induced FCA, which requires extra power consumption and external circuits unfavourable for large-scale integration. Third, the fabrication of nano-sized photonic crystal structure is challenging. Any coarse sidewalls, poorly defined air holes or unreleased structures can cause scattering of the generated light and lead to the failure of the device.

1.3.2 The Bandgap Engineering of Ge

Ge is an interesting candidate for light-emitting devices because it has a direct gap energy only slightly higher (136 meV) than the indirect L-band, which makes the band engineering of Ge into a direct-gap material possible, unlike Si with a much larger direct gap (3.4 eV) than the indirect gap (1.1 eV). Efforts towards higher directness of Ge band structure fall mainly into three categories: applying tensile strain, n-type doping, and alloying with α-Sn.

1.3.2.1 Tensile Strain

By implementing biaxial tensile strain, both the direct and indirect valleys of Ge shrink, while the direct gap shrinks faster than the indirect counterpart because of the difference of their deformation potentials, enabling achievement of complete directness of Ge at 1.8 % of tensile strain [66, 67]. The growth mode changes from two-dimensional coherent growth to Stranski-Krastanov (SK) growth mode after about 3 monolayers (ML) of strained system Ge on Si [68, 69], which means the Ge layers used in the device are mostly strain relaxed as 3 ML Ge is too thin for an active layer. There is a 0.25% tensile strain in Ge when Ge is grown on Si because of the larger thermal expansion coefficient of Ge than Si [67], but this thermal-mismatch-induced tensile strain is overall insufficient to make Ge a direct-bandgap material. As radiative recombination heavily depends on the directness of materials, the research into Ge band engineering therefore becomes more important. More recently in these two

decade, various attempts of applying stressors or suspension platforms to Ge succeeded in applying large tensile strain and achieving light emission [70, 71]. For example, mesa etching the relaxed Si_3N_4 stressor can induce large tensile strain to the suspended Ge-on-SOI structure [71].

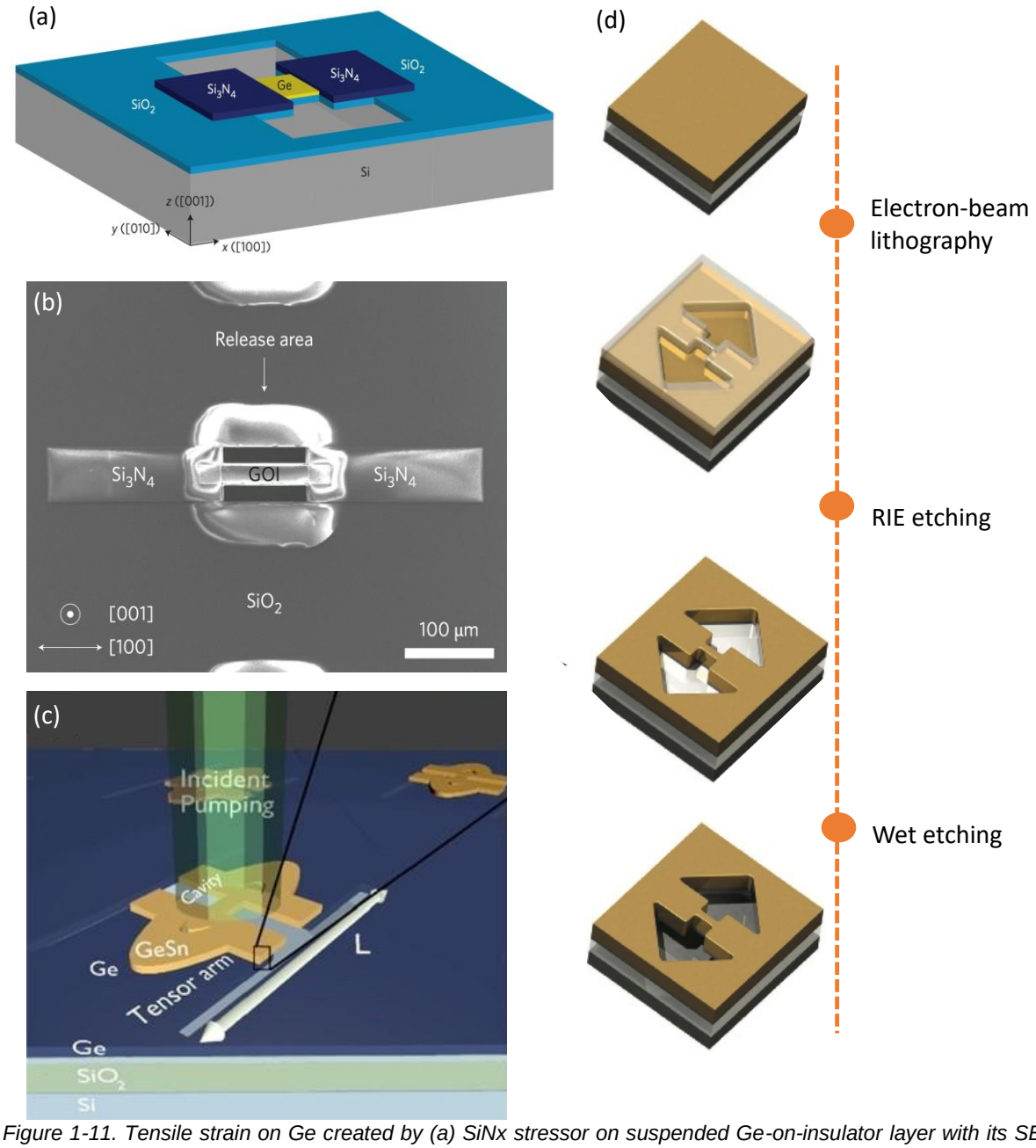

Figure 1-11. Tensile strain on Ge created by (a) SiNx stressor on suspended Ge-on-insulator layer with its SEM image in (b) [13], (c, d) improved approaches without external stressors [72, 73].

An illustration of the structure is shown in Figure 1-11 (a) with its Scanning Electron Microscopy (SEM) image in Figure 1.11 (b). The advantage of this mechanical design is that the introduced strain is very sensitive to the structure parameters and material properties including the length of the released stressor, Young's modulus, Poisson's ratio, and layer thickness, i.e., bandgap manipulation is within reach by changing the

design parameters while the corresponding drawback is that the layer thickness is limited by the stress transfer. In 2013, M. J. Süess *et al* developed the previous mechanical design of the suspended Ge-on-insulator by a top-down fabrication process (as can be seen in Figure 1-10 (c, d)) without the SiN_x stressor layer [72, 73], applied to Ge/SOI or Ge/Si and acquired 3.1% uniaxial strain and a predicted 460 cm^{-1} optical gain for $10^{19}cm^{-3}$n-type doping with electron-hole injection density of $3 \times 10^{19}cm^{-3}$ [73]. Although not tuning Ge into direct-bandgap material, this approach pushes forward the strain engineering of Ge to a more integrated direction (without nitride materials as stressor). In 2019, the same group improved their design and accomplished lasing in highly strained (5.9%) Ge microbridge with identical values of direct and indirect band energies [74].

1.3.2.2 N-type Doping

N-type doping increases the directness of Ge in a different way (see figure 1-12). The red lines stand for conduction band, blue lines represent light hole band and green lines are used for heavy hole bands. Electrons injected by n-type doping fill the L-band of Ge to level parallel to the direct gap, making the direct band-to-band transitions dominant. In the meantime, the 4-5 orders of magnitude faster process of direct band-to-band transition compared to the indirect transition of the radiative recombination consumes injected carriers more quickly in direct band, forcing the diffusion of carriers from L band to Γ band by scattering, helping to achieve net optical gain [66, 75]. Moreover, as the energy state of doped Ge in L valley is already filled by implanted electrons, a lower density of carrier injection is needed for population inversion which consequently reduces the free carrier absorption and thus decreases optical loss. Figure 1-13 (b) shows the optical gain obtained by a combination of applying tensile strain of 0.25% and n-type doping of $7 \times 10^{19}\mathrm{cm}^{-3}$ [67]. It suggests that n-type doping is essential to acquire net gain for low-tensile-strain conditions. Impressively, electrically pumped Ge laser is realized with delta doping (alternating dopant and Ge layers) [76] of a high doping density of $4 \times 10^{19}cm^{-3}$ [76]. However, the extrinsic-electrons-induced free carrier absorption does hinder the achievement of net gain when compared with the intrinsic direct-gap materials and optical loss will dominate when the population inversion is achieved, and the optical gain will be saturated.

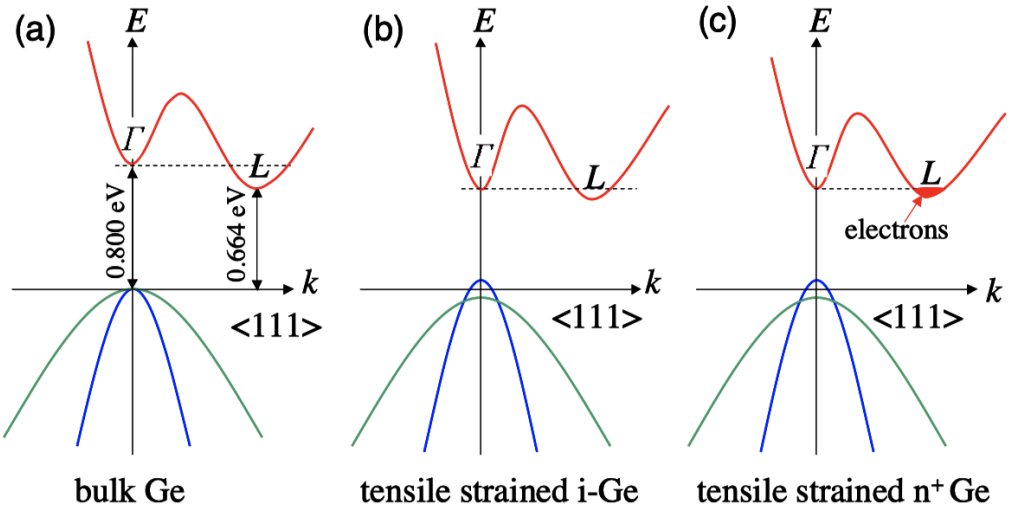

Figure 1-12. Band structure of (a) bulk Ge (the difference between Γ and L valley is 136 meV) (b) tensilely strained Ge without doping (energy difference decreases to 115 meV) and (c) tensile strained n^+-doped Ge [75]. The red lines stand for conduction band, blue lines represent light hole band and green lines are used for heavy hole bands.

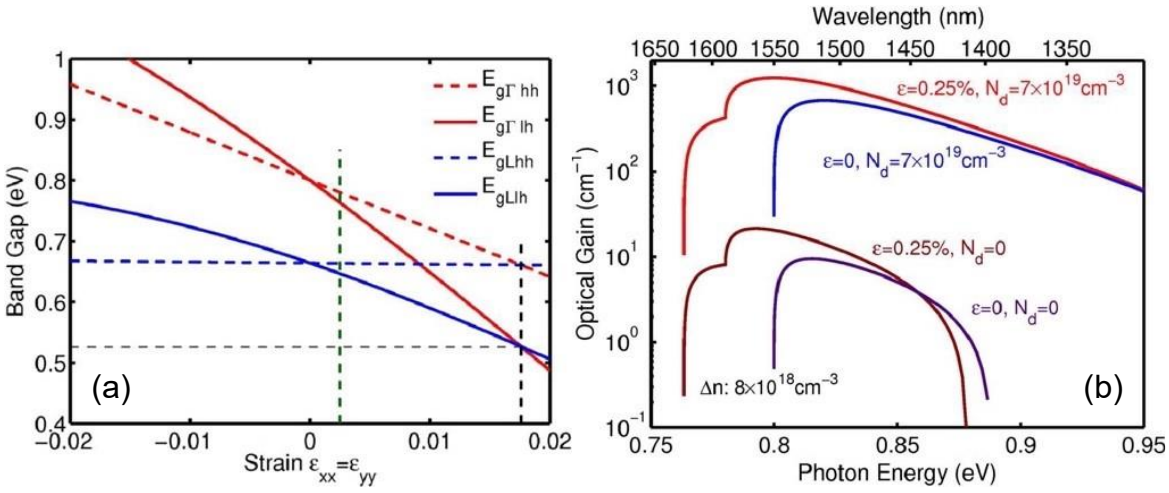

Figure 1-13. (a) The relation between in-plane tensile strain and Ge bandgap energy, $E_{g\Gamma hh}$, $E_{g\Gamma lh}$, E_{gLhh}, E_{gLlh}, are the energy difference between Γ and heavy-hole band, Γ and light-hole band, L and heavy-hole band, L and light-hole band, respectively, the vertical dashed-line close to strain value of 0.018 represents the crossover of Ge from an indirect bandgap material to direct bandgap material; (b) Impacts of combinations of tensile strain (0.25%) and n-doping (7×10^{19} cm^{-3}) on optical gain [67].

1.3.2.3 Alloying with α-Sn

Ge-Sn alloying as one of the approaches to attain direct bandgap of Ge received great research interest since its rise in 1982. The directness of the bandgap of GeSn alloy increases almost linearly with Sn composition. Two theoretical methods implemented for the analysis of GeSn band structure: second-nearest-neighbour tight-binding model of the Koster-Slater type using virtual-crystal-approximation and pseudopotential method gave similar results for $Ge_{1-x}Sn_x$ band structure and predicted the 'direct gap window' to be $0.2 < x < 0.6$ [77] and $0.26 < x < 0.74$ [78],

respectively in early studies. These two approaches explained the reason of lower direct bandgap energy of GeSn than pure Ge: the band structure of GeSn was deduced from the diagonalizing and averaging of the Hamiltonian including parameters of Ge and Sn, which meant the conduction band minimum of GeSn was a mixture of that of Ge and Sn. This averaging validity was derived from the sufficiently small difference in on-site energy of Ge and Sn. The estimated boundary values of 0.74 and 0.6 meant that $Ge_{1-x}Sn_x$ would become a zero-gap semi-metallic material upon further Sn incorporation [77, 78]. Other predictions of the crossover from indirect to direct bandgap are in a range of Sn incorporation from 6% to 11% [77, 79, 80]. These analyses shed light on probable band manipulation of Ge and the high carrier mobility of this group IV material should result in promising device performance [78].

1.3.3 GeSn Lasers

The first GeSn laser dates to only eight years ago, it was optically pumped, with cryogenic operation temperature of up to 90K, and high threshold excitation density of around 325 kW cm^{-2} [15], but it undoubtedly proved the viability of direct-bandgap all-group-IV lasers. It was grown by reduced-pressure CVD (RPCVD) on a slightly tensile-strained Ge buffer, with 12.6% Sn. The lasing behaviour can be attributed to the Sn-alloying induced direct gap, reduced defect density and improved crystal quality compared to the previous unsuccessful attempts [15]. However, compared with state-of-the-art III-V lasers, if one converts the threshold power density to current density under the same free carrier injection rate, it will be two orders of magnitude higher. The directions of improvements are threefold: (1) working under electrical pump (2) room temperature operation and (3) lower lasing threshold. The electrically pumped GeSn laser is still missing despite some efforts [81, 82]. To secure net gain it requires the optical gain surpassing optical loss. Increasing Sn composition can lower the energy difference between Γ and L band thus aiding population inversion at a significantly lower electrical injection density. This idea is confirmed by the increased electroluminescence with increasing Sn composition. However, there is a parallel increase in non-radiative recombination due to the misfit dislocations induced by plastic strain relaxation for higher Sn stoichiometry, consequently hindering the lasing [82]. Besides, doping and a reduction in p- and n-doped region thickness may also help to reduce the threshold current density in electrically injected GeSn layers because of decreased modal losses (a loss of energy on the part of an electromagnetic wave) [81]. The operation temperature can also be elevated by higher GeSn

directness through enhanced direct band transitions. Moreover, larger thickness of the GeSn active layer enhances optical mode confinement; strain relaxation contributes to a better directness, and lower defect density can both improve lasing temperature and decrease the threshold [83]. Several research groups have demonstrated successful attempts to fulfil these improvement parameters. First approach is adopting a microdisk-shaped laser structure, as the optical confinement is raised by the refractive index contrast between GeSn and the air and there is a favourable distribution of the electrons between Γ and L valleys due to strain relaxation [84]. An example is the raised maximum operation temperature of 130 K and a threshold power of 220 kW/cm^{-2} [84]. The second approach uses very high Sn content GeSn active layer to enable large directness. The maximum lasing temperature is further increased to 180 K (17.5% Sn) with a threshold excitation of 117 kW/cm^{-2} [85] and 270 K (20% Sn) with a threshold of 40 kW/cm^{-2} [86]. The third approach applies tensile strain to the GeSn active layer. The positive impact of tensile strain on GeSn lasing was first confirmed by the strongly enhanced PL of a $Ge_{0.94}Sn_{0.06}$ microdisk, where the strain is applied by the SiN_x stressor atop [87]. Then comparatively low threshold (in the range of kW/cm $^{-2}$) continuous-wave lasing was observed in a similar structure with the stressor underneath the GeSn layer [88]. Most recently, the best performances in terms of highest working temperature and lasing threshold so far were achieved by a tensile-strained GeSn micro-bridge laser, lasing up to 273 K with a threshold of 10 kW cm^{-2} [72] and a tensile-strained microdisk laser under pulsed excitation with pulsed excitation up to 100 K and with a threshold of 0.8 kW cm^{-2} [89], respectively.

1.4 Development of III-V lasers on Si

1.4.1 Semiconductor QDs

When the electrons are confined within sufficiently narrow region of semiconductor material, or in other words, quantisation energy of the system is comparable with a characteristic energy of the system, e. g. Fermi energy or thermal energy k_BT, size quantisation will impact significantly on energy spectrum, that is when the QW width falls into the same order of magnitude as the electron de Broglie wavelength in the case of one dimensional electron confinement [90]. In practice, at room temperature this well width is around 20 nm or less for GaAs. Similarly, if the energy barriers for electron motion exist in two or three directions, which are known as quantum wire and QD, respectively, size quantisation plays remarkable effects on the energy spectrum. Followed by that is the change of allowed electronic states over the energy, and thus

change the shape of density of states (DOS). Figure 1-14 (a) shows the DOS of bulk material, where there is no quantum confinement in any dimension, exhibiting a continuous DOS in parabolic shape. The DOS increases as square root of increasing energy. The DOS for QW structure, where the motion of electron is confined in one dimension, is a step-like function, as shown in Figure 1-14 (b). Compared to bulk material, such DOS is preferential for laser applications as the contribution of the higher energy states to the threshold is retarded [90]. For quantum wire structure in which two dimensions of electron motion have been restricted, the DOS presents a more quantised state as shown in Figure 1-14 (c). While for zero-dimension material QD whose electrons motion are confined in all three dimensions, the DOS shows completely discrete delta-function peaks centred at the atomic-like energy levels in Figure 1-14 (d). As a result, the density of charge carriers accounting for population inversion is significantly enhanced at the expense of the higher energy states of the continuum. This will contribute to the much steeper dependence of the optical gain on the current density and decreased transparency current. Consequently, given the same cavity loss, QD structure can provide much lower threshold current density compared to double heterostructure or QW structures. In addition, the optical behaviour of quantum dash structures might be considered as similar to quantum wires as they present broader PL emission than QDs.

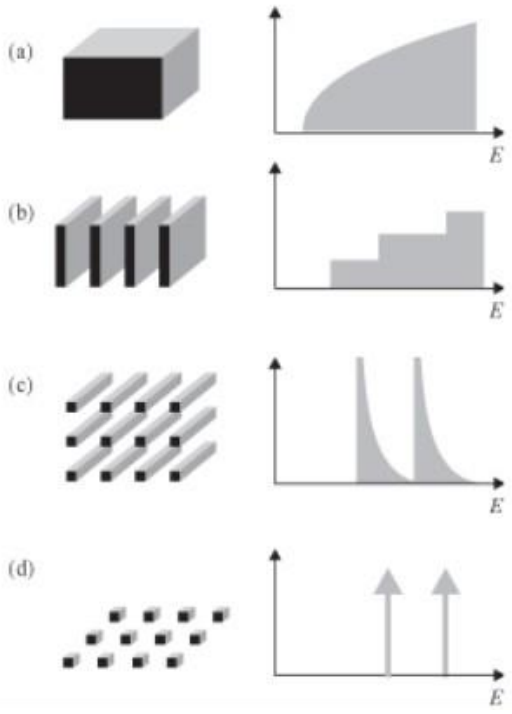

Figure 1-14. Schematic illustration of density of states for (a) bulk material; (b) quantum well; (c) quantum wire; (d) quantum dot [90].

1.4.2 QDs as active region for telecommunication

Given the excellent properties including low threshold, high reliability and insensitivity to crystal defects and temperature, the monolithic integration of III-V QD lasers on Si or Ge looks extremely promising for on-chip light source for Si photonics. Following the high reliability and high performance 1.3 μm electrically pumped InAs/GaAs QD lasers demonstrated on Ge and offcut Si substrates with low threshold of 55.2 A cm^{-2} and 62.5 A cm^{-2}, respectively [25, 91], more extensive research interests have been devoted to QD lasers on Si substrate, especially on streamline production-compatible on-axis Si substrates. Remarkable progress has been made on 1.3 μm electrically pumped InAs/GaAs QD lasers on on-axis Si by applying patterned V-groove Si substrates [92-94], GaP/Si APB-free template with optimised growth conditions [95-97] and dislocation trapping layers [45], improved III-As buffer with reduced thickness and QD active region, where a low threshold of ~ 83 A cm^{-2} and an excellent operation temperature of 120 °C has been achieved on on-axis Si substrates [34, 98]. The maximum operating temperatures of QD lasers grown on native substrate and on-axis Si substrate are 220 °C [99] and 150 °C [100], respectively, which are well beyond the requirement in telecom and datacom applications where the typical operating condition is around 80 °C [101]. A low TD density buffer layer on Si is critical to the monolithically integrated QD laser performance. The epitaxial growth structure and schematic device structure of the record-high thermal stability QD laser on Si [100] are shown in Figure 1-15 (a) and (b), respectively. A GaAs buffer layer grown with an optimised three-step growth method ensures a TD density of 4.3×10^6 cm^{-2} and p-modulation doping is used to enhance the thermal stability of the QD lasers as a result of the compensation of the holes. Highly reflective film with 95% reflectance is applied at the cavity surface. The continuous-wave temperature-dependent P-I curve with temperature from 10 °C to 150 °C for a 6 × 2000 μm^2 QD lasers is shown in Figure 1-15 (c). The 8-layer QD laser has a threshold current of 116.1 mA and an output power of over 100 mW at 20 °C. The saturation output power of the laser can still reach 2.5 mW at 148 °C, but decreases to 0.13 mW at 150 °C. In addition, a co-dope method that applying both p-type modulation and n-type doping in the active region is reported to reduce lasing threshold as well as increase the thermal stability [102].

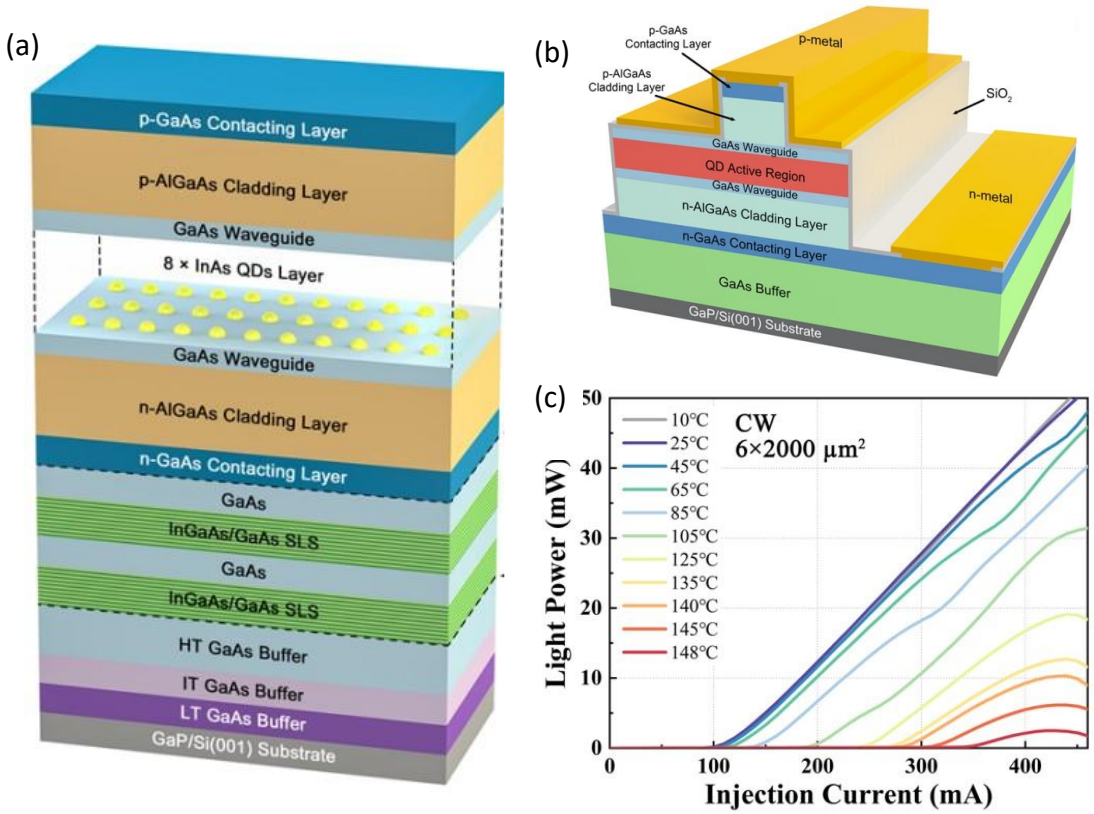

Figure 1-15 (a) The schematic growth structure of a 1.3 μm InAs/GaAs QD lasers grown on on-axis Si (001) with a record-high continuous-wave operating temperature of 150 °C. (b) An illustrative structure of the laser device. (c) Temperature-dependent P-I curves from 10 °C to 150 °C for a 6 × 2000 μm²QD laser [100].

Moreover, the development of InAs/InP QDs that emit at a wider and longer wavelength range from 1.4 to 2.5 μm [103-107] find themselves extremely useful in fibre optic telecommunication systems and sensing applications. Provided the challenges in growing highly uniform 'dot-morphology' InP-based QDs, the development of C-band InP-based lasers is relatively slower. The first electrically-pumped quantum dash laser dates back to 2001, where a room-temperature pulsed laser with a lasing threshold of 410 A cm^{-2} for single stack quantum dash device on InP (001) substrate [108]. To date, the performance of C-band quantum dash lasers have been improved to continuous-wave operation up to 55 °C with a lasing threshold of 528 A cm^{-2} for a five-layer device on InP substrate [109] and continuous-wave operation to 59 °C with a lasing threshold of 1.3 kA cm^{-2} for a three-layer device on on-axis Si substrate [110]. For QD devices, an optimised highest working temperature of 80 °C has been achieved while the threshold remains high at 1.6 kA cm^{-2} for a five-layer device [111]. In addition, high quality InP-based QD lasers emitting at 1.55 μm have also presented excellent temperature stability and high modulation characteristics [112, 113].

1.5 Thesis structure

In this PhD thesis, the investigation of buffer layers and high-quality light sources to be integrated on Si platforms for Si photonics is presented with 7 chapters.

The first chapter is the introduction of Si photonics, including the challenges facing the achievement of high-efficiency on-chip light sources, current solutions and the development of monolithically integrated group-IV and III-V semiconductor light sources on Si.

The second chapter details the experimental methods used for the investigations, including the epitaxial growth, material characterisation as well as optical characterisation.

The third chapter describes the growth optimisation of low-threading dislocation density Ge buffer growth on Si substrate. Various parameters of the structures (dopants in the nucleation layer, layer thickness, growth temperature gradient, thermal cycling) have been investigated. The implications of combining these growth conditions-optimised Ge buffer layer with GaAs-on-Si growth has also been discussed.

The fourth chapter presents two novel approaches to growth high-quality GeSn layer with high nominal Sn values of ~ 10 %. The growth methods have been based on the in-situ RHEED observations during the epitaxial growth, where significantly improved crystallinity has been observed. Detailed material characterisation and the implications of those findings for high-quality GeSn material for real applications have been demonstrated as well.

In the fifth chapter, the growth optimisation, fabrication, and characterisation of long-wavelength InAs/InAlGaAs/InP QD lasers are discussed. Details of MBE growth conditions and fabrication steps are reported. PL and laser characterisations are reported demonstrating the high quality of the growth structures.

The final chapter is a short conclusion of the work presented in the thesis. The main achievements of each chapter are summarised as well as the relationships between the chapters. At the end of the chapter, future work based on the findings of this thesis will be discussed.

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Chapter 2.

Experimental methods

2.1 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is a non-equilibrium physical evaporation method suitable for growth of high-quality thin films or low-dimensional energy confined structures such as quantum dots, nanowires and quantum wells. As a solid source deposition instrument operated in ultra-high vacuum usually in the range of 10^{-10} Torr, which gives atoms a long mean free path, it is highly suitable to grow thin films down to several nanometres and quantum dots with accurate control over each layer. MBE was first intended for GaAs/$Al_xGa_{1-x}As$ and GaAs superlattice growth [1] and then developed for wider variety of applications while maintaining its advantages. MBE's advantages over other epitaxial film growth methods lie in the high precision reproducibility of thin films of the thickness down to several angstroms and its in-situ analysing systems, which allow live monitoring of the epitaxial growth dynamics. Its counterpart Metal-Organic Chemical Vapour Deposition (MOCVD) is not able to grow high-quality quantum dots because of the vapour phase of the source material that is

hard to precisely control, despite it having the advantages of high deposition rate, large-scale production, and low cost.

2.1.1 MBE key components

2.1.1.1 Chambers and pumps

MBE is a large system with numerous components. There is a growth chamber containing effusion cells, a liquid nitrogen cooled cryopanel, an in-situ monitoring system Reflection High Energy Electron Diffraction (RHEED) and a substrate heater and manipulator. Epitaxial growth is achieved here. A load lock chamber has two quartz infrared baking lamps mounted around, for loading and brief baking of samples at 100~200℃ to eliminate water vapour while other samples are grown in the growth chamber. And a buffer (preparation) chamber connects the growth chamber and the load lock chamber with a degas station where the sample substrate is degassed at up to 600 ℃ without affecting the growth chamber. Each chamber has its own pumps to achieve a graded pumping system. The turbo and/or scroll pump in load lock chamber allow rough pumping to the vacuum range of 10^{-7}~10^{-8} Torr. These pumps can also be used to roughly pump other chambers from atmosphere to high vacuum. The preparation chamber has an ion pump to enable vacuum down to 10^{-10} Torr. A cryopump using cryo-condensation of He, an ion pump and a titanium sublimation pump (TSP) are equipped in the growth chamber to achieve 10^{-10}~10^{-11} Torr vacuum level [2]. Sample transfer is accomplished via a rail between chambers. Additionally, cryopanel is a crucial part of the design because it can condense the condensable gases and exclude the source-evaporation-induced localised heating. Ultra-high vacuum (UHV) gate valves separate the chambers to secure a good vacuum and prevent cross-contamination, the valves are opened only when transferring samples. One of the advantages of our MBE lab is that we have a transfer system connecting group III-V MBE and group IV MBE under high vacuum, allowing us to grow mixed layers of Group IV and III-V materials. Figure 2-1 shows a picture of the group-IV Veeco Gen930 solid-source MBE in our lab and Figure 2-2 is a schematic image of it.

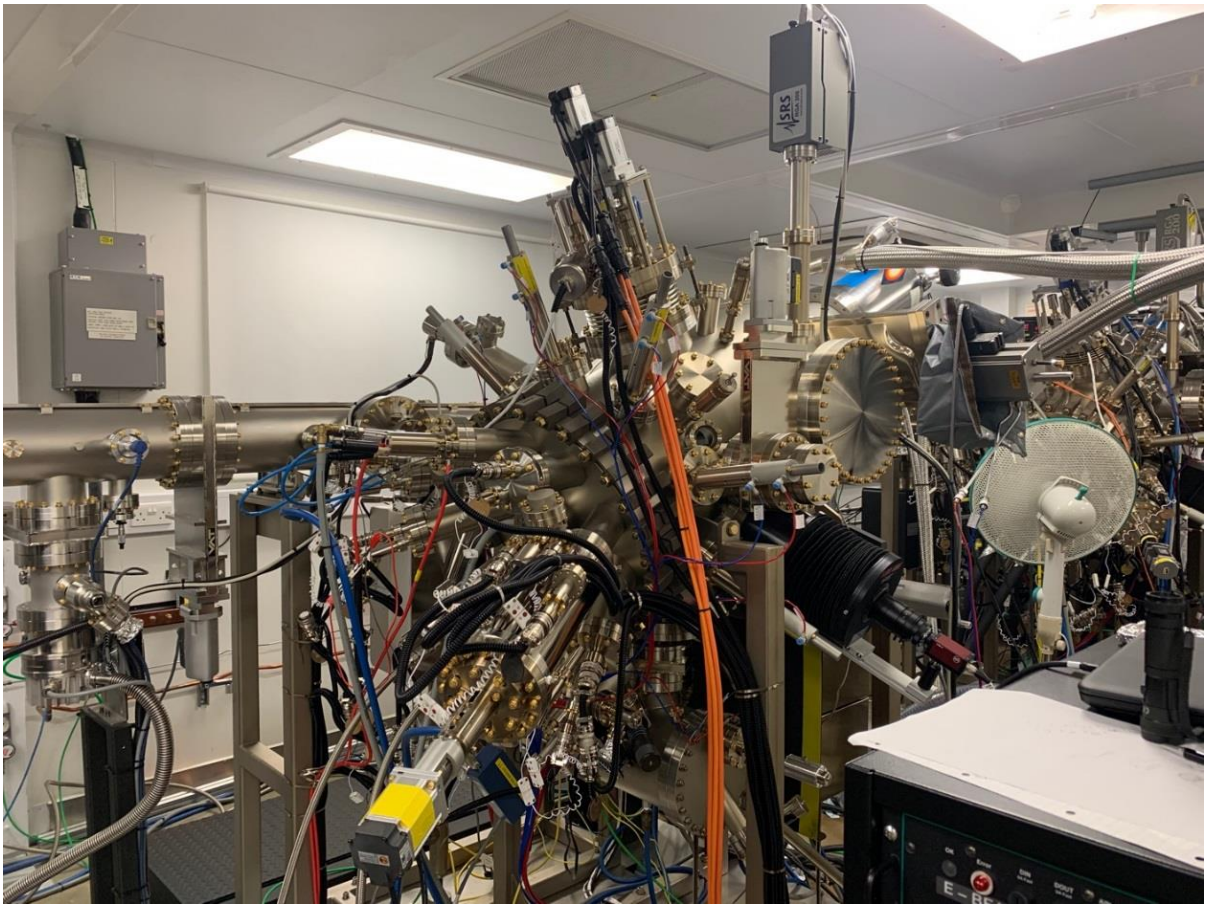

Figure 2-1. A picture showing the Veeco Gen930 solid-source MBE in the UCL MBE lab.

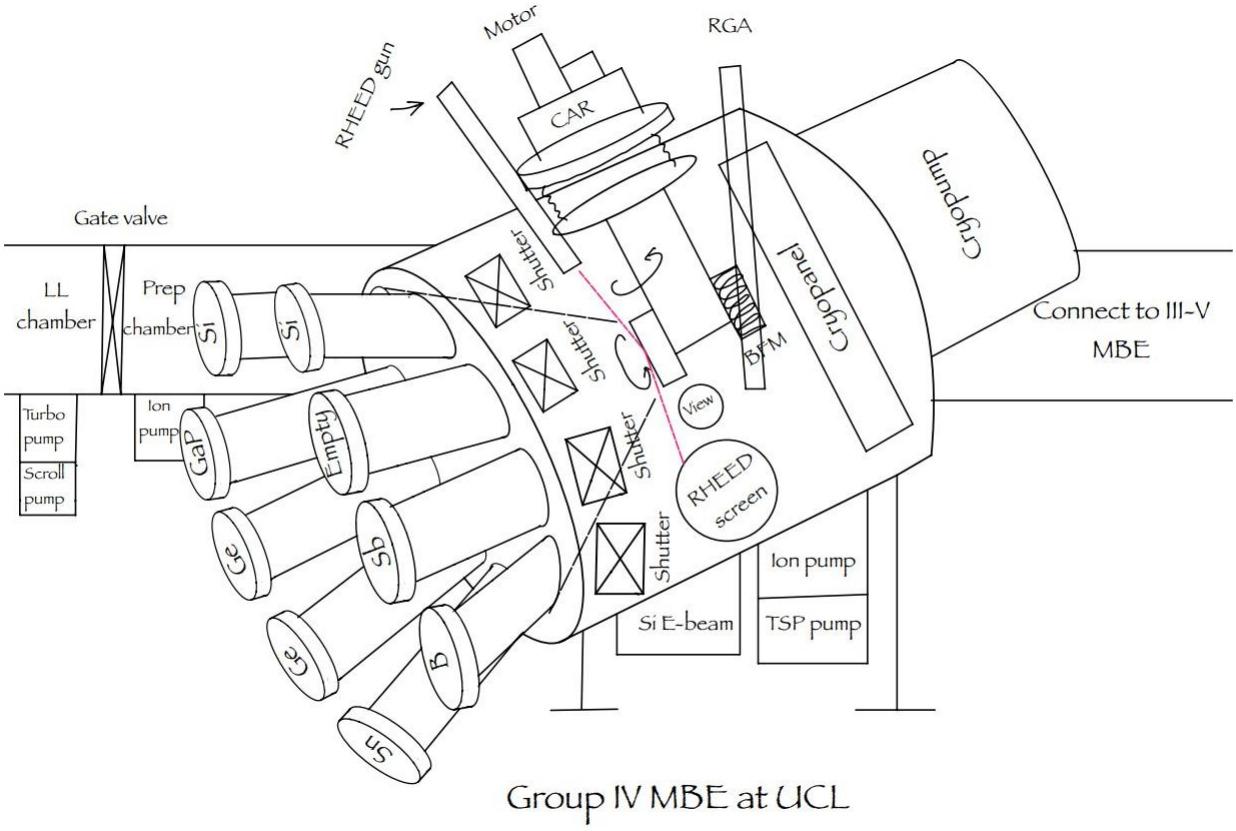

Figure 2-2. A schematic drawing of the group-IV MBE Veeco Gen930 at UCL.

2.1.1.2 Effusion cells

Another key component of MBE is its materials' sources. MBE-grown materials quality has improved thanks to the development of the sources. Standard effusion cells are the Knudsen cells, which generally evaporate any kind of source materials in the temperature range of 200 to 1400℃. The design of the effusion cells is crucial to material quality. An example is depicted in Figure 2-3. The improvement of the small aperture crucible inside effusion cells to conical shape solves the problem of shadowed flux and outgassing, achieving more uniform flux distribution (see Figure 2-3 (a, b)) [2]. However, at very high temperature and high-efficiency evaporation requirements of some source materials such as silicon, an electron beam evaporator is applied to aid the generation of source flux. The e-beam evaporator is a separate system using a high-energy electron beam of 5 – 12 keV to bombard the source material and is directly connected to the growth chamber via an ultra-high-vacuum valve.

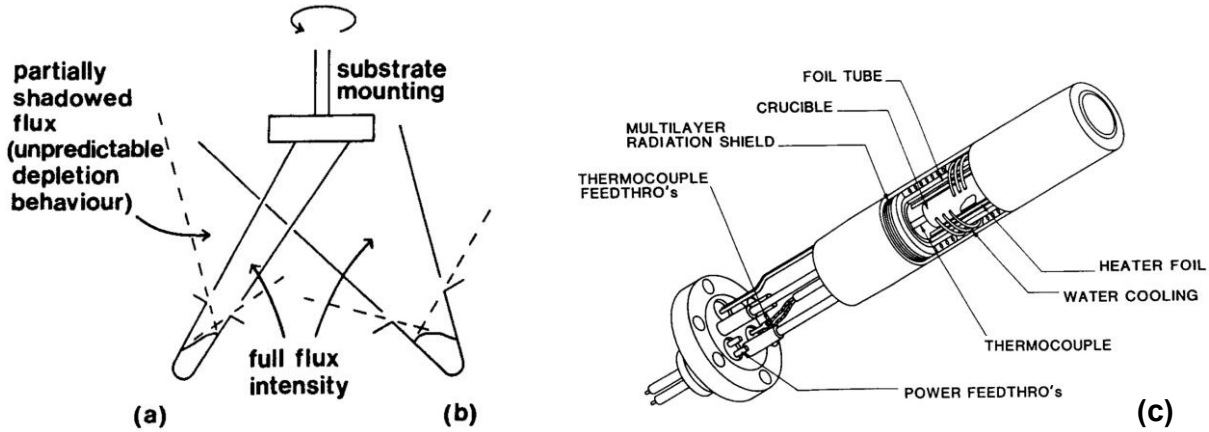

Figure 2-3. (a) Small aperture crucible with shadowed flux problem (b) Modern crucible design with a conical shape (c) Schematic diagram of a K-cell [2].

2.1.1.3 In-situ monitoring instrument: Reflective High Energy Electron Diffraction (RHEED)

As mentioned previously, RHEED makes MBE superior to other epitaxial thin film growth methods in in-situ monitoring of the growth dynamics. RHEED is a diffraction method in essence, so it has the benefit of being very sensitive to the surface crystalline structure of materials, which is desirable for MBE growth, while it also has the drawback of the indirect translation of the diffraction patterns. Usually, it needs extensive investigation and analysis to understand the complex growth dynamics reflected by RHEED patterns. From the perspective of instrumentation, RHEED structure is simple: a high-energy electron gun launches an electron beam of 10-20

keV to the sample surface at a glancing angle of less than 5° to avoid blocking the source, then the diffracted beam is projected onto a phosphorescent screen. The image can then be collected and seen from a laptop. Although a large amount of information contained in RHEED pattern requires careful analysis, one can obtain intuitive impressions on cluster-like or film-like growth features, which is very useful when growing quantum dots as the time and thickness of formation of the dots can be recorded and calculated for reference in further growths.

2.2 X-ray diffraction

X-ray diffraction (XRD) is the most efficient way to determine the crystal structure of a material [3]. It can distinguish between different compounds or phases of the same composition. More importantly, it is a non-destructive method highly desirable in semiconductor material characterisation as post-growth fabrication is usually needed.

2.2.1Working principle

X-ray diffraction approach is based on wave interference of X-rays incident on the crystalline solid. A schematic illustration is shown in Figure 2-4. The two incident X-ray beams can only achieve constructive interference when the Bragg's Law:

$$n\lambda = 2dsin\theta$$

is satisfied, i.e., the path difference between the two beams deflected by the lattice plane is $n\lambda$. From this working principle we can obtain lattice parameter by combing the d spacing acquired at a given incident angle and the X-ray wavelength using the following equation:

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}}$$

Where h, k and l are Miller indices of the diffraction plane.

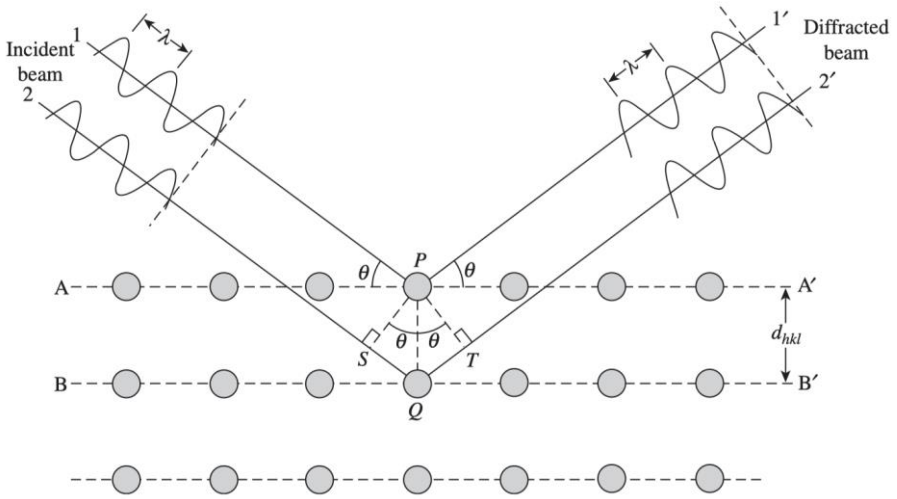

Figure 2-4. Working principle of XRD [3].

In addition to lattice parameters, high-resolution X-ray diffraction (HRXRD) can measure epilayer thickness, superlattice period by the thickness fringes in the XRD image; various crystalline defects such as mismatch, misorientation, mosaic spread, curvature, dislocations; and strain relaxation etc. In this report on investigation of GeSn material quality, the focus of using HRXRD is put on obtaining the lattice parameter, strain relaxation and material quality in terms of dislocation density, mosaic spread and misorientation. The fully relaxed and strained films are illustrated as the Figure 2-5 below, and the determination of strain state is achieved by Reciprocal Space Map as will be detailed in a later section. In general, a fully relaxed lattice has a lattice constant same with its bulk value while a fully strained film has a lateral lattice parameter identical with the substrate underneath. Slip dislocations generate a broadened rocking curve and diffuse scatter. Mosaic spread occurs when slightly misoriented crystals join and form low energy domain boundaries, as shown in Figure 2-5.

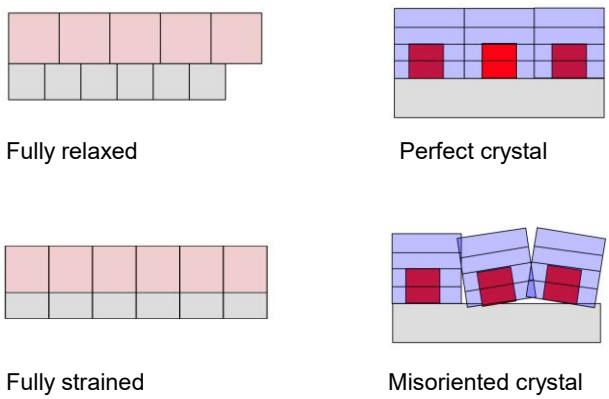

Figure 2-5. Illustration of fully relaxed and fully-strained crystal and perfect and slightly-misoriented crystal [4].

2.2.2 Scan types and applications

2.2.2.1 Rocking curve

There are deferent types of scans available for specific uses. A rocking curve is a plot of X-ray intensity and Omega (the angle between the incident X-ray beam and sample surface). When operating, the detector and X-ray source are fixed, while the incidence angle Omega is changed by rotating the sample. An illustrative image of XRD instrumental setting is shown in Figure 2-6 (a). At the presence of crystal defects or misoriented crystal lattice, the full width at half maximum (FWHM) of rocking curves will be broadened. As shown in Figure 2-6 (b), curve A stands for a sample with EPD revealed dislocation density of 1900 cm^{-2}, while curve D corresponds to a sample with an elevated dislocation density of 99000 cm^{-2} [5]. The mechanism of the FWHM broadening is shown in Figure 2-6 (c). When lattice misorientations or defects exist, the Bragg condition is satisfied at more angles θ_1 and θ_2, except for the original θ. The rocking curve is mainly used to investigate defects such as inhomogeneity, dislocation state, mosaic spread and curvature, which can be reflected from the peak position, broadening etc.

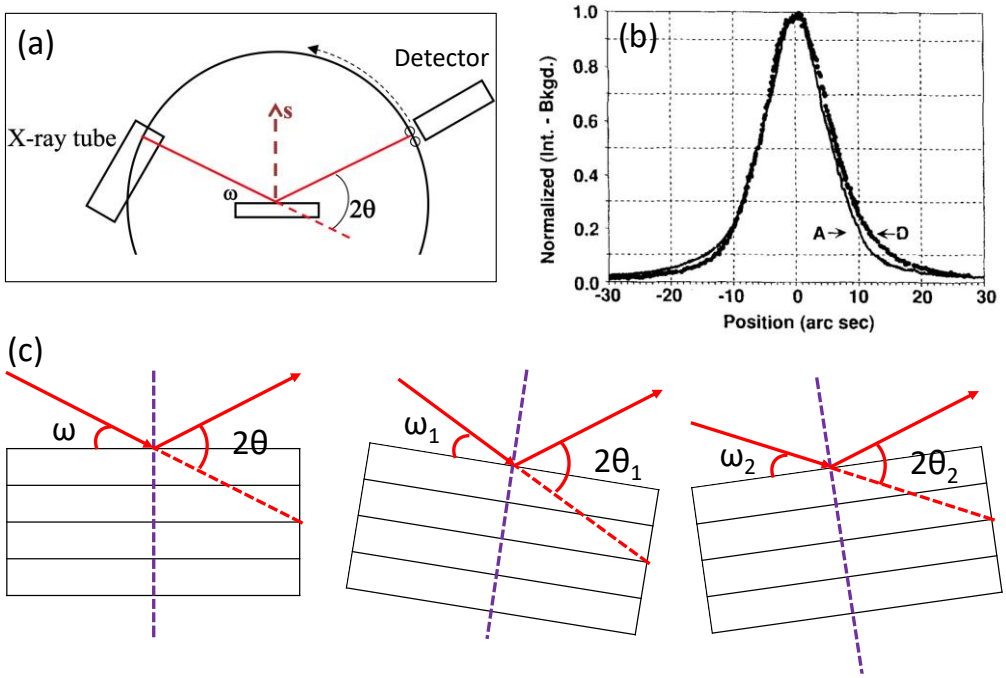

Figure 2-6. (a) Illustrative image of XRD instrumental settings [4].(b) Examples of rocking curves (curve A and D), where curve A stands for a sample with EPD revealed dislocation density of 1900 cm^{-2}, while curve D corresponds to a sample with an elevated dislocation density of 99000 cm^{-2} [5]. (c) Schematic illustration of rocking curve FWHM broadening due to misorientations or crystal defects.

2.2.2.2 Coupled-scan (Omega-2Theta scan)

A coupled scan plots X-ray and 2Theta, but Omega also changes in a way that Omega equals ½ 2Theta plus an offset angle. Coupled scan (also Omega-2Theta scan) is primarily applied to study lattice mismatch, thickness, superlattice period, relaxation and ternary composition. However, because composition, relaxation and lattice mismatch all play roles in changing the position of the Bragg peak, a single Omega-2Theta scan can only work when we know two of these factors, otherwise multiple coupled scans, namely a Reciprocal Space Map (RSM), is required for analysis. RSM provides the most comprehensive information on strained thin films, so it is ideal for the studies in this thesis.

2.2.2.3 Reciprocal Space Map

RSMs are generated by collecting Omega-2Theta scans at different Omega offsets, where $2Theta = 2 \times Omega - offset$. From the map, in-plane and out-of-plane lattice constants, mosaic spread, strain relaxation and misorientations can be easily determined. However, to translate information from RSMs one must think in reciprocal space. Figure 2-7 below is a figure of the reciprocal lattice, where every spot corresponds to a crystallographic plane (hkl). The reciprocal lattice is prominent in understanding diffraction patterns of crystalline solids.

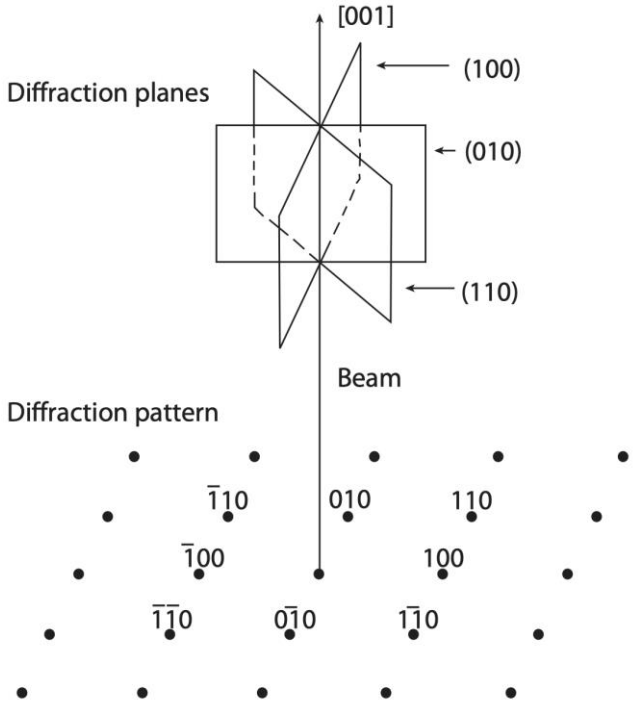

Figure 2-7. Reciprocal lattice and the corresponding diffraction planes [3].

Ewald sphere is a way of simplifying and visualizing the diffraction pattern using the notion of reciprocal lattice. It can link the real space with the reciprocal space in the following way: in Figure 2-8 (a), assume point C is the central point of a circle and O, B and D are points on the circle. D, C and O are in the same line. θ is the angle between line DO and DB. Then the length of line OB:

$$OB = OD\ sin\theta$$

If we set point O to be the origin of the reciprocal space and the radius of the circle to be 1/λ, where λ is the X-ray wavelength used experimentally, then OB is the d spacing of the point B in reciprocal space, which is $1/d_{hkl}$. Then, we will get,

$$\frac{1}{d_{hkl}} = \frac{2}{\lambda}\ sin\theta$$

i.e., Bragg's condition is satisfied in this Ewald sphere. In other words, Ewald sphere depicts the essential conditions to detect crystallographic planes by diffraction. It can be used in RSMs to reveal the d spacing, which can be translated into lattice parameters, of a film as compared with the substrate material both in the in-plane direction and out-of-plane direction. In addition, rocking curves and RSMs can also indicate the extent of mosaicity (mosaic spread), which is a measure of the extent of crystal lattice misorientations. In a mosaic crystal, it contains numerous tiny perfect crystals that are misoriented to some extent. It can be mapped by the amount of the broadening of the reciprocal lattice point perpendicular to the reflecting plane normal, and the peak broadening parallel to the interface is referred to as lateral correlation length, as shown in Figure 2-8 (b).

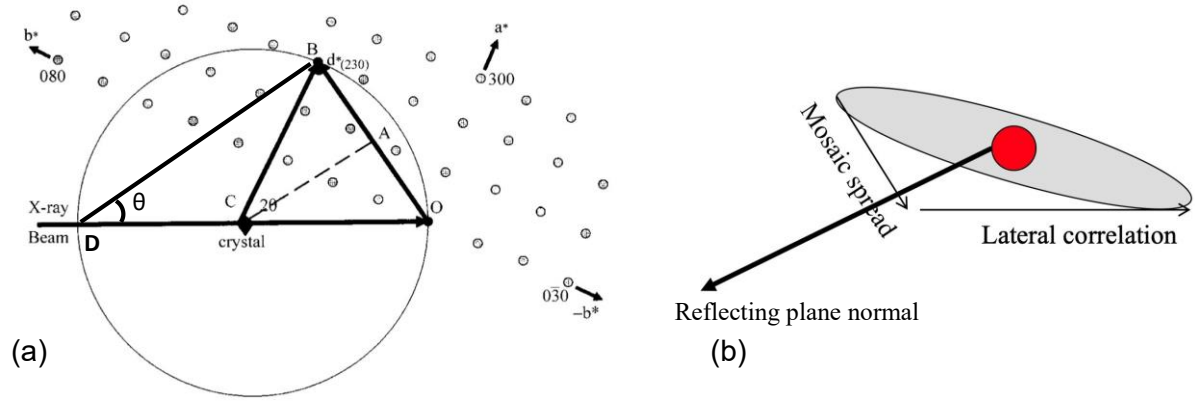

Figure 2-8. (a) Schematic image of Ewald sphere [3]. (b) Mosaic spread and lateral correlation direction [4].

Inspired by the Ewald sphere method, the diffraction patterns created by a rocking curve scan and a coupled scan can be demonstrated as an arc shape centred on the origin and a straight line pointing outside of the sphere, respectively, as shown in

Figure 2-9. Besides, by measuring the broadening of the lattice point perpendicular with the reflecting place normal in the RSM, the mosaic spread can be quantified. Peak broadening parallel with the interface originates from the lateral correlation length.

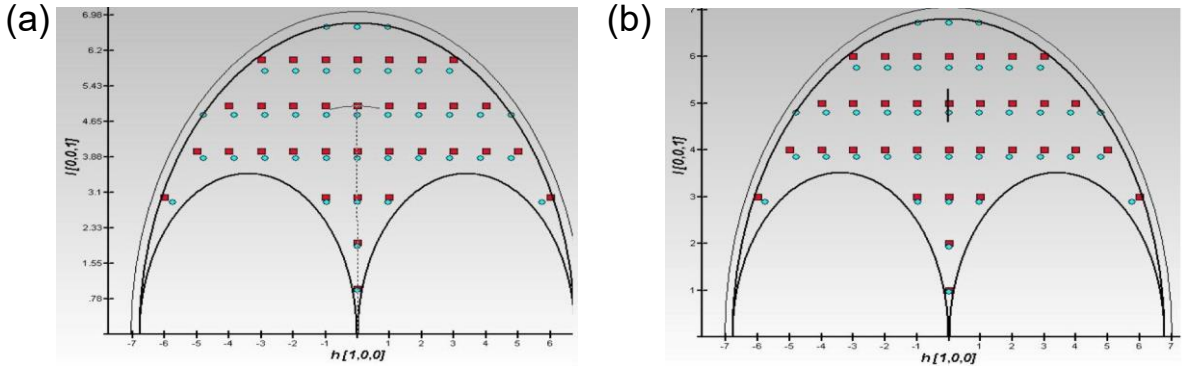

Figure 2-9. (a) Rocking curve scan is an arc centred on the origin of the reciprocal space. (b) Coupled scan appears as a straight line pointing away from the origin of the reciprocal space [4].

2.3 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is one of Scanning Probe Microscopy (SPM) techniques that uses near-field forces between the atoms of the sample surface and the probe tip apex to collect signals on surface topography. It probes surface features down to atomic spacing and a lateral length of a tenth of a millimetre. AFM is a widely used method because it examines materials surface not limited to conductive materials like other SPM methods e.g., Scanning Tunnelling Microscope (STM).

From the perspective of instrumentation, AFM uses a very sharp tip to detect and map the topography of samples. In operation, the tip is mounted on the end of a cantilever and the force between the sample and the tip induces elastic bending of the cantilever, which is examined by a laser beam deflected by a mirror on the back of the cantilever and detected and recorded by position-sensitive photodiodes arranged in four quadrants, as shown in Figure 2-10. The photodiodes are installed three orders of magnitude larger distance from the sample surface than the configuration of the cantilever to enable the magnification of the tip motion, promoting high sensitivity.

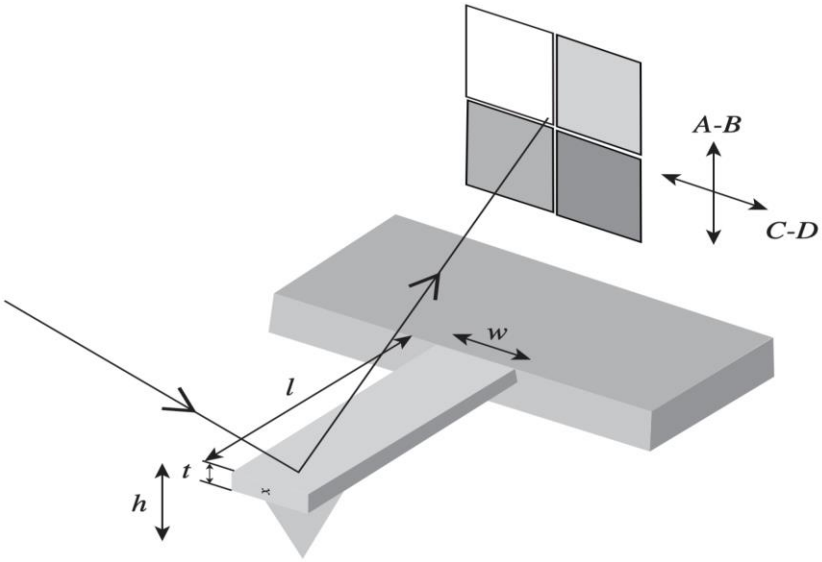

Figure 2-10. Schematic image of the AFM working principle [3].

Static and dynamic modes are the two basic operating modes of an AFM. Under the static mode, a.k.a. the contact mode, a strong repulsive force is used to give high resolution. In this mode, the degree of the deflection of the cantilever is maintained by a feedback loop. In the dynamic mode the cantilever oscillates at a set frequency, and the feedback loop keeps this designed amplitude of oscillation. Tapping mode is the most widely used dynamic mode and it has the advantage of a non-destructive approach while maintaining high resolution, especially for vertical height measurement. There are different types of tips depending on the type of operation mode. Stiff tips are used for non-contact mode and soft tips are applied for contact mode operation to avoid sample surface damage. The tip has a shape of a triangular beam, which can be considered as a cone with an opening angle. An AFM tip of a triangular shape is shown in Figure 2-11. The open-angled shape and the remaining apex radius are vital parameters for the lateral resolution of the AFM. In the AFM measurements in this report, the tip had an apex of 20 nm.

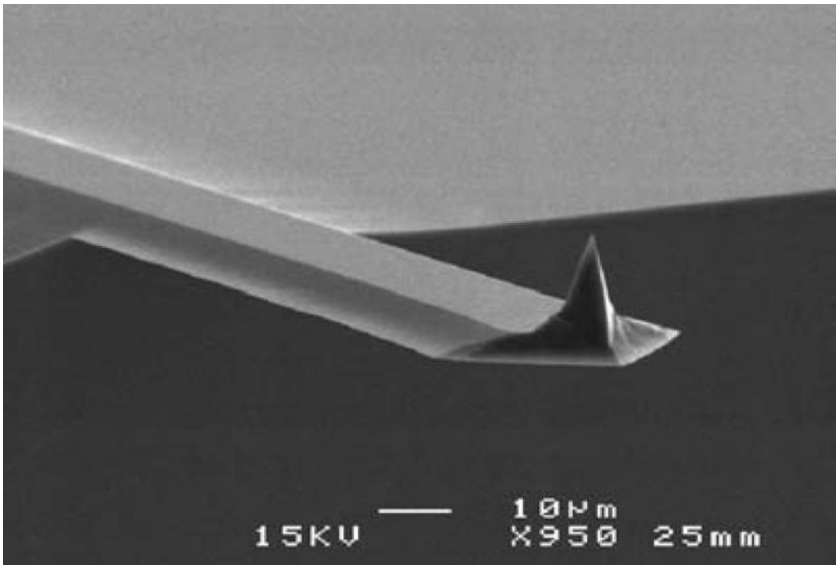

Figure 2-11. An AFM tip of a triangular shape [3].

2.4 Raman spectroscopy

2.4.1 Working principle

Raman spectroscopy and Fourier transform infrared spectroscopy (FTIR) are the two most commonly used methods of vibrational spectroscopy. Vibrational spectroscopy works very differently from other spectroscopic methods like XRD. It uses much lower energy infrared light to match the vibrational energy of molecules and crystal lattice, see Figure 2-12. Raman spectroscopy examines the molecular vibrations (lattice vibrations) via inelastic scattering of light by a molecule (lattice). It can be used to investigate various materials including organic or inorganic materials, polymers, ceramics, and semiconductors etc. but excluding metals due to their high reflectivity of electromagnetic waves.

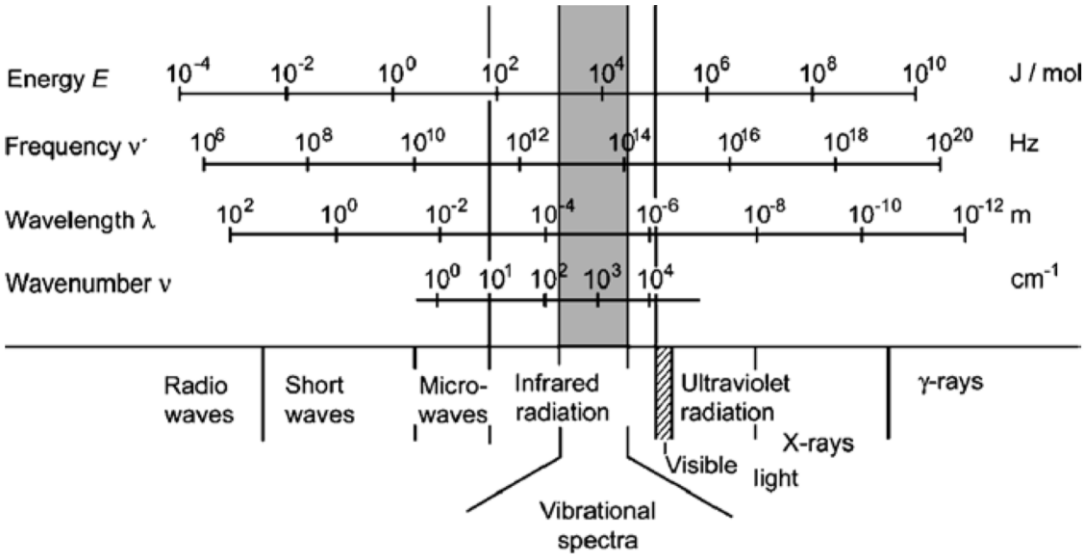

Figure 2-12. Frequency υ^* , wavelength λ and wavenumber υ ranges of electromagnetic waves. Molecular vibrations are in the range of infrared close to the visible light [3].

As infrared light has energy close to molecular vibrational energy, when particular infrared light frequency matches the vibrational frequency of a molecule and the infrared light irradiates the molecule, the infrared light energy will be absorbed and consumed to excite the molecule to a higher vibrational energy level. Vibrational energy is calculated from the spring harmonic vibration model and expressed in the unit of wavenumber, which is reciprocal of the wavelength, in cm^{-1}. After excitation, the vibration either returns to its initial level (Rayleigh scattering) or it returns to a different level. The latter is called an inelastic or Raman scattering process. If the vibrational energy returns to a higher level than the original value, it is called a Stokes scattering, otherwise it is called anti-Stokes scattering as illustrated in Figure 2-13. As the anti-Stokes scattering is much weaker than the Stokes scattering, a Raman spectrum normally counts only the frequency changes induced by the Stokes scattering by molecules and such changes are represented by Raman shift in the Raman spectroscopy spectrum.

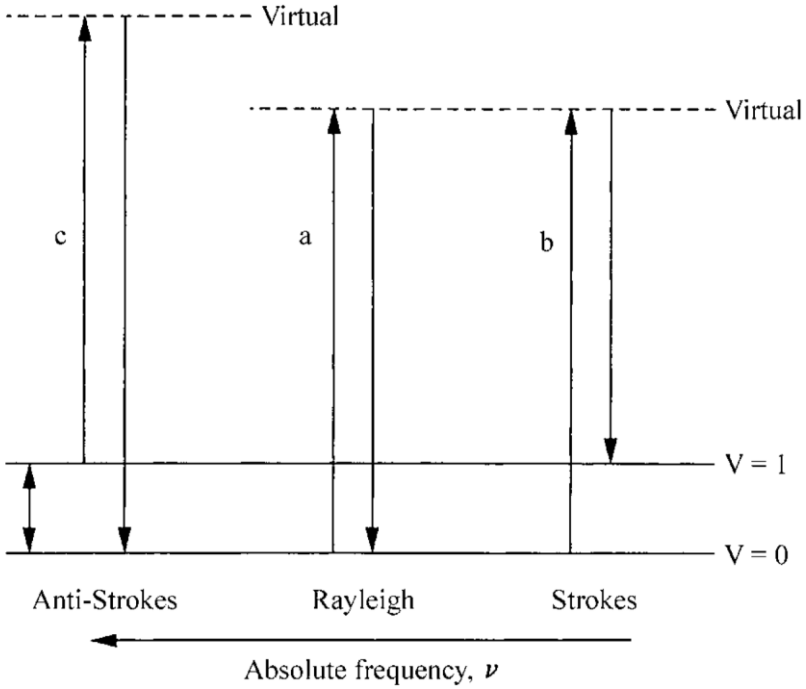

Figure 2-13. Dynamics of different molecular vibration modes [3].

2.4.2 Advantages in compositional and strain-state analyses

Raman spectroscopy is a favourable characterisation approach in various fields such as in ceramic and polymeric materials, due to the simplicity of sample preparation and efficiency, as well as semiconductor composition, strain detection and crystallographic orientation determination. An example is identification of

$Si_{1-x}Ge_x$ composition variation. As can be seen in Figure 2-14 (a) of the Raman spectrum of $Si_{0.7}Ge_{0.3}$ on silicon substrate, the distinct vibrational states of Ge-Ge, Si-Si and Si-Ge bonds show three different Raman peaks. We should note that the Si-Si bond in the thin $Si_{0.7}Ge_{0.3}$ film shows different Raman shift compared to pure Si substrate because strain also affects the chemical bonds thus altering the Raman shift. The vibrational energy is exponentially influenced by the bond length. Figure 2-14 (b) shows the Raman shift of $Si_{1-x}Ge_x$ with the change of x value, and for different film thicknesses. In thinner films in the range of 50-100nm, compressive strain remains because of the lattice mismatch between Ge and Si affecting the Raman shift relation with x as indicated by the solid line, while in thicker films where strain is relaxed by generation of crystalline defects the Raman shift is closer to the fully relaxed dotted line. Another example of the effect of strain on Raman shift is exhibited in Figure 2-14 (c) where the Raman shift of thin silicon film grown on sapphire is compared with pure bulk silicon. In summary, Raman spectroscopy is a good way to analyse the strain when composition of the material can be determined by other means.

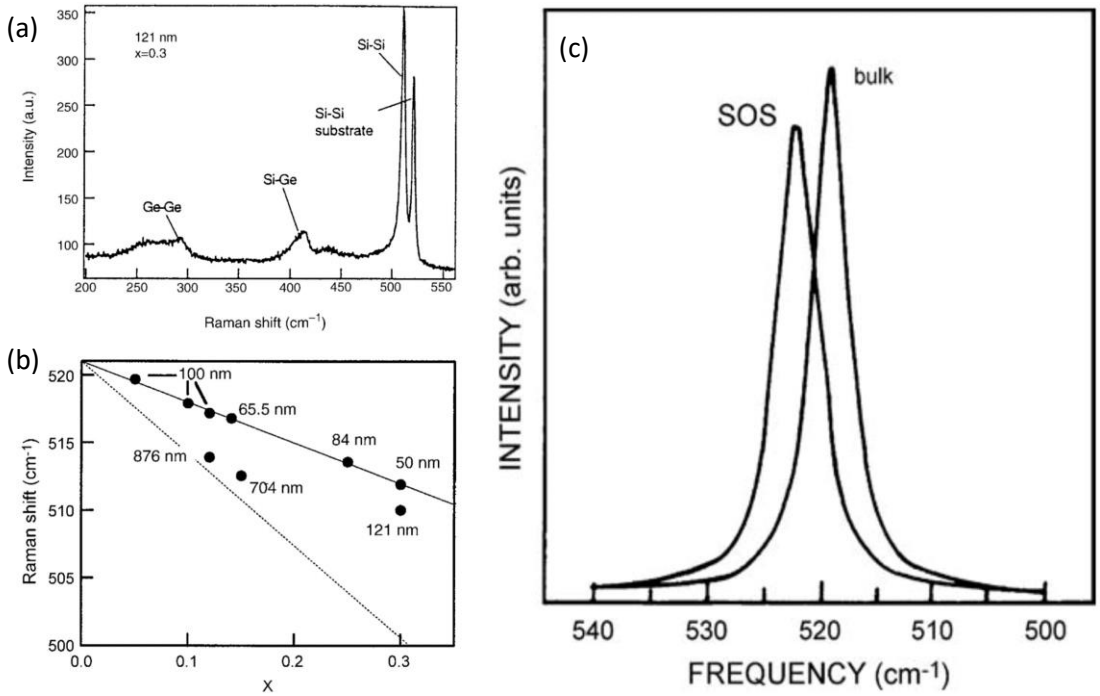

Figure 2-14. Raman spectra of SiGe alloy (a) and its change with layer composition (b); Si on sapphire (SOS) compared to bulk Si (c) [3].

2.5 Scanning Electron Microscopy (SEM)

The SEM is the most frequently used type of electron microscopy [3]. It examines the microscopic structure of a specimen surface by scanning a focused electron beam over the surface area of the specimen. Compared to a standard microscope, the most

important feature of a SEM is a large depth of field. To be specific, the depth of field can reach the order of micrometres at 10^4 × magnification [3]. Moreover, SEM systems are easier to operate and maintain compared to transmission electron microscopy (TEM). Chemical composition analyses are also applicable by equipping the X-ray energy dispersive spectrometer (EDS).

The schematic structure of a SEM system is shown in Figure 2-15. It consists of an electron gun and a set of electromagnetic condenser lenses and apertures. The electron gun for generating an electron beam is usually either a thermionic or a field emission type gun. The acceleration voltage for the generation of an electron beam is in the rage of 1 – 40 kV. The generated electron beam is then condensed to a fine probe for surface scanning through the electromagnetic condenser lenses. The objective lens then focusses the electron beam as a probe with a diameter in the nanometre scale. The beam scanning function is enabled by the beam reflection system incorporated within the objective lens, which is controlled by two pairs of electromagnetic coils and moves the probe in a line along the specimen surface and then displaces to the next line for scanning. The emitted signal electrons from the sample are collected by a detector and amplified and finally used to reconstruct an image.

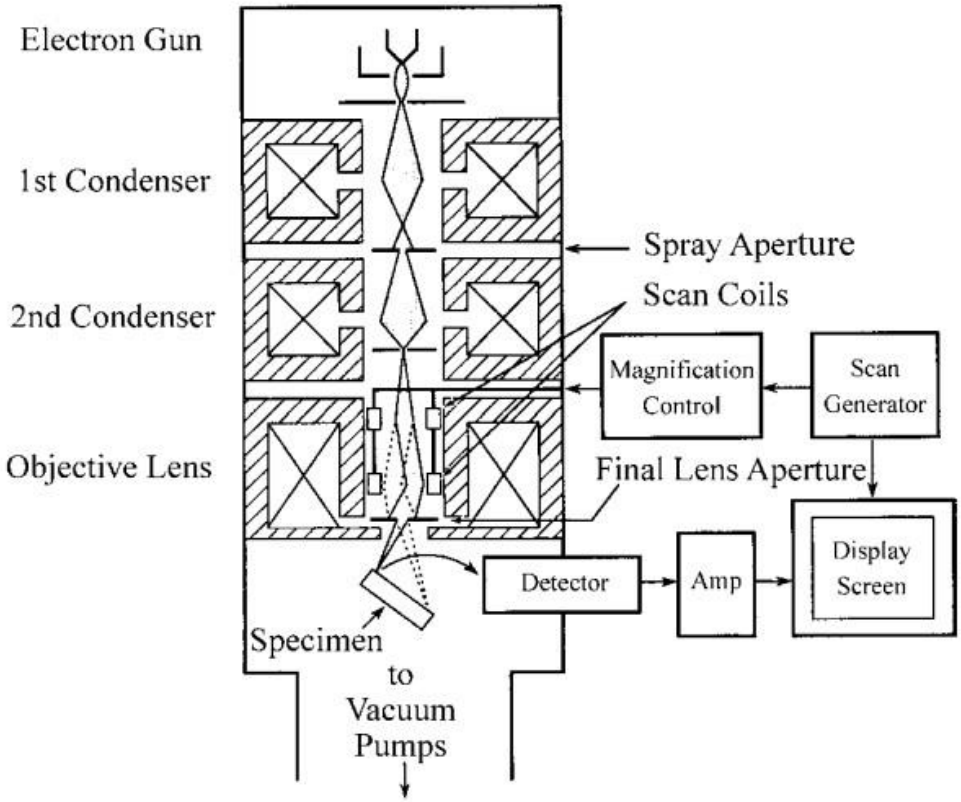

Figure 2-15. The schematic structure of a SEM system [6].

There are two types of signal electrons that are useful for the research in this thesis: secondary electrons and backscattered electrons. When the sample is hit by high energy electrons, it either produces elastic scattering by backscattering the incident electrons or produces inelastic scattering by ejecting electrons from atoms in the specimen. These two types of signal electrons are named backscattered electrons and secondary electrons, respectively. Backscattered electrons are usually deflected from the sample at large angles and with little energy loss while secondary electrons are deflected from the sample at smaller angles but with higher energy loss. Secondary electrons are the main signals for probing topographic contrast, while backscattered electrons are primarily significant for achieving elemental composition contrast. By using the backscattered electron detector, the channelling of electrons down the lattice planes of crystalline materials can be probed. When the incident electron beam path through different crystal lattice orientations changes, the backscattered electron intensity will vary, resulting in a greyscale contrast image for different grains. This approach is called an electron channelling contrast imaging (ECCI) method, an example is shown in Figure 2-16 (a). The TDs reaching the surface show up as the contrasted spots. The TD density of a sample can be estimated by dividing the counted number of TDs by the measured area. Another image taken using secondary electron is also shown in Figure 2-16 (b). ECCI is now widely used as a feasible and accurate approach for dislocation revealing because in a relatively flat oriented sample, the presences of individual dislocations can cause a significant backscattered-electron intensity change when the crystal lattice orientation of a specific grain satisfies the two-beam diffraction condition. The two-beam condition is achieved by tilting the sample such that only one diffraction vector with small Miller indices is excited and satisfying the Bragg condition.

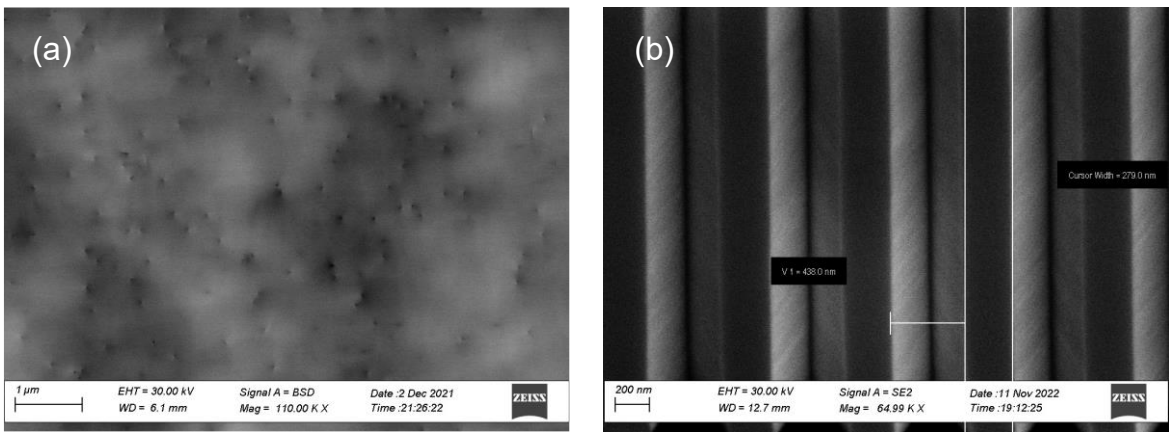

Figure 2-16. (a) An ECCI image shows TDs presenting on the sample surface under backscattered electron mode. (b) An example of secondary electron mode SEM image of the patterned Si substrate.

2.6 PL

PL is an essential optical characterisation tool widely used for various semiconductor materials such as epitaxially grown III-V and group IV semiconductor materials. It is a non-destructive technique allowing the assessment of the bandgap, defects and impurities, and quality of the material under investigation. PL involves the photon emitting process where the sample is excited by an optical source with higher photon energy. For a semiconductor sample under excitation, the electrons in the valence band will be excited into the conduction band, and after the energy transition within the bands and vibrational relaxation to the band edge, carriers will start to recombine and form electron-hole pairs and emit photons with the energy equals the bandgap when they relax back to the valence band. In this way, the bandgap information can be obtained from the PL spectrum. In addition, as the recombination process may involve both radiative and non-radiative processes at the same time, the PL intensity will provide a hint for the crystalline quality as defects usually act as non-radiative recombination centres that deplete carriers for light emission.

The room temperature PL setup used in this thesis consists of three different wavelength excitation laser sources (532 nm, 635 nm and 980 nm), a sample stage which can be vacuumed, three different gratings with seven energy filters. Upon excitation, the PL emission from the sample can be collected and directed into a monochromator by a set of lens, followed by the selection and filtering by the grating and extended optical routes. Then the signal will reach a detector. Depending on the type of detector selected (either a charge-coupled device camera or an extended InGaAs detector), a wide range of emission wavelengths from visible light to a cut-off wavelength of 2000 nm can be detected in the current PL setup. The built-in PL mapping function provides additional information of the uniformity of the optical properties over the entire area of the wafer and facilitates the epitaxial growth optimisation to a large extent. In addition, temperature-dependent PL spectra can provide more accurate measurements for quantum confined devices, because the increase in temperature can result in thermal escape of the carriers, which may also contribute to the radiative recombination, and redshift of the emission originating from the bandgap change upon temperature variation. A photo of the PL mapping system RPM-2000 used in this thesis is shown in Figure 2-17.

Figure 2-17 The PL mapping system RPM-2000 at UCL.

In addition, a micro-PL measurement system where a surface normal pump configuration can be used to optically pump laser devices by using a 632 nm red emission laser (100ps pulses separated by 100 ns period) as the pumping source is shown in Figure 2-18. The pumping powers are controlled and adjusted by the input current of the pumping source. The pumping beam is focused on the microdisk cavity with a spot size ~ 12 μm in diameter through a x50 objective lens. The emission spectra of the microdisk lasers are collected from the top by using the same objective lens and were further analysed by a monochromator with a InGaAs detector. A long-pass filter is used to block the excitation light from reaching the InGaAs detector. And the near-field intensity profile of the microdisk lasers is collected by the InGaAs detector.

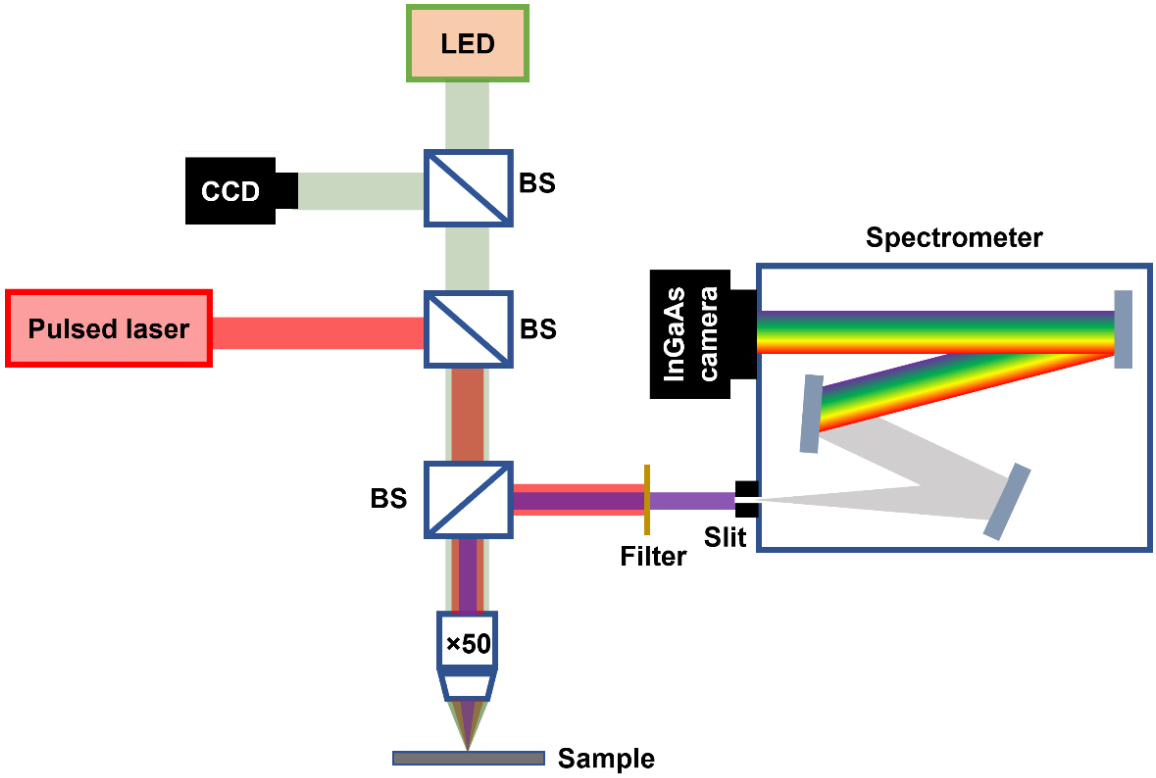

Figure 2-18. Schematic diagram of the micro-PL setup for InAs/InP QDs microdisks characterizations. BS represents beam splitter. A long pass filter is used to block the pumping light from reaching into the spectrometer. To capture the near field image, the grating in spectrometer is replaced by a mirror.

2.7 Transmission Electron Microscopy

TEM is another type of useful electron microscope that generates material microstructures with very high magnification and resolution. The high resolution of TEM comes from short wavelengths of electrons used for microscope illumination and can reach the order of 0.1 nm if lens aberrations can be controlled sufficiently small [3]. Similar to SEM components, TEM consists of electron gun, condenser lens, sample stage, objective lens and projector lens. Using electrons as illumination distinguishes TEM from SEM. The beam in a TEM is highly converged to allow the atomic resolution image and is often used to observe crystal defects. In addition, TEM has special requirements for sample preparation, because the TEM specimens must be thin enough for transmitting electrons, which renders it less flexible and feasible compared to SEM. Grinding, electrolytic thinning, ion milling and ultramicrotomy are the typical methods for preparing thin samples for TEM imaging.

There are two primary modes of TEM imaging, namely bright field imaging revealing levels of transmitted electrons and dark field imaging counting for the scattered electrons. The signal electrons being transmitted and scattered cause the variation in contrast of the image and is used to reconstruct the information about the sample.

Figure 2-19 presents an example of a cross-section TEM image showing crystal defects generated at the interface of Ge and Si substrate. The piled-up lines represent TDs (example marked with white arrows) that originate from the lattice mismatch between Si substrate and subsequently grown Ge epitaxial layers. As most of the TDs are bent to travel horizontally, the top part of the layer shown in the upper half of Figure 2-19 indicates good crystal quality free from TDs, which is of prime importance for achieving high-performance devices. The author greatly appreciates Dr. Mateus Gallucci Masteghin for measuring TEM images of Ge epilayers on Si.

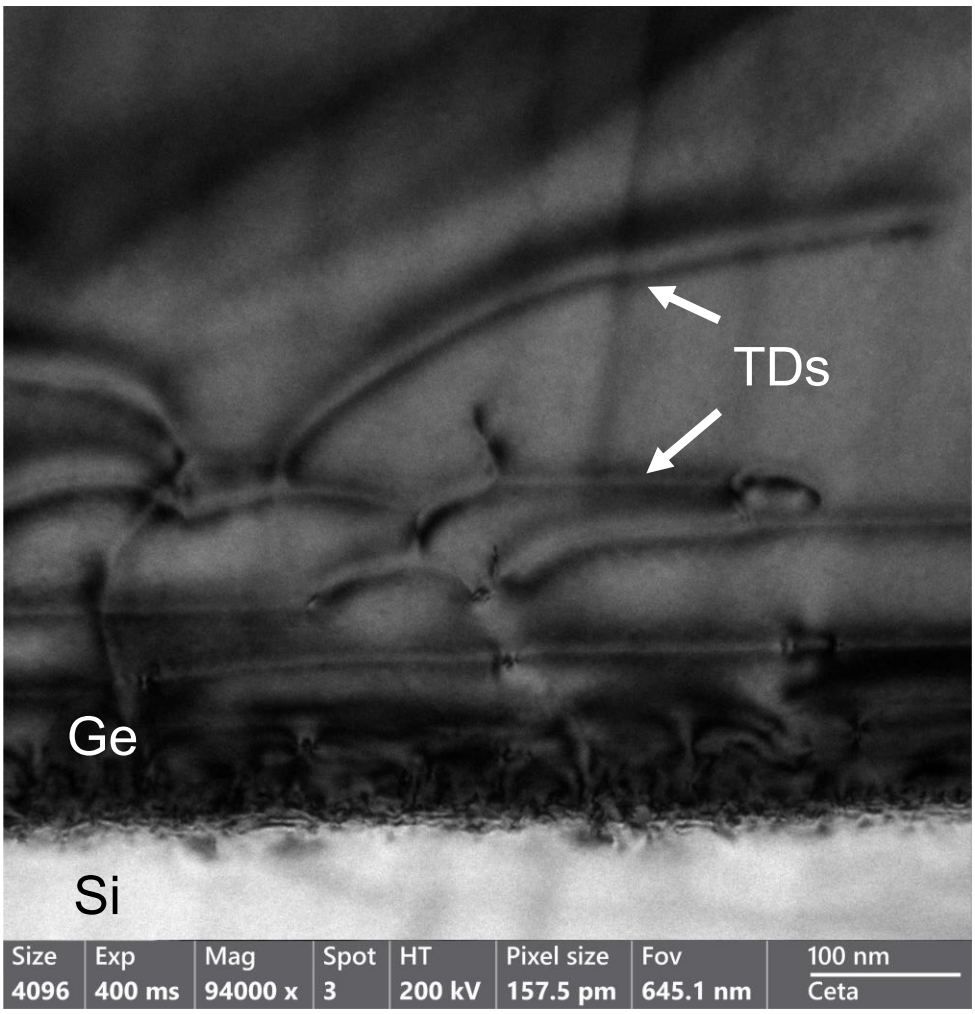

Figure 2-19. A cross-section TEM image showing the crystal defects generated at the interface of Ge and Si substrate. The white arrows denote the position of TDs bent horizontally.

2.8 References

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Chapter 3.

The Growth Optimisation of Low Defect Density Ge Buffer on Si

3.1 Introduction

Driven by the rapidly expanding demand for data transmission in large-volume markets, e.g., data links in data centres and supercomputers, Si-based photonic integrated circuits have been heavily investigated as a desired solution for the high-bandwidth, high-speed and low-cost data communication [1]. However, practical applications are hindered by poor light emission properties due to the indirect-bandgap nature of Si. Currently, compared to hybrid approaches like wafer bonding, the monolithic integration of III-V lasers on Si is one of the most promising alternatives in terms of high throughput and potential scalability. However, the epitaxial growth of III-V material on Si remains challenging because of the presence of large quantities of crystal defects including TDs, APBs and microcracks, as described in Section 1.2. These crystal defects will act as non-radiative recombination centres depleting carriers for lasing. Methods to eliminate the defects include the application of thick III-V buffer layers [2, 3], strained-layer superlattices (SLSs) or QDs as dislocation filter layers (DFLs) [4, 5], patterned Si substrate [6, 7], etc. Usually, these methods will be used in

combination to achieve a low-defect-density platform (in the range of ~ 10^6 cm^{-2}) for subsequent laser structure growth, which in turn results in large buffer thickness (> 2.5 μm) that renders the generation of micro-cracks and reduced coupling efficiency to bottom waveguides. The aspect ratio trapping method using patterned Si substrate can reduce the defect density without significantly increasing the total buffer thickness, but it will add a fabrication burden and address extra difficulties for growths by MBE where the surface cleanliness is dispensable.

On the other hand, partially replacing the thick GaAs buffer layer on Si with Ge/Si accommodates the large lattice and thermal mismatches between GaAs and Si, leaving a low-defect-density surface without significantly increasing the total thickness. Besides, the heteroepitaxy of Ge on Si is also fundamental to group-IV electronic and optoelectronic devices such as GeSn lasers, Ge transistors and Ge photodetectors [8] on Si. It has been reported that by growing only 270 nm Ge on Si substrate, the threading dislocation density (TD density) (6.1×10^8 cm^{-2}) can be reduced to the same level of 1300 nm GaAs on Si [9]. A high operating temperature of 130 °C has also been demonstrated for InAs/GaAs QD laser grown on such GaAs/Ge/Si templates [10]. Moreover, as the TD density of 270 nm Ge on Si is still in the 10^8 cm^{-2} range and the TD density difference after the several DFL layers is not obvious [10], more effective ways of leveraging beneficial effects of Ge buffer and DFLs to enable lower surface TD density and total buffer thickness are possible. In this chapter, the growth optimisation process of Ge on Si is first demonstrated by varying a series of growth parameters, aiming to obtain a low TD density. Then, the TD density change with Ge thickness (from 300 nm to 1000 nm) is investigated to show the trend and find the plateau of the TD density reduction. These investigations will facilitate the buffer design for both III-V and group-IV optoelectronic devices on Si.

3.2 Challenges and The Epitaxial Growth Methods of Ge on Si

As a promising platform for the integration of III-V materials on Si, the growth of Ge on Si has long become of great research interest. However, there is a relatively large lattice mismatch (4%) between Ge and Si, the heteroepitaxial growth of Ge on Si thus will proceed through Stransky-Krastanow (SK) or Volmer-Weber (VW) modes, where three-dimensional (3D) islands are formed to relax the strain and spontaneously introduce a large number of defects. The illustrative images of three growth modes are

shown in Figure 3-1. When the deposited material has a same or a small lattice mismatch with the substrate, it will grow layer-by-layer (Frank-van der Merwe (FW) growth mode), as shown schematically in Figure 3-1 (a), an example of which is the deposition of Ge on GaAs. During the epitaxial growth of a material on a several-percent-smaller-lattice substrate, e.g., InAs on InP where the lattice mismatch is 3.2%, the growth will first follow two-dimensional (2D) growth mode within several atomic layers [11]. Then the growth will proceed through the formation of three-dimensional (3D) islands. This is known as the SK mode (island and layer growth mode), as seen in Figure 3-1 (b). The transition thickness is called a critical thickness, and the 2D layer is named as wetting layer. The formation of the islands originates from the elastic relaxation of the mismatch strain and is energetically favourable. This self-formation of the 3D islands through SK growth mode is called a self-assembly process critical for the synthesis of semiconductor nanostructures [12]. The advantages are that the process is one simple deposition step, and the density, size and uniformity can be easily controlled by varying growth conditions. Besides, as the strain is relaxed elastically, crystal defects can be avoided by choosing the deposition thickness below the island plastic relaxation. Defect-free QDs can be grown using this method. The third growth mode is VW mode (island growth mode) (Figure 3-1 (c)), where the interactions between adatoms are stronger than that between adatoms and the substrate atoms. Therefore, 3D islands or clusters are form directly onto the substrate. Ge on Si growth follows the SK mode and suffers from two major challenges: 1) high density of threading dislocations (TDs) and 2) large surface roughness because of island growth. Those high-density TDs originating from the Ge/Si interface can propagate to the active regions in devices either depleting carriers of a laser or increasing the leakage current of a rectifying junction significantly deteriorating device performance. And the rough Ge epilayer will result in difficulties in process integration.

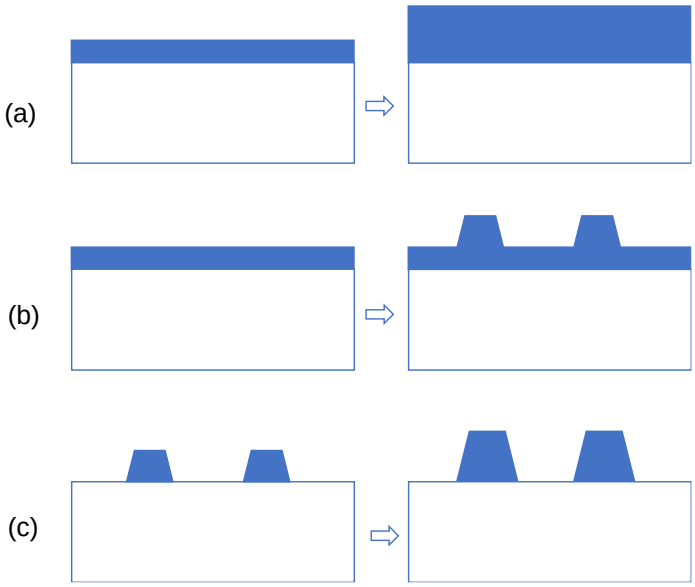

Figure 3-1. Schematic illustrations of epitaxial growth modes of semiconductor materials. (a) Frank-van der Merwe (layer-by-layer growth); (b) Stranski-Krastanov (island and layer growth mode); (c) Volmer-Weber (island growth mode).

From the perspective of epitaxial growth, to address the issue of high surface roughness, two strategies are most widely used: 1) lowering the growth temperature so that the diffusion of adatoms on the deposited surface is greatly suppressed. This will prevent the adatoms from locating their energetically preferred positions. In other words, it will avoid the formation of 3D islands. Nonetheless, the high defect density is a consequence of low-temperature growth because substantial point defects can be introduced to the film at low growth temperatures. As a result, only the nucleation phase of Ge growth on Si is typically carried out at low temperatures. 2) The use of surfactants. By careful selection of surfactant atoms, it is possible to passivate the surface by saturating most of the dangling bonds on the surface; thus, the deposited atoms will not differentiate between flat surfaces and step edges, favouring layer-by-layer growth [13-16]. Passivation should be adequate from suitable surfactant atoms. For example, pentavalent Sb atoms are preferable to tetravalent Sn atoms as surfactants for passivating tetravalent Si substrate [13].

Methods to eliminate the TD density are mainly threefold. 1) The insertion of graded SiGe buffer layers between Ge and Si substrate is a standard approach that has been well-studied. This method can gradually accommodate the lattice mismatch by the grading of Si composition. The drawback of this method is that it usually involves large epitaxial thickness and thus elevated surface roughness. For example, combined with chemical-mechanical polishing, the TD density can be decreased to 2.1×10^6 cm^{-2} [17]. However, the epitaxial thickness added up to 12 μm and the root means square

(rms) was 24.2 nm. Facilitated by Sb surfactant, the TD density of a 4 μm SiGe graded buffer on Si can be improved to 5.4×10^5 cm^{-2} with a rms roughness of 3.5 nm [16]. 2) Two-step growth is generally adopted where the initial growth is carried out at low temperature (LT) to facilitate the 2D nucleation, followed by high-temperature growth and cyclic thermal annealing [18]. High-temperature (HT) growth is beneficial for the crystal quality and surface morphology and will help to remove point defects introduced in the low-temperature step. Thermal stress-induced dislocation glide and annihilation during thermal cycling annealing is the stimulus for defect reduction. Besides, the thermally induced Si diffusion into the epilayer is reported to decrease the TD velocity [19] and the difference in TD velocities in Si diffused region and the 'undoped' region gives rise to the bending of TDs [20]. Moreover, 60° dislocations can react and form pure edge dislocations during thermal annealing process [21, 22]. A schematic demonstration of the TD reduction mechanism induced by high-temperature thermal annealing is shown in Figure 3-2. The as-grown film is composed of a 60° TD threading up to the surface (Figure 3-2 (a)). Under high-temperature thermal annealing, the thermal stress and increase vacancies facilitate TD motion within the film (Figure 3-2(b)). Meanwhile, in the case of GaAs growth on Si, the Si diffusion can also lead to a slow-down of the TD moving in the Si-diffused region, and the TD propagation velocity difference at the interface of the Si-doped region and undoped region bends the TD and eventually TDs can form pure edge dislocations, see Figures 3-2 (c) - 1 – 3. For 60° TDs with opposite Burgers vectors, they can react and disappear from the surface, as shown in Figure 3-2 (d) - 1 – 3 [20]. Besides, annealing temperatures can be carefully selected to maximise dislocation velocity, hence increasing the chance of self-annihilation [18]. An intermediate layer grown between LT and HT layer with a growth temperature gradient has also been introduced both for chemical vapour deposition (CVD) [23, 24] and molecular beam epitaxy (MBE) [25]. The mechanism behind this intermediate layer for TD density reduction is based on thermodynamics. As has been well-studied, partial dislocations on certain low-index glide planes can either annihilate or fuse through the diffuse glide and climb [21]. However, there exists an energy barrier for TD gliding and the probability of a TD trying to overcome the energy barrier is related to the temperature and time between LT and HT [25]. Consequently, a lower temperature ramping rate is preferential for the pursuit of reducing TD density. 3) Using high concentration ($> 10^{18}$ cm^{-3}) donor dopants like Sb or As is proven to boost dislocation velocity [26], thus increasing the probability of

dislocation annihilation. A single-bond energy model has also been reported to explain the observed increase in TD velocity by As incorporation [27]. Given the weaker As-Ge bond energy than Ge-Ge bond estimated from the model, the dislocation propagation enabled by successive breaking bonds close to the TD is enhanced. A TD density reduction of 1×10^8 cm^{-2} has been achieved with 5×10^8 cm^{-2} Sb doping in the LT Ge layer and a final TD density of 2.6×10^8 cm^{-2} was realised by a 500 nm Ge buffer layer on Si [9].

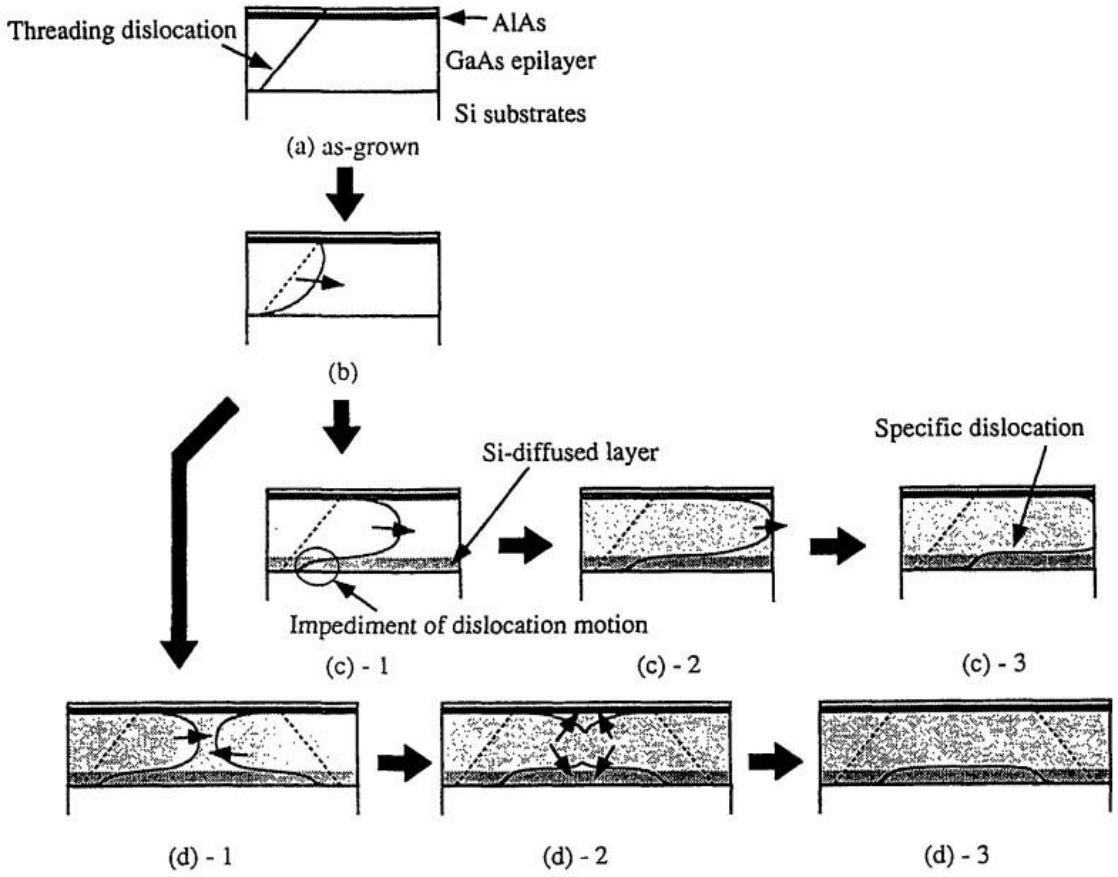

Figure 3-2. TD reduction mechanism enabled by high-temperature thermal annealing. (a) A schematic image of 60° dislocation presents in as grown GaAs film on Si. (b) TD motion during high temperature annealing because of thermal stress and increased vacancies. (c) – 1 – 3 The schematic illustrations of impeded TD motion in the Si-diffused layer. The difference of TD velocities in the interface of Si-doped layer and undoped layer results in the TD bending effect and the formation of pure edge dislocations. (d) - 1 – 3 TDs with opposite Burgers vectors react and form a closed loop at the Si diffusion interface or annihilate with each other [20].

Besides, the method used to count TD density is also important for the investigation of defects in Ge/Si growth. Etch-pit density counting (EPD) is more suitable for low TD density in the range of ~ 10^6 cm^{-2}, where plan-view transmission electron microscopy (TEM) measurement results tend to be inaccurate. The shortcomings of EPD are that in higher TD density levels i.e., over 10^8 cm^{-2}, etch-pits may merge with their neighbour and make EPD statistically unsound and on the other hand, the high TD density will

challenge the resolution limit of the optical microscope as well. From our experience, the counted number may also be affected by the stoichiometric concentration of the etchant and the etched surface may suffer from uneven etch rates thus leaving a nonuniform surface, as shown in Figure 3-3. Besides, for low surface roughness samples, the TDs can also be counted clearly from AFM images, however, with the increase of surface roughness, TDs in the valley of the surface may not be detected effectively, as indicated by the areas inside the white circles in Figure 3-4. In contrast, electron channelling contrast imaging (ECCI) results are almost not affected by the sample preparation, and the operation is more feasible. The existence of a defect will cause the coherency of the crystal lattice and the channelling primary electron wave field to be disturbed, followed by strong backscattering at the defect site. An example of ECCI image is shown in Figure 3-5. Consequently, the defect will appear as a highly contrasting feature compared with its background when a backscatter electron detector is used in an SEM for sample observation. ECCI can be generally used for both low defect density as well as high defect density samples by adjusting the magnification according to requirement.

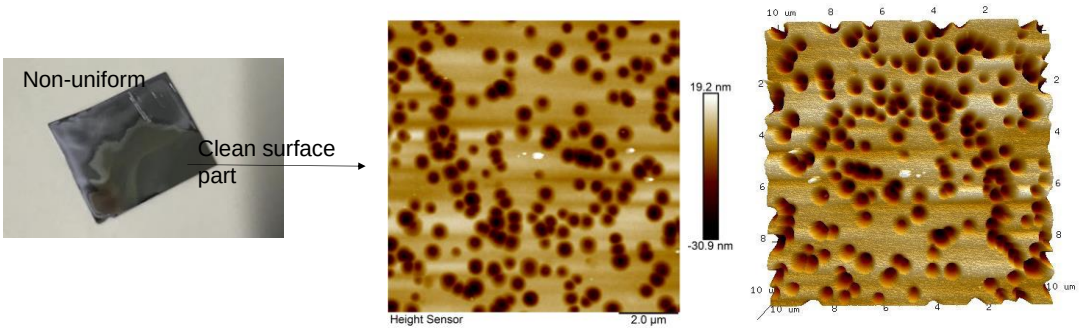

Figure 3-3 Plan-view etch-pit density AFM images of the surface of the clean part of a Ge/Si sample. The etchant used is $CH_3COOH/HNO_3/HF$ (67:20:10) solution without I_2.

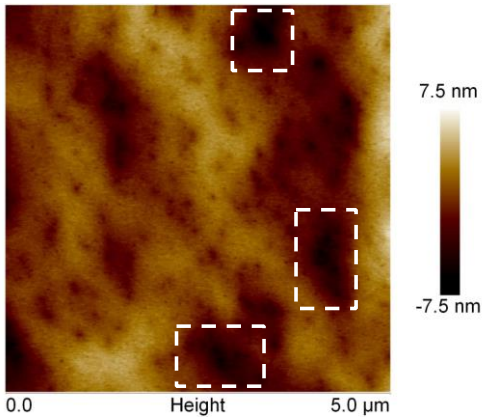

Figure 3-4 Atomic force microscopy (AFM) image of the surface of a 300 nm Ge/Si sample. Areas inside white circles are valleys of the surface where threading dislocation counting is impractical.

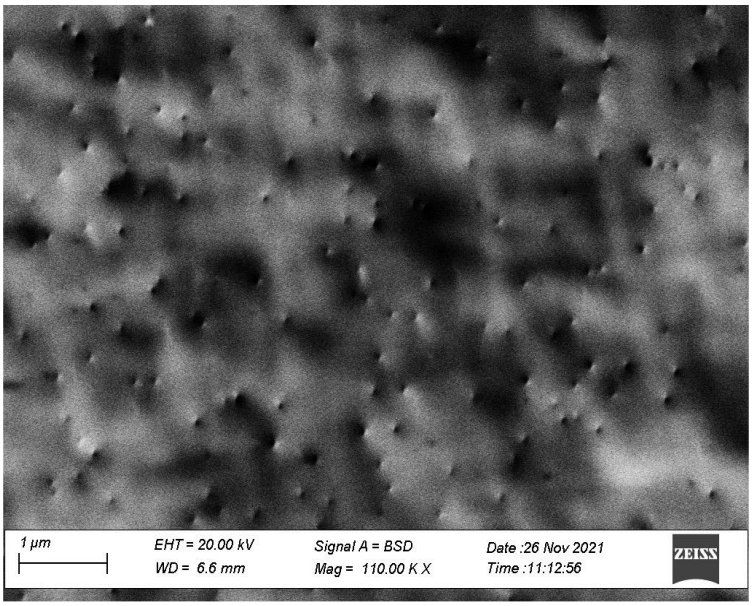

Figure 3-5 Electron channelling contrast imaging (ECCI) of the surface of a 400 nm Ge layer on Si substrate. The counted threading dislocation density (TD density) is 2.47 × 10^8 cm^{-2}.

3.3 Growth optimisation of Ge on Si

In this section, three-step growth method with an intermediate temperature-ramp layer, surfactant Sb and thermal cycling were adopted as a starting point. To optimise the Ge/Si growth to lower TD density and maintain a smooth surface within acceptable overall thickness as a buffer for III-V lasers integrated on Si, mainly two series of samples are discussed. In the first series of samples, focuses are put on the fundamental growth aspects including the comparison between temperature-ramp middle-temperature (MT) layer and temperature-constant MT layer, the growth temperature of the low-temperature (LT) layer with Sb doping and the temperature of the thermal cycling, the effect of Sb pre-layer and co-doping in the LT layer, with a thin Ge layer of 300 nm. The aim is maintaining a thin buffer thickness while reducing the TD density. In the second series, more details into the doping species, the growth rate of the LT with doping layer, and temperature-ramp layer thickness, and TD reduction with layer thickness for doped and undoped samples were investigated and compared based on the promising preliminary results of the 300 nm samples. N-type 4° offcut toward <110> Si substrates were used for all the samples grown in this project. AFM was carried out for surface morphology probing and TD density counting; ECCI and transmission electron microscopy (TEM) measurements were applied to present the crystal quality of samples. TEM results demonstrated in this chapter were performed by our collaborators from the University of Surrey, as highlighted in the Acknowledgements.

3.3.1 Effects of intermediate temperature-ramp layer

At first, the effects of the intermediate temperature-ramp MT layer are investigated. For comparison, three samples with a thickness of 300 nm Ge were grown on Si. The N^+ 4° offcut Si (001) substrate was first baked in the load-lock (LL) chamber at 200 ˚C to remove any water. Then, it would be degassed in the preparation chamber on the degas station at 600 ˚C for 1 hour. The final step before epitaxial growth was to deoxidise the wafer at 1000 ˚C for 0.5 hours to remove surface oxide. The growth schematic structures are shown in Figure 3-6, which were all initiated by an LT Ge seed layer grown at 300 ˚C. Then the intermediate layers were grown at 525 ˚C (marked as MT) for the first two samples, their thicknesses were 180 nm and 220 nm, respectively. The intermediate layer of the third sample was grown with a continuous temperature ramp from the LT to 525 ˚C with a ramp rate of 9.2 ˚C/min. The principle is that the growth rate should be high to match the high atom mobility at elevated growth temperature because a low growth rate at high temperature will easily lead to 3D growth mode and that the ramp rate should be low to ensure enough time for defects to glide. Therefore, we used the highest growth rate that can be obtained from our Ge sources available for the intermediate layer growth, and the ramp rate is calculated by dividing the thickness by the growth rate. Then the growth was followed by thermal cycling between 900 and 600 ˚C for four repeats and finished by HT Ge grown at 600 ˚C. The annealing temperatures and number of repeats were selected based on the studies reporting that higher annealing temperature (> 700 ˚C) results in a more efficient TD density reduction [22, 28] and this effect will start to saturate after around four repeats due to reemission accompanied by the coalescence of TDs and new TDs generation [22]. 5 × 5 μm^2 AFM images of the samples are presented in Figure 3-7 (a – c), and the root mean square (rms) roughness and TD density are summarised in Figure 3-7 (d). The TD densities for the samples with 180 nm MT layer, 220 nm MT layer and 220 nm ramp temperature layer are 6.08 × 10^8 cm^{-2}, 5.4 × 10^8 cm^{-2}, 4.8 × 10^8 cm^{-2}, respectively. It can be concluded that a relatively thick temperature-ramp layer (220 nm) is more advantageous for both low surface roughness and TD density reduction for a sample with a total thickness of 300 nm.

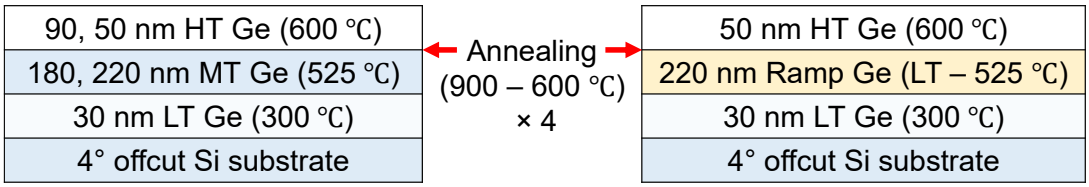

Figure 3-6 Schematic diagrams of Ge/Si without and with temperature-ramp layer.

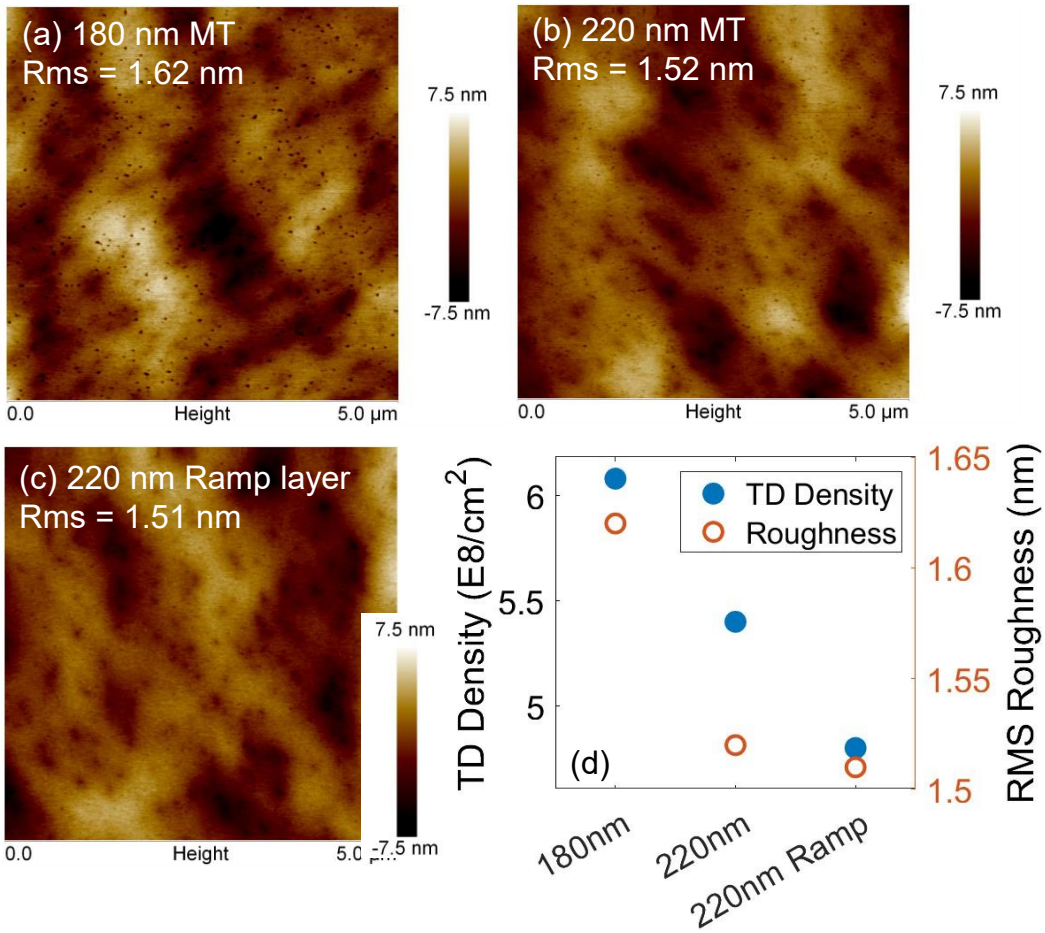

Figure 3-7 AFM images of samples with different intermediate layers (a – c). (d) TD density and root mean square (rms) roughness of the samples.

Moreover, the effects of the thickness of the temperature-ramp layer were also investigated for Sb-doped LT layer samples. The comparison was carried out on two 500 nm Ge/Si samples. The schematic diagrams and the corresponding ECCI images of grown structures are shown in Figure 3-8. One sample was grown with a 385 nm temperature-ramp layer (Figure 3-8 (a)), followed by thermal cycling, and finished by 65 nm HT Ge. As an extreme case of increasing the thickness of the temperature-ramp layer, the other sample was grown completely without the HT layer (Figure 3-8 (b)). The 385 nm ramp layer sample has a TD density of 1.31×10^8 cm^{-2}, while the

450 nm ramp layer sample has a slightly higher TD density of 1.54 × 10^8 cm^{-2}, as can be seen from Figure 3-8. This result demonstrates that the high temperature layer is indispensable for high quality Ge growth on Si and has been verified with thicker samples. Based on these results, the temperature-ramp layer thickness for 300 nm Ge/Si samples is set as 220 nm and that for 500 nm Ge/Si samples is set as 385 nm.

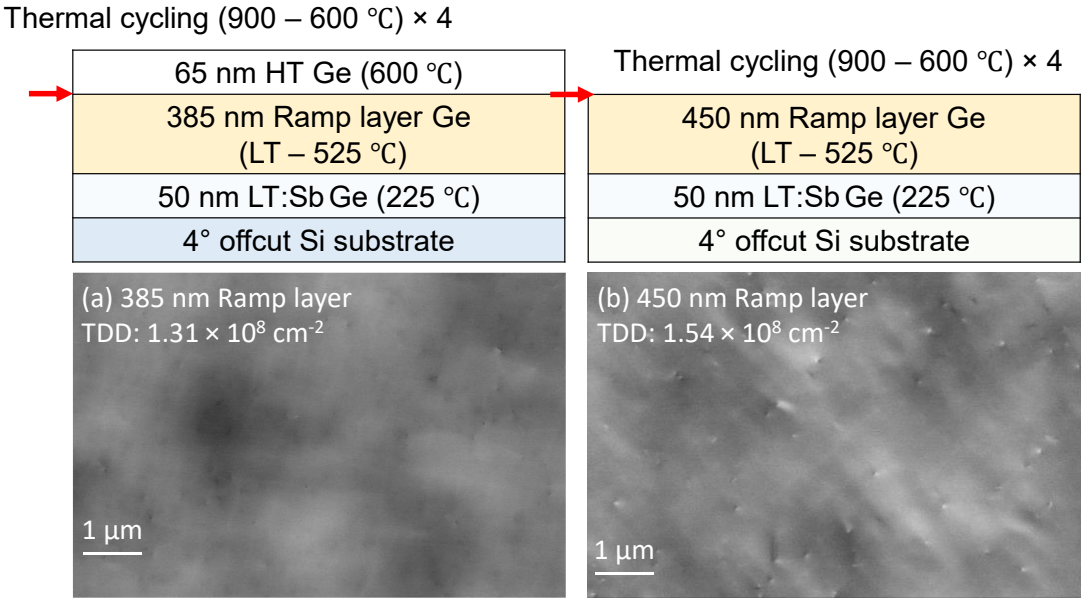

Figure 3-8 Schematic diagrams and corresponding ECCI images of samples with (a) 385 nm and (b) 450 nm intermediate ramp layers.

3.3.2 Effects of doping

The effects of doping on surface roughness and TD density reduction have been studied in this section aiming to find the appropriate doping density at proper doping temperature. It has been reported that high concentration (> 10^{18} cm^{-3}) n-type dopant As can increase whereas p-type dopant Ga will decrease the dislocation velocity in Ge and that the dislocation velocity rises with increasing doping concentration [26, 29]. However, on the other hand, 1 ML As aided Ge growth on Si (001) substrate has also been demonstrated to introduce strain-induced V-shape defects that cannot be overgrown [30]. On the contrary, making a monolayer of Sb float on the epi-surface can not only achieve strain relief but also leave a defect-free epitaxial Ge film on Si (111) substrate by a self-annihilation mechanism [15]. In addition, group-V elements such as Sb and P provide better passivation of step edges of Ge than group-IV elements like Sn. Therefore, in the first instances, four samples with high Sb doping concentrations were grown. The doping densities were 1 × 10^{19} cm^{-3}, 5 × 10^{18} cm^{-3} in the LT layer and 1.5 × 10^{18} cm^{-3} in the ramp layer, 5 × 10^{18} cm^{-3} in the LT layer and background doping in the ramp layer, 5 × 10^{18} cm^{-3} in the LT layer, respectively, and

were grown at a substrate temperature x_T for LT layer, where x_T = 275 ˚C. The total thickness of these four samples is 300 nm. The schematic diagrams of the grown structures are shown in Figure 3-9. However, these four samples suffered from severe material segregation and the epilayer surface was milky due to Sb accumulation at the surface. Therefore, a substrate temperature of 275 ˚C is considered to be too high for Sb concentrations over 5 × 10^{18} cm^{-3}.

50 nm HT Ge (600 ℃)
Thermal cycling (900 – 600 ℃) × 4
220 nm Ramp Ge (LT – 525 ℃)
30 nm LT Ge (x_T ℃): with Sb (x_D × 10^{18} cm^{-3})
4° offcut Si substrate

Figure 3-9 Schematic diagram of the grown structures with Sb doping in LT Ge layer.

Then the doping temperature was maintained at 275 ˚C and the doping concentration was reduced to 2.5 × 10^{18} cm^{-3} and 1.25 × 10^{18} cm^{-3} for the next two samples to avoid Sb segregation. After the growth, the sample surfaces are mirror-like, and their 5 × 5 μm^2 AFM images are shown in Figure 3-10. The surface roughness is slightly decreased for the 2.5 × 10^{18} cm^{-3} doped sample compared with the 1.25 × 10^{18} cm^{-3} doped sample, which is 1.06 nm, and the TD density is lower (5.2 × 10^8 cm^{-2}) as well. This means more Sb incorporation is beneficial for TD density reduction. Consequently, the next two samples were grown at lower temperatures 250 ˚C and 225 ˚C, respectively, with 2.5 × 10^{18} cm^{-3} Sb doping to compare the low doping temperature on the crystal quality and at lower doping temperature, it is easier to obtain higher doping concentration without phase segregation. It is shown that with 2.5 × 10^{18} cm^{-3} Sb doping, the TD density level of the sample grown at 275 ˚C is the lowest. Further decreasing the growth temperature is detrimental to defect reduction at this doping concentration (Figure 3-11).

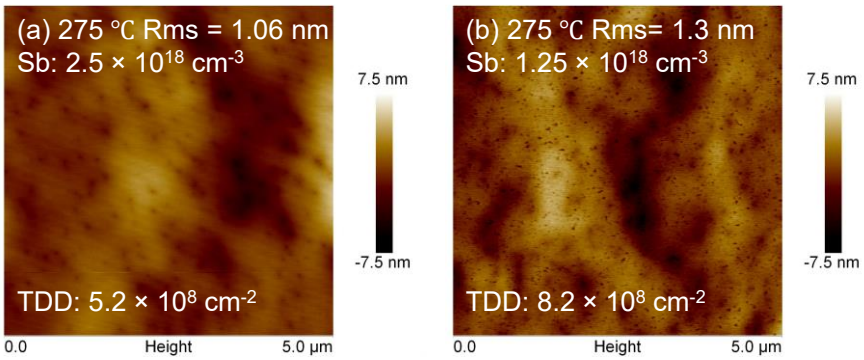

Figure 3-10 AFM images of samples with LT Ge with different Sb doping concentrations grown at 275 ˚C.

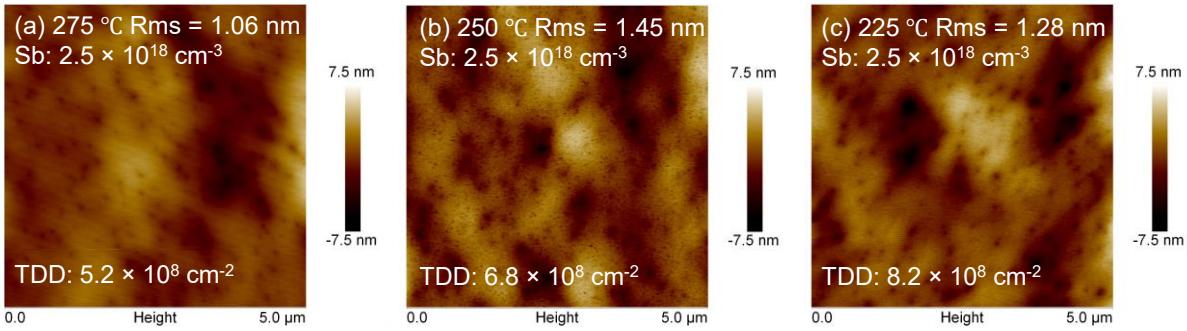

Figure 3-11 AFM images of samples with LT Ge with 2.5 × 10^{18} cm^{-3} Sb doping grown at (a) 275 ˚C, (b) 250 ˚C and (c) 225 ˚C.

Then, a further increase of doping concentration to 5 × 10^{18} cm^{-3} was applied to subsequent samples at different temperatures (225, 200, 175 ˚C) to find the optimal condition, and the results are shown in Figure 3-12 (a – c). A significant reduction in surface roughness is observed for this higher doping regime. A rms roughness of 0.82 nm is obtained from the sample with a LT layer grown at 225 ˚C. Meanwhile, TD density is reduced to 4.4 × 10^{8} cm^{-2}, indicating that a lower growth temperature is more suitable for higher Sb doping density (compared to the optimal growth temperature of 275 ˚C for 2.5 × 10^{18} cm^{-3} Sb doping). Doping temperatures lower than 225 ˚C causes significantly elevated surface roughness (from 0.82 nm to 1.5 nm) and induces a bit higher TD density (from 4.4 × 10^{8} cm^{-2} to 5.4 × 10^{8} cm^{-2}). It infers that a low temperature is required to incorporate Sb, but a too low temperature may lead to suppressed adatom mobility, hindering adatoms to migrate to appropriate lattice sites. Moreover, further increasing the doping density to 1 × 10^{19} cm^{-3} shows a rms roughness of 1.06 nm and a degraded TD density of 6.6 × 10^{8} cm^{-2}, as can be seen in Figure 3-13.

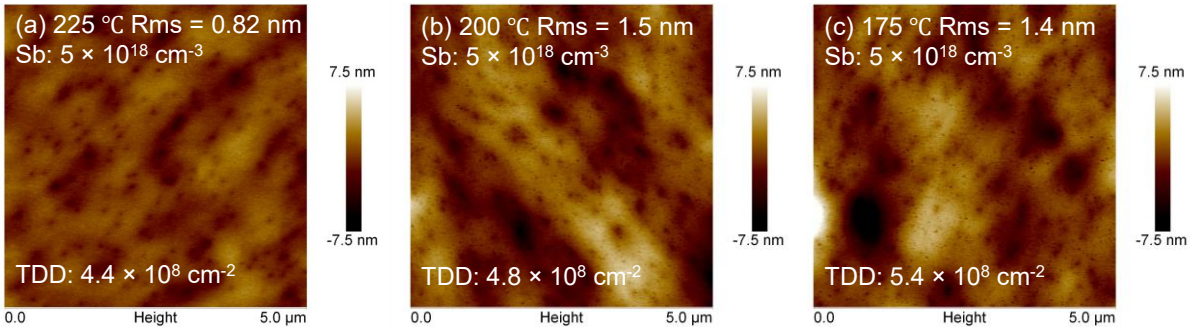

Figure 3-12 AFM images of samples with LT Ge with 5 × 10^{18} cm^{-3} Sb doping grown at (a) 225 ˚C, (b) 200 ˚C and (c) 175 ˚C.

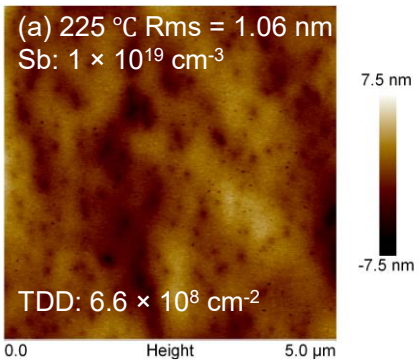

Figure 3-13 AFM image of the sample with LT Ge with 1 × 10^{19} cm^{-3} Sb doping grown at 225 ˚C.

The TD density and surface roughness results of the first series of samples (300 nm) are shown in Figure 3-14. From these results, an optimal doping condition among all 300 nm samples mentioned above is obtained for 5 × 10^{18} cm^{-3} Sb doping grown at 225 ˚C, which results in a TD density of 4.4 × 10^{8} cm^{-2} and a low roughness of 0.82 nm. A trend of TD density change with increasing Sb doping concentration (at the optimal growth conditions for each concentration found in this study) is presented in Figure 3-15. The effect of TD reduction by Sb incorporation in 300 nm Ge grown on Si is maximised around at a doping concentration of 5 × 10^{18} cm^{-3}.

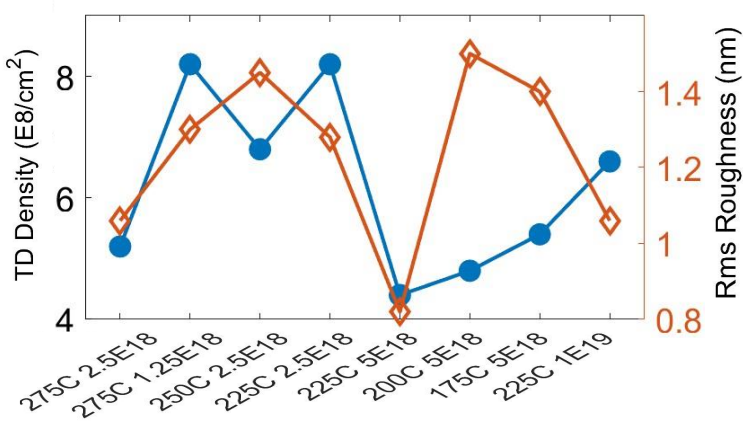

Figure 3-14 TD density (left axis) and surface roughness (right axis) of samples grown at various doping concentrations and temperatures.

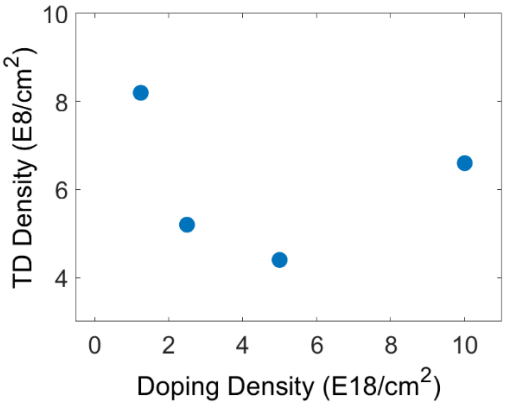

Figure 3-15 TD density change with increasing Sb doping concentration (at the optimal growth condition found in this study) for 300 nm Ge on Si samples.

Later, different doping sequences and species were examined. 1) An Sb pre-layer method was performed in comparison with continuous Sb supply during LT growth. 1 monolayer (ML) Sb growth before Ge deposition was applied by fully opening the Sb cracker cell valve for 5 minutes, after that, no Sb was incorporated and the rest of growth structure was the same, as shown in Figure 3-16. The dopant Sb acts as a surfactant in this experiment, it passivates the surface with low-energy Sb atoms so that deposited atoms will not recognise step edges or flat surfaces. When Ge adatoms are deposited, an exchange process will happen between Sb and deposited Ge atoms, where Sb atoms will always float at the surface, as described in surfactant-mediated epitaxial growth in general [13]. The reason to test this pre-layer method is that the exchange process also requires energy, thus there may exist differences in the effect of roughness and defect reduction between the Sb pre-layer and continuous Sb flux supply, where the epi-surface may be easier to be passivated during growth. The AFM result of the Sb pre-layer method is presented in Figure 3-16 (b). The surface roughness is 0.88 nm, and the TD density is estimated to be 7.0×10^8 cm^{-2} from the AFM image. This result is inferior to the best sample (5×10^{18} cm^{-3} Sb doping grown at 225 ˚C of a TD density of 4.4×10^8 cm^{-2}). It is thus deduced that ensuring enough Sb atoms to passivate the surface during growth is significant to maximise the effects of Sb doping. In this context, combining 1 ML Sb pre-layer and Sb incorporation in the LT layer could be a better option for future growth.

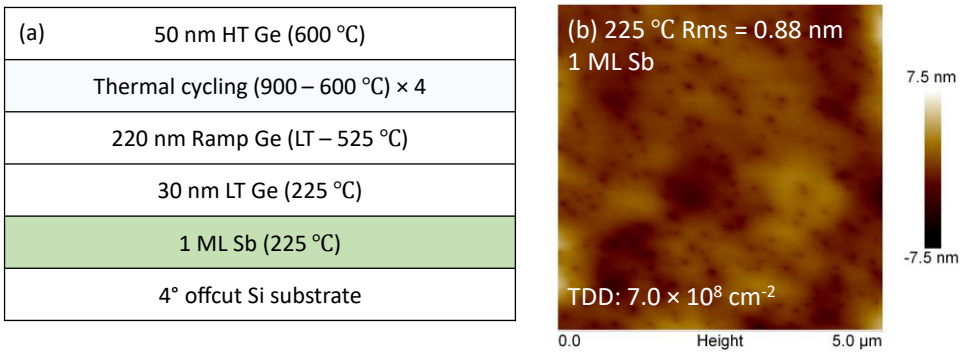

Figure 3-16 (a) Schematic structure and (b) AFM image of the sample with 1 ML Sb before LT Ge growth.

2) Co-doping method has also been investigated because of documented benefits of increasing the total doping concentration and reducing TD density [31]. The co-doping method applies two types of dopants at the same time, the motivation is that the microscopic strain field induced by one type of dopant may facilitate the incorporation of the other type of dopant into substitutional lattice sites. Besides, because Si atoms are smaller than Ge, the compensated strain may be helpful for Sb

atoms to incorporate into the Ge lattice. Therefore, two samples with Si and Sb dopants were grown with different doping structures. For the first sample, Sb and Si were co-doped in the LT Ge at a substrate temperature of 225 ˚C. The Sb concentration was 5 × 10^{18} cm^{-3} while the Si composition was 1%. The schematic growth structure is shown in Figure 3-17 (a). And for the second sample, as we know, the high crystal-quality growth of Si favours high temperatures, the doping of Si is carried out at a relatively higher temperature in the temperature-ramp layer and HT Ge layer and Sb doping is maintained at the LT layer. The schematic growth structure is shown in Figure 3-17 (b). AFM results shown in Figure 3-17 (c) and (d) demonstrate some support for the proposed growth method, that both TD density and rms roughness are improved for the sample where Si was incorporated at a higher temperature. However, compared to the Sb-only LT layer sample grown at optimal condition, the effect of Si seems trivial. Besides, elevated surface roughness compared with Sb-doped-only samples may indicate that tetravalent Si itself is not a promising candidate for Ge surface passivation. Three samples were grown with the same condition to verify the doping effect of Si.

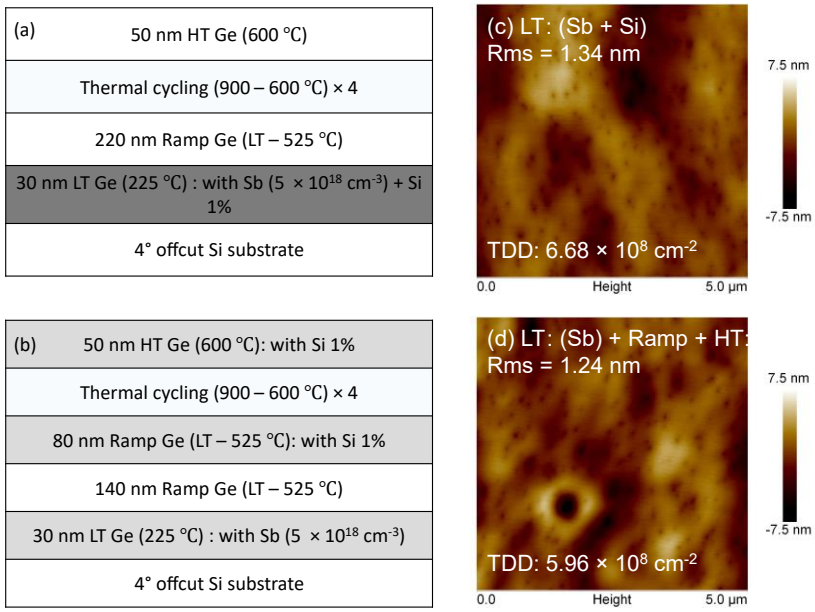

Figure 3-17 Schematic structure and AFM image of Sb and Si co-doped Ge on Si samples

Group-IV surfactant P can be a good candidate for this co-doping method as it is a pentavalent atom, and has been reported to enhance TD mobility [31]. A sample with P doping in the LT layer was investigated for a 500 nm Ge/Si sample (Figure 3-18 (a)), which results a reduced TD density of 1.83 × 10^8 cm^{-2}, as shown in Figure 3-18 (b). Our later experiments (after the submission of this thesis) have demonstrated positive

effects of P doping and co-doping with P and Sb on TD density reduction during the Ge growth on Si.

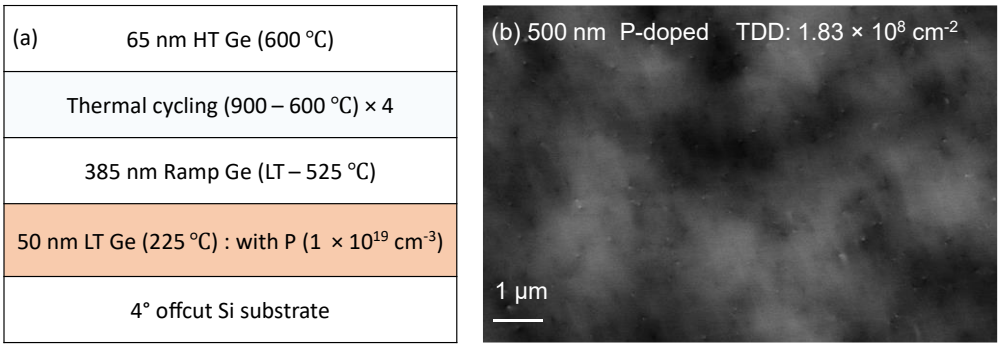

Figure 3-18 (a) Growth structure and (b) ECCI image of P-doped 500 nm Ge/Si.

3.3.3 Effects of thickness

For the second series of samples, the relationship between thickness and TD density was first investigated. This relationship has been well-studied both theoretically and examined experimentally in the literature for un-doped Ge/Si growth to be inversely proportional to layer thickness [21, 32]. The notion of line tension, which is the increase in energy per unit increase in the length of a dislocation line, was proposed to explain the correlation between film thickness and increased TD interaction [33]. The line tension of a dislocation is analogous to the surface tension of a liquid, and it will tend to straighten the line and reduce the total energy by producing forces perpendicular to the dislocation and towards the centre of the curvature. Therefore, considering the attractive force between adjacent TDs within certain spacing, the minimum stable separation can be determined by the balance of the attractive force between TDs and the line tension associated with misfit dislocations [21]. The TD density reduction effect with increasing thickness tends to saturate when TD density gradually becomes smaller and the spacing between adjacent TDs increases. However, the correlation between thickness and TD density for doped Ge has not been sufficiently investigated compared to the undoped Ge on Si growth. In this section, the effects of thickness on TD density reduction have been studied for un-doped and doped Ge/Si and the obtained results will help in choosing the growth parameters for Si-based platforms according to requirements at ease.

300 nm, 400 nm and 500 nm un-doped and doped samples were grown for comparison. For the un-doped samples, the thickness of each layer is shown in Figure 3-19 (a – c). The increase in thickness is mainly inserted in the temperature-ramp layer to allow a higher possibility of TD self-annihilation. The TD density estimated from

ECCI is 6.72 × 10^8 cm^{-2} for 300 nm un-doped Ge/Si, 2.47 × 10^8 cm^{-2} and 2.45 × 10^8 cm^{-2} for 400 nm and 500 nm un-doped samples, respectively, as shown in Figure 3-19 (d – f). The TD density almost remains the same for 400 nm and 500 nm undoped samples. It is thus interpreted that the TD density reduction effect with thickness is limited to the overall TD density within the grown material as the equilibrium TD spacing is dependent on the balance of the attractive force between adjacent TDs and the line tension related to lattice mismatch as mentioned above. Without external intervention, TD density will be difficult to decrease after reaching this balanced TD spacing. On the contrary, for doped samples, where the layer structure is shown in Figure 3-20 (a – c), although the TD density for 400 nm Ge/Si sample is higher than un-doped 300 nm sample, the TD density reduction trend continues, decreasing from 4.86 × 10^8 cm^{-2} to 1.31 × 10^8 cm^{-2} for the 500 nm sample as shown in Figure 3-20 (d – f), respectively. The comparison of the TD density with thickness for doped and un-doped samples is summarised in Figure 3-21. And therefore, thicker Ge layers up to 1 μm were grown using a heavily-doped LT seed layer to further investigate the TD density reduction effect.

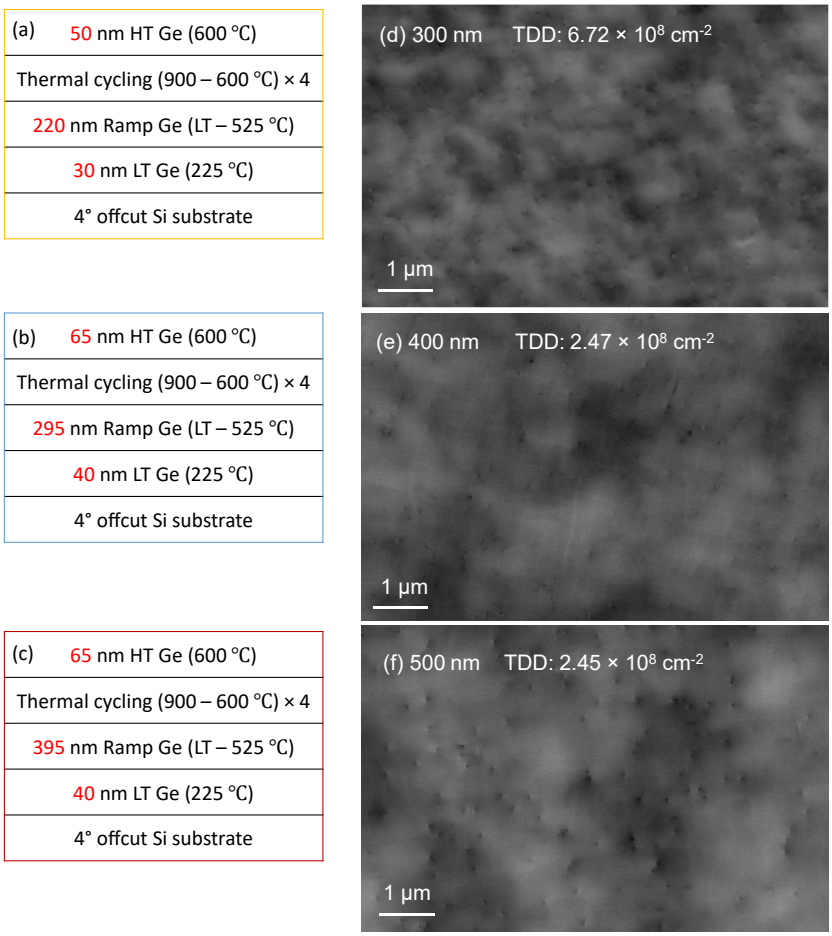

Figure 3-19 Schematic structures and ECCI images of 300 nm, 400 nm, and 500 nm un-doped Ge/Si samples.

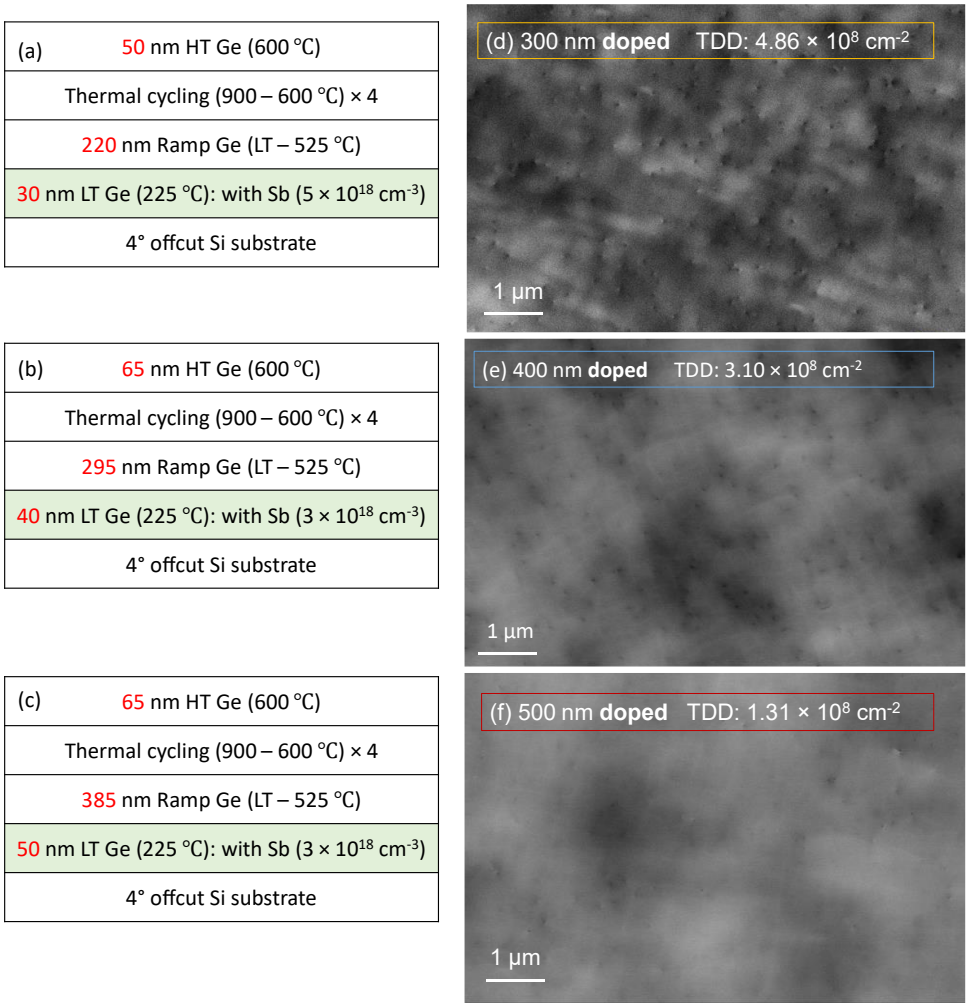

Figure 3-20 Schematic structures and ECCI images of 300 nm, 400 nm, and 500 nm doped Ge/Si samples.

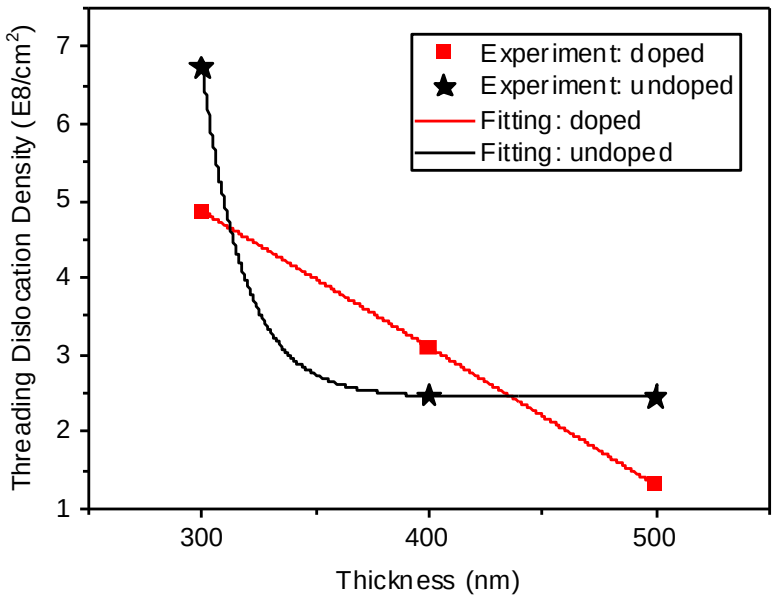

Figure 3-21 Comparison of TD density with a thickness of un-doped and doped samples. The exponential fitting has been applied to both as indicated by solid lines.

The schematic diagram of the grown 1 µm Ge on Si is shown in Figure 3-22. Heavily doped LT layers were first grown, followed by 400 nm temperature ramp layer and 450

nm Ge grown at 525 ˚C. Then 4 repeats of thermal cycling were carried out and finalised with 100 nm HT high crystal quality Ge to smoothen the surface. As expected, the TD density keep decreasing to 3.3 × 10^7 cm^{-2} for 1 μm doped sample, which is a great improvement and the lowest value obtained in our group for 1 μm Ge on Si characterised by ECCI.

A comparison of the ECCI images of the lowest TD density values 300 nm, 400 nm, 500 nm and 1 μm Ge on Si samples are presented in Figure 3-23 (a – d), respectively. A dramatic decrease in TD density can be observed for 1 μm samples compared to 300 nm, 400 nm, and 500 nm samples. Experimental results as well as the exponential fitting line of TD density reduction with increasing thickness can be seen in Figure 3-24. From the initial 500 nanometres, TD density drops rapidly with growth thickness, and this reduction gradually comes to a plateau as the thickness reaches ~ 1 μm.

100 nm HT Ge (600 ℃)
Thermal cycling (900 – 600 ℃) × 4
450 nm MT Ge at 525 ℃
400 nm Ramp Ge (LT – 525 ℃)
50 nm LT Ge (225 ℃): with Sb (3 × 10^{18} cm^{-3})
4° offcut Si substrate

Figure 3-22 Schematic growth structure of 1 μm Ge on Si with heavily-doped seed layer.

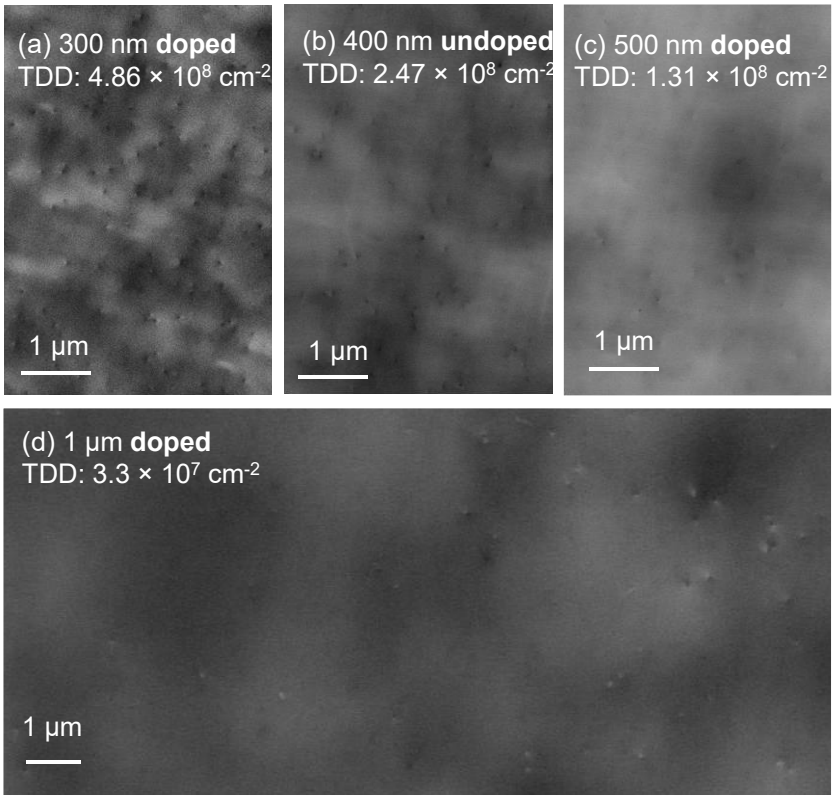

Figure 3-23 ECCI images of the lowest TD density 300 nm, 400 nm, 500 nm and 1 μm Ge samples on Si.

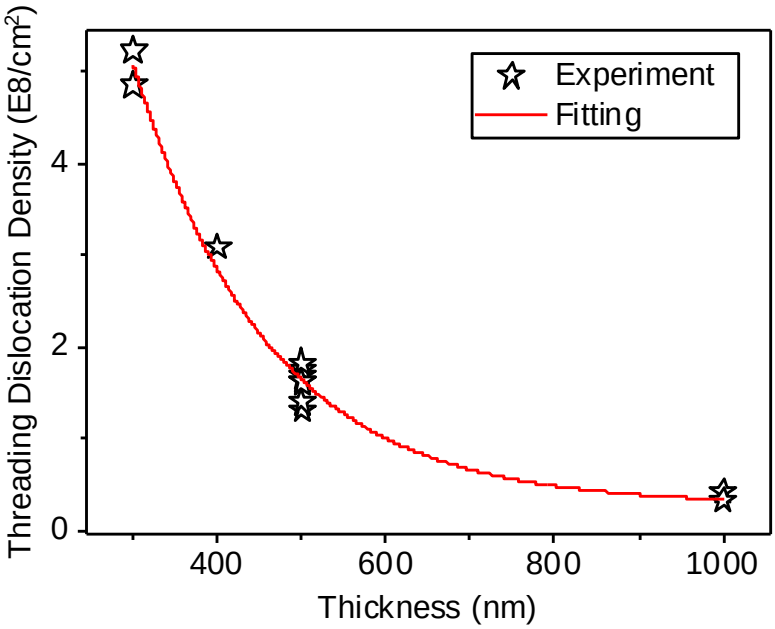

Figure 3-24 A plot of TD density with increasing thickness of all doped-seed-layer Ge/Si samples. The exponential fitting has been applied as indicated by the red solid line.

In addition to the overall thickness, the effect of the LT thickness on TD density has also been examined because, during the investigation of overall thickness, the thickness of LT has also been increased. To find out the origin of TD density reduction, a sample with a thicker LT layer of 60 nm was grown to compare with a 50 nm LT layer sample. The ECCI result presented in Figure 3-25 demonstrates that a thicker LT layer is detrimental to TD density reduction and that the TD density reduction effect should come from the increase in the total thickness rather than the LT thickness.

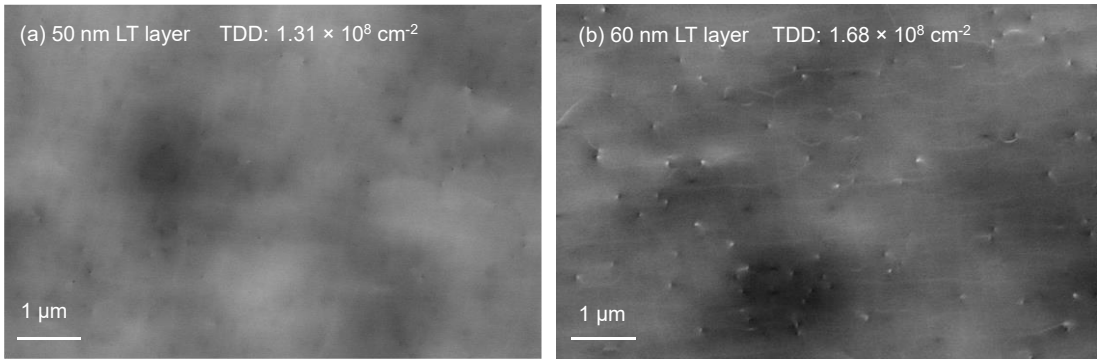

Figure 3-25 ECCI images of 500 nm samples with (a) 50 nm and (b) 60 nm LT layers, respectively.

3.3.4 Effects of growth rate

In this section, different growth rates were used in the LT layer to investigate the effect of growth rate on Ge epilayer crystal quality on Si. 0.54 Å/s and 0.66 Å/s Ge growth rates were examined for two 300 nm samples with Sb doping. The doping profile is the same as described in the previous section. 30 nm LT layer with 5×10^{18} cm^{-3} Sb doping was first deposited on Si substrate, followed by 220 nm temperature-

ramp layer and thermal cycling, and finished by 50 nm HT Ge to improve the surface morphology. In the 3-step growth method adopted by us for samples in series I and II, a low growth rate of the LT layer of around 0.54 Å/s was applied, this is to secure the high crystal quality of the nucleation layer. Generally, a low growth rate should be used for LT growth to allow sufficient time for atoms to migrate on the surface. The ECCI results of the grown samples are shown in Figure 3-26. An increase in TD density was found for the higher growth rate samples, and therefore the growth rates for the rest of the samples were kept at 0.54 Å/s for the LT layer. However, as the effect is not manifest, and keeping the growth at low temperature for an extended time can be detrimental to the material quality (increase the chance of the impingement of impurities), further decreasing the growth rate of the LT layer was not planned deliberately.

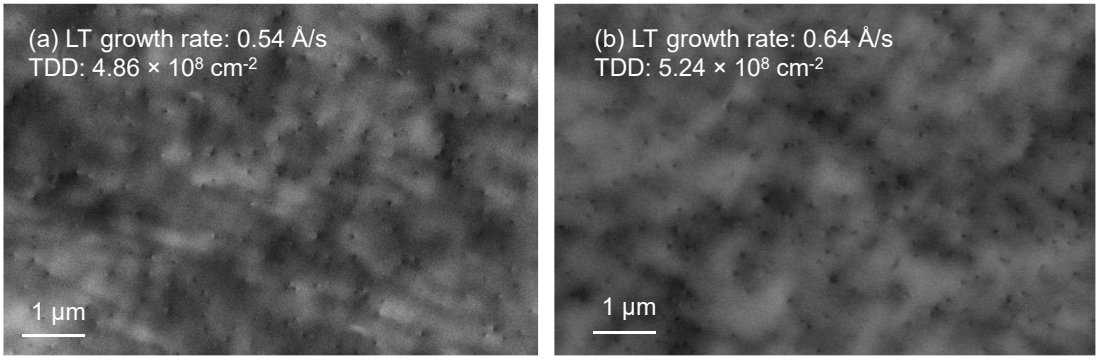

Figure 3-26 ECCI images of samples with LT Ge growth rates of (a) 0.54 Å/s and (b) 0.64 Å/s.

3.3.5 Effects of thermal annealing

Cyclic thermal annealing is a well-studied technique for TD density reduction in Ge/Si epitaxial growth. It is carried out by increasing the substrate temperature to a higher temperature (T_H) e.g., 900 ˚C, just after the temperature-ramp layer, then decreasing to a lower temperature (T_L), such as 600 ˚C, as indicated in the schematic growth structure in Figure 3-27 (a). A repeat of this heating-up and cooling process is called a thermal cycle. The number of thermal cycle is N in Figure 3-17 (a). After thermal cycling, the substrate temperature will be decreased to 600 ˚C for HT Ge growth. The thermally induced strain and energy will boost the motion of TDs and enhance the possibility of self-annihilation. Increasing the number of annealing cycles is shown to facilitate TD reduction for a 1 μm Ge grown on Si, and the temperatures were set as 900 ˚C and 780 ˚C to maximise the TD motion speed [18]. However, most of the results in the literature involve thick (> 1 μm) Ge on Si, from the perspective of reducing buffer thickness while maintaining low TD density, the effects of thermal

annealing on a relatively thin Ge layer on Si should be investigated. In this section, different annealing strategies were studied for 300 nm, 500 nm and 1 μm Ge/Si samples.

1) Two 300 nm samples with 4 repeats of (900 ˚C – 600 ˚C) or (900 ˚C – 400 ˚C) were grown for comparison. The schematic growth structure and AFM images of the two samples are shown in Figure 3-27. It is demonstrated that both surface roughness and TD density can be decreased with higher annealing temperatures, which is a result of high temperature-induced improved crystal quality and enhanced high TD mobility.

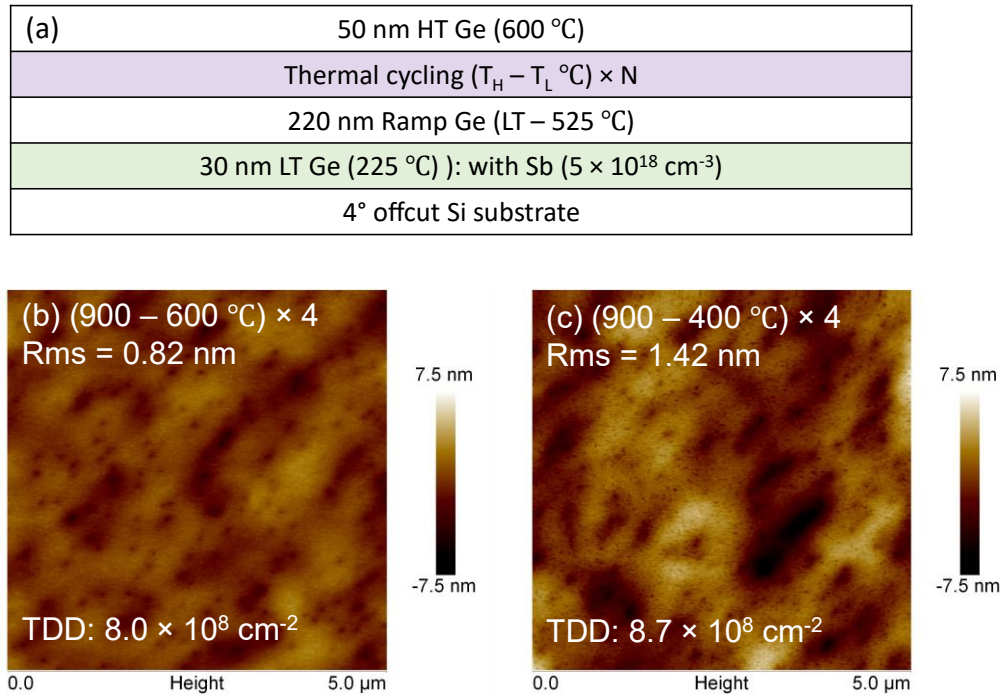

Figure 3-27 (a) The schematic structure of the grown samples, N is the number of thermal cycles. (b) and (c) AFM images of samples with thermal cycling temperatures between 900 ˚C and 600 ˚C and between 900 ˚C and 400 ˚C, respectively.

2) The effect of the number of thermal annealing cycles on TD density was also tested for 500 nm and 1 μm Ge on Si samples. The ECCI results of 500 nm and 1 μm Ge on Si samples with different thermal cycles are shown in Figure 3-28. TD density reduces with thermal cycles increasing from 4 to 12 for a 1 μm sample, which is as expected because more annealing cycles provide more time for TDs to interact and annihilate. However, such behaviour for 500 nm samples is anomalous. For the sample annealed for 8 repeats, the TD density increase to 1.76 × 10^8 cm^{-2} compared to 4 repeats (1.31 × 10^8 cm^{-2}). For the sample annealed for 12 repeats, TD density shows a slight decrease (1.63 × 10^8 cm^{-2}) compare to 8 repeats but is still higher than

4 repeats of thermal cycling. This behaviour can be explained by the possibility that 500 nm thickness is too thin for TDs to bend, attract and finally annihilate with each other so that they arrive at the surface before merging. In contrast, thicker samples allow more sufficient time for TDs to interact. A comparison of thermal cyclic annealing on TD density for 500 nm and 1 μm samples are presented in the bottom right in Figure 3-28.

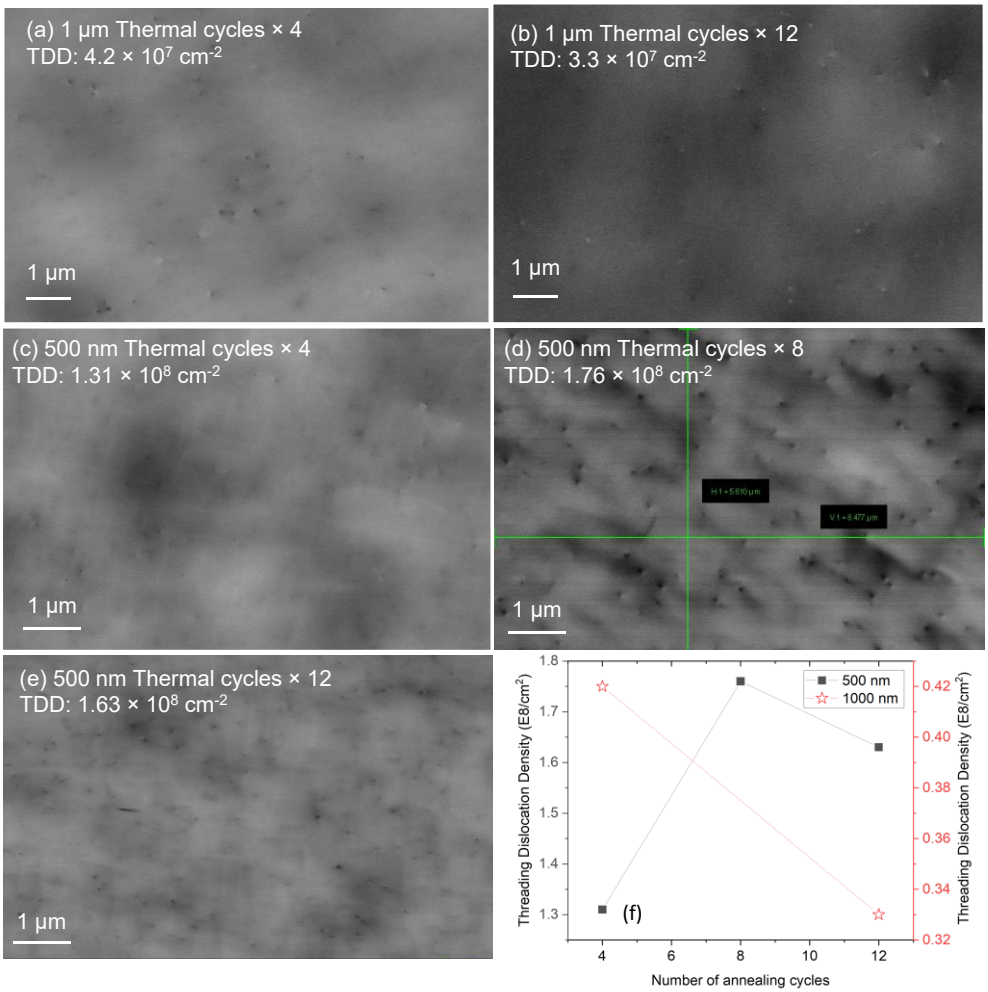

Figure 3-28 ECCI images of 1 μm Ge samples with (a) 4 and (b) 12 thermal annealing cycles, and 500 nm Ge on Si with (c) 4, (d) 8, and (e) 12 thermal annealing cycles. A comparison of thermal cyclic annealing on TD density for 500 nm and 1 μm samples are presented in (f).

3.4 Conclusions

The objective of the work described in this chapter is to reduce the TD density while maintaining a thin buffer thickness of epitaxially grown Ge on Si for the integration of group IV and III-V optoelectronic devices on Si. To achieve this goal, the growth optimisation of the Ge buffer was investigated in the following aspects:

1. The implementation of a heavily doped Ge seed layer. The doping species should be selected to ensure the acceleration of TD motion to reduce TD density and

the dopant is also required to fully passivate the surface so that it can facilitate layer-by-layer growth. Sb is examined to be a superior choice than P or Si both from the perspective of TD density reduction and surface smoothness. As the TD speed increases with doping density in the LT seed layer, a large doping density is desired, and at the same time, the growth temperature is critical to avoid dopant segregation at different doping concentrations and to maintain the effectiveness of the dopants in TD density reduction. Besides, the LT seed layer thickness is not the most important factor in TD density reduction, an increase in this layer thickness is shown to deteriorate the crystal quality of the grown Ge film on Si.

2. The adoption of a temperature-ramped layer. From the perspective of thermodynamics, the TD density reduction favours high growth temperature and longer time between LT and HT layer. Therefore, the temperature ramp should be selected to balance this trade-off. A larger thickness before the thermal cycling is beneficial for TD density reduction.

3. The use of thermal cycling (4/8/12 repeats were applied). The thermal stress generated between the heating-up and cooling-down process will drive the TDs to move in the material and increase the possibility of annihilation. More repeats of thermal cycling are examined to be more efficient for relatively thick samples, i.e., for samples in this chapter, ~ 1000 nm. For thinner samples, TDs may not be fully bent and thus annihilate with adjacent TDs and arrive at the surface before they can be merged.

4. Total thickness of the Ge buffer layer (300/400/500/1000 nm). TD density is reversely related to the thickness of grown Ge on Si. The TD density reduction effect for samples with a heavily doped LT Ge layer will saturate at around 1000 nm.

5. Sb pre-layer technology. 1 ML Sb deposition before LT Ge layer growth was investigated to compare with continuous Sb supply during Ge growth. It is shown that sufficient Sb supply is required to maintain layer-by-layer growth while reducing TD density.

6. Sb and Si co-doping in the low-temperature Ge layer. The co-doping method has also been tested to prove if the dopants can facilitate the incorporation of each other. Sb and Si were applied at the same time in the LT Ge layer from the consideration of strain compensation of large Sb and small Si atoms compared to Ge. However, this method is not promising both from the aspect of surface roughness and TD density. Sb and P could be a better choice for the co-doping method as they are

both n-type dopants, which are expected to boost TD motion, and P atoms are small to release strain introduced by Sb. Our preliminary research on co-doping method using P and Sb have shown come promising results in reducing TD density while maintain a good surface quality.

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Chapter 4.

GeSn for Light Emitting Applications

4.1 Introduction

4.1.1 Challenges

Ge_xSn_{1-x} alloy has received considerable attention in recent years as it overcomes the indirect-bandgap nature of group-IV materials, rendering all-group-IV optoelectronic devices possible. The development of Ge_xSn_{1-x} alloy potentially enables the scalability of the fabrication of group-IV photonic integrated circuits with low cost and can be used for extremely high throughput data centres. The successful indirect-to-direct bandgap transition of Ge_xSn_{1-x} depends mainly on Sn composition and strain engineering. The direct character of the Ge_xSn_{1-x} bandgap grows continuously with increasing Sn composition due to the Sn-induced conduction band mixing effect [1] while a direct-to-indirect bandgap crossover is shown to happen with around 8% Sn [2]. For light emission purposes, higher Sn content is favourable because it increases the directness (the energy separation between Γ and L band minimum) and thus radiative recombination. The optical transition rate *w* is:

$$w = \frac{2\pi}{\hbar}|M|^2 g(\hbar\omega) \tag{4.1}$$

where *M* is the matrix element of the transition operator from an initial state to a final state and the transition operator is determined by the type of interaction that induces

the transition between quantum states; $|M|^2$describes the transition probability, and $g(\hbar\omega)$ represents the density of states expressed as

$$g(\hbar\omega) = g(E) = \frac{1}{2\pi^2}(\frac{2m^*}{\hbar^2})^{\frac{3}{2}}E^{\frac{1}{2}} \quad (4.2)$$

As the conduction band effective mass at L point is much higher, a slight increase in directness strongly affects the radiative emission [3]. Earlier studies have made great efforts to grow crystalline GeSn with high Sn content up to approximately 30 % [4, 5]. However, Sn atoms has lower surface energy than Ge, and the solid solubility of α-Sn in Ge is very low (less than 1 % at room temperature), while Sn segregation can be observed at typical Ge growth temperatures ($\sim 300 - 600$ °C). Crystalline $Ge_{1-x}Sn_x$ growth with $x > 0.005$ is found to show compositional metastability and thus can only be accomplished by non-equilibrium methods such as CVD and MBE [6] at low temperatures. Moreover, as the lattice mismatch between α-Sn (6.46 Å [7]) and Ge is large (14.2 %), the Sn composition required for a direct-bandgap transition of 8% will introduce a lattice mismatch of 1.1 % to Ge. An increase in nominal Sn composition during growth will exacerbate the tendency of Sn segregation, and crystal quality will also degrade as the increasing lattice mismatch induces more misfit dislocations. These defects act as preferential diffusion network for Sn, which enhance the Sn diffusivity by two to three orders of magnitude [8], i.e., pre-relaxed GeSn layers may exhibit thinner critical thickness before Sn segregation happens. Therefore, Sn out-diffusion and accumulated strain in the epilayers can easily lead to an epitaxial breakdown, as observed by a dramatic surface roughness jump, at low thicknesses, e.g., for 10 % Sn GeSn, the epitaxial breakdown thickness is less than 200nm. On the other hand, higher Sn composition imposes more compressive strain to GeSn, which is proven to cancel the Γ-valley shrinkage effect by alloying with Sn [9, 10] and limits Sn incorporation to Ge lattice sites [11], hindering the achievement of a direct bandgap.

4.1.2 MBE Growth of GeSn

Many approaches have been implemented to overcome the aforementioned difficulties to obtain direct bandgap GeSn for light emitting applications based on Si platform. For example, the induced tensile strain helps to increase the direct character of the GeSn bandgap beneficial to light emission without affecting crystal quality significantly. Aided by tensile strain, the amount of Sn required for achieving direct bandgap can be largely reduced, which led to a demonstration of low lasing threshold optically-pumped GeSn laser with only 5.4 % Sn [12]. This compensated Sn

composition brings mediated tendency of Sn segregation, and lower chance of defects generation, which are all benefits for light emission purposes. Besides, fabricating tensor arms [13], and depositing stressors and structuring microdisks [9, 12, 14], all contribute to the tailoring of GeSn bandgap and pushing the performance of the GeSn lasers towards room temperature operation and lower threshold operating power. Maximising the benefit of Sn-incorporation-induced direct-bandgap character while obtaining improved crystal quality is consequently of paramount pursuit of research related to GeSn-based laser devices.

Apart from post-growth fabrication approaches, from the growth aspect substantial endeavours have also been made:

4.1.2.1 Low-temperature growth regime

The material growth temperature of GeSn is critical. Optimised GeSn growth temperature for CVD is around 350 ℃ [10, 13-19] while that for MBE growth, where the typical two-step growth temperatures of Ge are around 300 to 600 ℃, is too high for GeSn. Temperatures below the eutectic temperature of 231.1 ℃ are usually applied for GeSn growth because low temperature-induced point defects are thought to contribute to Sn trapping by lowering the local strain around Sn atoms and enhancing lateral misfit dislocation propagation thus mitigating Sn precipitation [20]. Therefore, a usual MBE growth temperature for growing direct-bandgap GeSn is between 120 – 200 ℃ [4, 19, 21-23]. A growth temperature of 150℃ by MBE is proven to be beneficial for the crystallinity of epitaxial growth of GeSn on Ge (110) and results in no stacking faults nor Sn segregation at 4.8 % Sn [22]. Further reducing the growth temperature to 120 ℃ could successfully contributes to crystalline GeSn with very high Sn content of 25 % [4]. Besides, it is found that the epitaxial breakdown, where the surface roughness increases dramatically while the growth mode changes from two-dimensional to three-dimensional, is closely related to Sn composition and decreases linearly with growth temperature: with Sn composition less than 2 %, epitaxial breakdown is larger than pure Ge; with Sn content between 2 – 6 %, this critical thickness (the maximum thickness before epitaxial breakdown) varies inversely with Sn content in the range of 100 – 1000 nm [21]; and with Sn composition between 5% and 20%, almost linear decreases in critical thickness are found both with increasing Sn composition and growth temperature. Specifically, the critical thickness for GeSn layers grown on Ge-virtual substrate with over 15 % Sn can be as low as

around 10 nm. And for similar Sn composition GeSn layers, a critical thickness of less than 100 nm is found if the growth temperature exceeds 160 ℃ [4].

4.1.2.2 Ge virtual substrates and graded-compositional (Si)GeSn buffer layers

Apart from low-temperature growth, thick GeSn layers demonstrate positive effects of accommodating tetragonal compressive strain by the generation of a point-defect-aided misfit dislocation network at the GeSn/Ge interface [10]. As dislocations are trapped within the interface of the graded GeSn buffer, bulk GeSn shows improved crystal quality. Likewise, applying graded (Si)GeSn buffer layers [24-26], which alleviate the lattice mismatch between GeSn and the substrate (usually Si) or even apply tensile strain to engineer the band structure of GeSn, helps to mitigate Sn segregation and MDs generation. Atomically flat GeSn with Sn content up to 22.3% [11] and PL at wavelengths of 3.0 – 3.5 μm [23] can be achieved using such compositional-graded buffer layers. These solutions are effective because they either accommodate the cumulated strain or release the strain by introduction of defects within the buffer layers. During device fabrication, the structure can be designed to avoid carriers passing through the buffer and the substrate. Additionally, it has been confirmed by *Gibbs* free energy calculation that the limitation of Sn incorporation is mainly due to compressive strain rather than chemical reaction dynamics, and through spontaneous relaxation of GeSn enhanced Sn incorporation and thick layers (up to 1 μm) can be achieved with graded composition layers [10, 11].

4.1.2.3 Thermal treatments

Thermal annealing, as a widely used approach for strain relaxation, is usually unfavoured for GeSn because of the low solubility of Sn in Ge and the metastable nature of GeSn with even moderate Sn composition. After reaching certain critical annealing temperature, Sn segregation phenomenon arises, where Sn clusters deposit at the GeSn surface, at the GeSn/Ge interface or in bulk. It causes dramatically increased surface roughness, reduced lattice parameters and significantly varied surface morphology. Out of consideration for thermal processing during device fabrication, the thermal stability of GeSn has been investigated and reported by a few tens of papers.

The thermal budget for GeSn depends heavily on Sn composition, strain state within epilayer and growth conditions [8, 27]. For the epitaxial growth of GeSn with higher Sn content on Ge/Si, where the lattice mismatch is large, Sn segregation happens at

lower annealing temperature as the strain needs to be released either through the generation of misfit dislocations or Sn out-diffusion [8]. Examples can be given in ref. [28] that used indirect-direct crossover Sn content of around 8% with some extent of strain relaxation within the as-grown layer. Specifically, post-growth annealing of $Ge_{0.915}Sn_{0.085}$ at temperatures ranging from just above growth temperature up to 300 °C makes no difference to the surface morphology; annealing between 300 – 500℃ changes surface roughness and Sn composition, while annealing temperatures higher than 500 – 550 °C causes obvious Sn diffusion out of Ge and accumulation on the epilayer surface. In comparison, annealing of $Ge_{0.9232}Sn_{0.0768}$ only induces changes in surface morphology and Sn content when the annealing temperature reaches 500 °C, and Sn segregation occurs at 700 °C [28].

Moreover, misfit and threading dislocations are proved to accelerate Sn diffusion, thus thick pre-relaxed GeSn layers can sustain higher temperature annealing than pseudomorphically grown layers but with a sharp transition from a high Sn-content alloy to a stable 1% Sn alloy [8] . In fact, after reaching the critical temperature, Sn segregation powered by the lower surface energy of Sn can be seen either suddenly in pre-relaxed GeSn layers or progressively in pseudomorphic GeSn. This behaviour can be explained by the enhanced Sn diffusivity in defects (misfit dislocations and threading dislocations) induced by plastically relaxed GeSn layers. Because the pre-existing dislocation cores act as a preferential diffusion network, Sn precipitation can be observed both on the interface between GeSn and its underneath layer and on the surface for partially relaxed GeSn while for pseudomorphic GeSn layers only surface Sn clusters are observed [8]. An example is given in ref [8] that by varying Sn composition while maintaining the thickness, for partially relaxed GeSn layers the onset of Sn segregation is abrupt and the corresponding annealing temperature decreases steadily with increasing Sn composition, for example, a sudden Sn segregation is observed at 650 °C for $Ge_{0.95}Sn_{0.05}$ while it is around 350 °C for $Ge_{0.88}Sn_{0.12}$. In pseudomorphic growth, the onset of Sn segregation process is gradual and starts at a lower temperature.

Additionally, low-temperature-growth-induced point defects also affect the behaviour of Sn clusters formation, as they aid the lateral propagation of misfit dislocations and help to bind Sn atoms, reducing the strain in GeSn epilayers or local strain around Sn atoms [20]. The positive effects of thermal annealing include improved strain relaxation and crystal quality [10, 27-29]. However, as the thermal

annealing effects are highly sensitive to initial material conditions, i.e., the results can vary significantly with different material parameters, thorough investigations are still demanded for research with different purposes.

4.1.3 Aim

As discussed above the growth of GeSn is challenging and highly dependent on the nominal composition of Sn, defect level and the strain within the GeSn layers. Provided that a higher Sn composition is favourable for light emission purposes, this chapter focuses on the growth optimisation of the buffer layer by a strain compensation method (section 4.2) for the growth of active-region direct-bandgap GeSn and the investigations on thermal budget of GeSn during post-growth processing for device fabrication purposes (section 4.3). An in-situ low temperature annealing approach has also been developed to facilitate high quality composition-graded GeSn buffer layer growth (section 4.4). For the ultimate application of GeSn-based materials for optoelectronic devices, MQW structure has been developed (section 4.5) and characterised by AFM, HRXRD and TEM analyses.

4.2 Strain-Compensation Method

In this section, the effects of a novel strain-compensation method inserting ultra-thin Ge layers within the bulk GeSn are investigated. Initially, a reference sample with a nominal Sn composition of 5 % and a thickness of 200 nm was grown on Ge (001) substrate. The growth structure is shown in the inset of Figure 4-1 (a). The sample has been grown by a solid source Veeco Gen 930 MBE system, the one described in Section 2.1 of this thesis. Before the growth started, the Ge substrate was first baked in the load-lock chamber at 200 °C for 12 hours to remove the water vapour. Then it was degassed in the preparation chamber at 400 °C for one hour. The final preparation step is to deoxidise the substrate and get rid of any remaining oxides. This was achieved by elevating the substrate temperature to 700 °C and kept for 30 minutes. After the deoxidation process and cooling down to around 250 °C, very bright and smooth 2 × 2 RHEED patterns were observed, symbolising a high-quality very flat epitaxial surface. Following that is the deposition of a 12-nm Ge layer at 250 °C to further ensure the surface quality. Then the substrate temperature was cooled to 125 °C and 200 nm $Ge_{0.95}Sn_{0.05}$ was grown at 125 °C.

The composition of the grown GeSn film was examined by XRD. The symmetric Omega-2 Theta scan along (004) lattice plane is demonstrated in Figure 4-1 (a). A

narrow GeSn peak with diffraction patterns is observed left to the Ge substrate, which characterises a Sn composition of 5.4 % with high crystal quality. The diffraction peaks along the GeSn peak are due to the thin film thickness. From these initial results of the reference sample with a nominal Sn composition of 5%, where the lattice mismatch is as low as 0.7 %, a large surface roughness or an epitaxial breakdown is expected for the growth of higher Sn composition GeSn used for the active region of a light-emitting device, i.e., above 8 % Sn content.

The surface morphology was characterised by AFM, and 1 × 1 μm^2 and 5 × 5 μm^2 results are shown in Figure 4-1 (b) and (c), respectively. Uniformly distributed 'dot-like' features can be observed on the surface from the 1 μm^2 image, which reflect the process of strain relaxation through the generation of islands. A root-mean-square roughness (rms) of 1.06 nm is estimated from the 5 × 5 μm^2 AFM image.

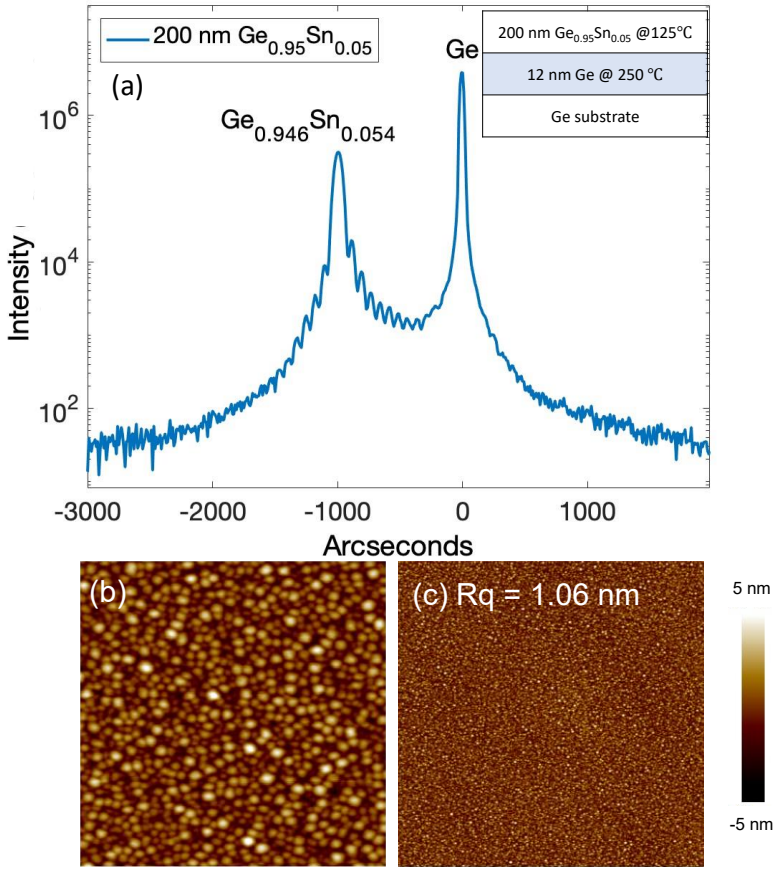

Figure 4-1. (a) The HRRD Omega-2Theta scan along (004) crystal plane and the schematic growth structure of the reference sample with 5 % Sn. The inset shows the growth structure. (b) 1 × 1 μm^2, and (c) 5 × 5 μm^2 AFM images of the reference sample with a nominal Sn composition of 5 %, respectively.

To obtain high-quality GeSn active region with high Sn composition, a strain-compensation method along with different techniques to get smoother surfaces is

applied to the growth of 10 % GeSn layer on Ge substrates. The growth structures are shown in Figure 4-2 (a – c), respectively.

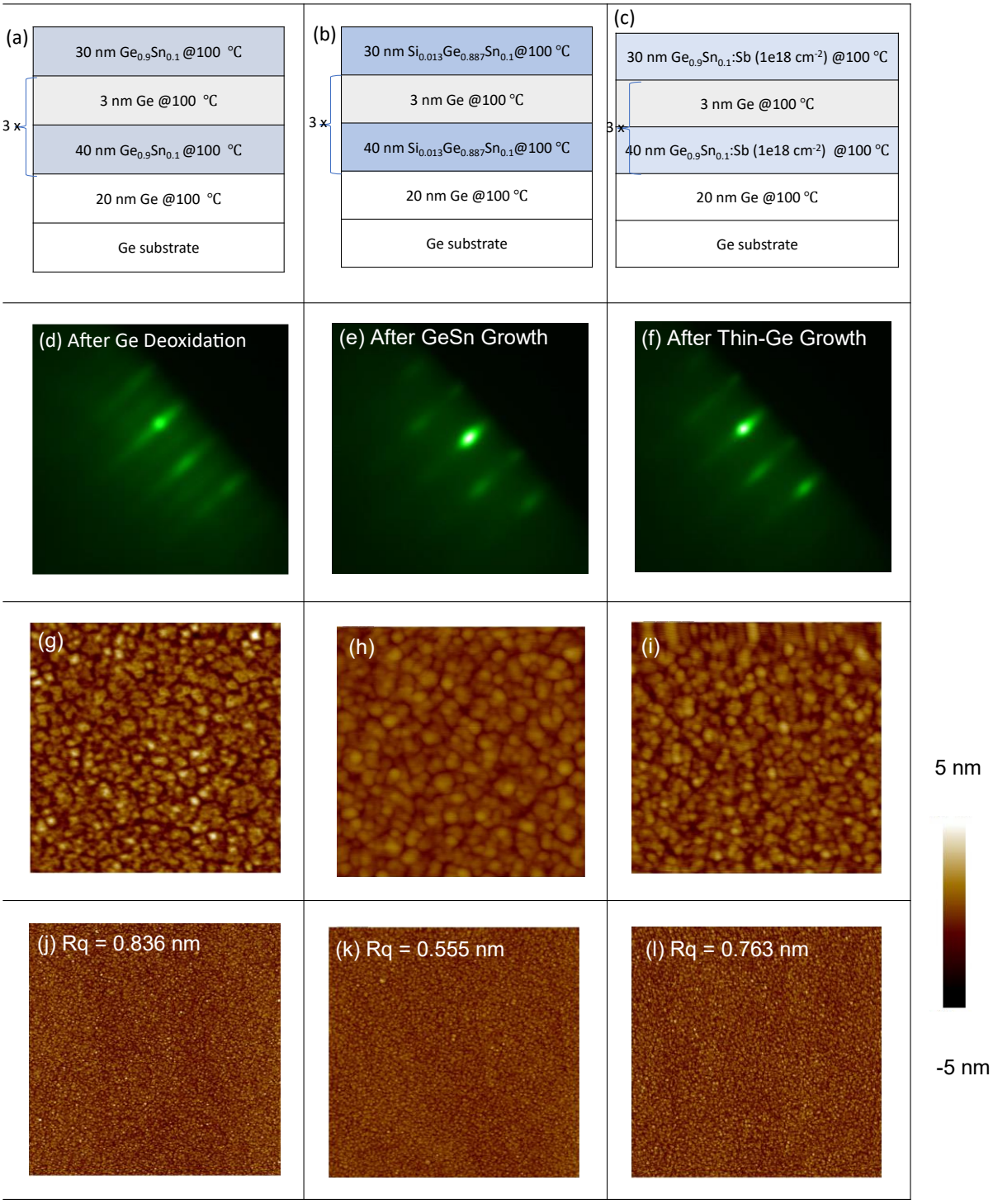

Figure 4-2 (a – c) Schematic growth structures of samples applying the strain-compensation method. Specifically, the layer structure of 150 nm $Ge_{0.9}Sn_{0.1}$ with Ge insertion layers is shown in (a), layer structure of 150 nm $Si_{0.013}Ge_{0.887}Sn_{0.1}$ with Ge insertion layers is shown in (b) and that of 150 nm $Ge_{0.9}Sn_{0.1}$:Sb with Ge insertion layers is presented in (c). (d) 2 × 2 RHEED patterns observed after the deoxidation of Ge substrate; (e) and (f) RHEED patterns after a layer of $Ge_{0.9}Sn_{0.1}$ growth and after a thin 3-nm Ge insertion layer growth, respectively. (g – i) 1 × 1 μm^2 AFM images of the three samples; (j – l) 5 × 5 μm^2 AFM images of the samples.

The strain-compensation method is expected to accommodate the heteroepitaxial strain induced by Sn incorporation by interrupting the strain build-up with the growth of an ultra-thin Ge layer during the GeSn growth. Therefore, the initial growth was designed to be that after each 40 nm $Ge_{0.9}Sn_{0.1}$, a 3-nm Ge layer was inserted, and the total thickness of GeSn is 150 nm, as shown in Figure 4-2(a). During the growth, the surface morphology was investigated by RHEED, where an immediate surface morphology change could be observed upon the growth of the Ge insertion layer. The RHEED patterns just after the deoxidation process are bright and streaky 2 × 2 constructions, which are presented in Figure 4-2(d), demonstrating a smooth two-dimensional morphology. The RHEED observations before and after the Ge insertion layer growth are shown in Figure 4-2 (e) and (f), respectively. Just after a few nanometres of $Ge_{0.9}Sn_{0.1}$ growth, the smooth and streaky fundamental patterns will become intermittent and spotty. At the same time, the diffraction patterns disappeared after a few seconds, leaving the 1 × 1 patterns which demonstrate the roughening of the surface. In stark contrast, immediately after the start of the Ge insertion layer growth, the streaky patterns were resumed, although the diffraction patterns are not recovered, as shown in Figure 4-2(f). This smoothening mechanism was observed to be effective during the whole 150 nm $Ge_{0.9}Sn_{0.1}$ growth. Despite the extent of surface smoothening effects degraded with increasing thickness. The surface morphology of the sample with Ge insertion layer is characterised by 1 × 1 μm^2 and 5 × 5 μm^2 AFM images, as shown in Figure 4-2(g) and (j), respectively. A rms of 0.836 nm is obtained from the 5 × 5 μm^2 AFM image, which is even lower than the $Ge_{0.95}Sn_{0.05}$ reference sample.

In order to further improve the growth technique, SiGeSn and surfactant-mediated growth method are combined with the strain-compensation technique. From the perspective of epitaxial growth, SiGeSn can act as a buffer layer between GeSn and Si or Ge because of its intermediate lattice constant, which is controllable with Si and Sn composition. Moreover, from the device aspect, SiGeSn can be a superior barrier material than bare Ge, as the bandgap is also manipulatable by Si and Sn composition and is potentially capable of providing better electron confinement. Zhou *et al* have theoretically and experimentally proved the effectiveness of using SiGeSn instead of Ge as the cap layer in realising better laser performance [30]. Electrically injected GeSn laser has been achieved based on SiGeSn buffer layer and barrier layers [31]. In this study, $Si_{0.013}Ge_{0.887}Sn_{0.1}$ is used in combination with the strain-compensation

method because the lattice constant is almost identical to $Ge_{0.9}Sn_{0.1}$, which are 5.7352 Å and 5.7382 Å, respectively. The growth structure is shown in Figure 4-2(b). The smaller Si atoms are expected to accommodate the local strain brought by large Sn atoms. The 1 × 1 μm^2 and 5 × 5 μm^2 AFM images are presented in Figure 4-2(h) and (k), respectively. The surface of the $Si_{0.013}Ge_{0.887}Sn_{0.1}$ with Ge insertion layers is smoother than that of the $Ge_{0.9}Sn_{0.1}$ with Ge insertion layers, which can be confirmed from the rms roughness of the 25 μm^2 AFM images. The rms is only 0.555 nm for 150 nm $Ge_{0.9}Sn_{0.1}$ grown on Ge substrate.

Then, the effect of surfactant is also examined for GeSn growth. This was inspired by the Ge on Si growth, that the Sb surfactant always tends to float on the surface, passivating the step edges and the flat surfaces and facilitating the two-dimensional growth. In addition, the incorporation of Sn in the epitaxial GeSn film can be enhanced by surfactant Sb, which has been reported recently by different research groups [32, 33]. Therefore, Sb doping of a density of 1 × 10^{18} cm^{-3} was applied to the $Ge_{0.9}Sn_{0.1}$ growth with Ge insertion layers. The growth structure is shown in Figure 4-2(c). The surface morphology is revealed by 1 × 1 μm^2 and 5 × 5 μm^2 AFM images in Figure 4-2(i) and (l), respectively. A rms roughness of 0.763 nm is obtained from the 25 μm^2 AFM image, which is slightly improved compared with the sample without the surfactant.

HRXRD symmetric omega-2theta scans around (004) lattice plane were also applied to probe the growth-direction lattice parameters. As shown in Figure 4-3 (a – c), the normalised intensities correspond to $Ge_{0.9}Sn_{0.1}$, $Si_{0.013}Ge_{0.887}Sn_{0.1}$, and $Ge_{0.9}Sn_{0.1}$:Sb, respectively, and Figure 3 (d) is a summary plot for intuitive comparison. Due to the thin Ge insertion layer, periodic diffraction satellite peaks accompanying the GeSn peak, which is the highest peak left to the Ge peak, can be observed for all three samples, which is also a reflection of the high crystallinity. The lattice parameters calculated from the GeSn peak positions are 5.74 Å, 5.73 Å, 5.74 Å, respectively for Figure 4-3 (a – c), which well match the nominal values for $Ge_{0.9}Sn_{0.1}$. In Figure 4-3 (d), the peak positions of Ge substrate have been normalised to 0 for the comparison of different samples. As expected, for the $Si_{0.013}Ge_{0.887}Sn_{0.1}$ sample, a clear shift towards zero is observed, whereas for the sample with Sb, it presents an obvious shift to the left, when comparing with the peak position of $Ge_{0.9}Sn_{0.1}$. This is because the incorporation of Si will result in a smaller lattice constant while the presence of Sb

increases the lattice size. The peak intensities of GeSn and Ge are almost identical for the three samples, indicating no distinguishable crystal quality degradation induced by the third atoms.

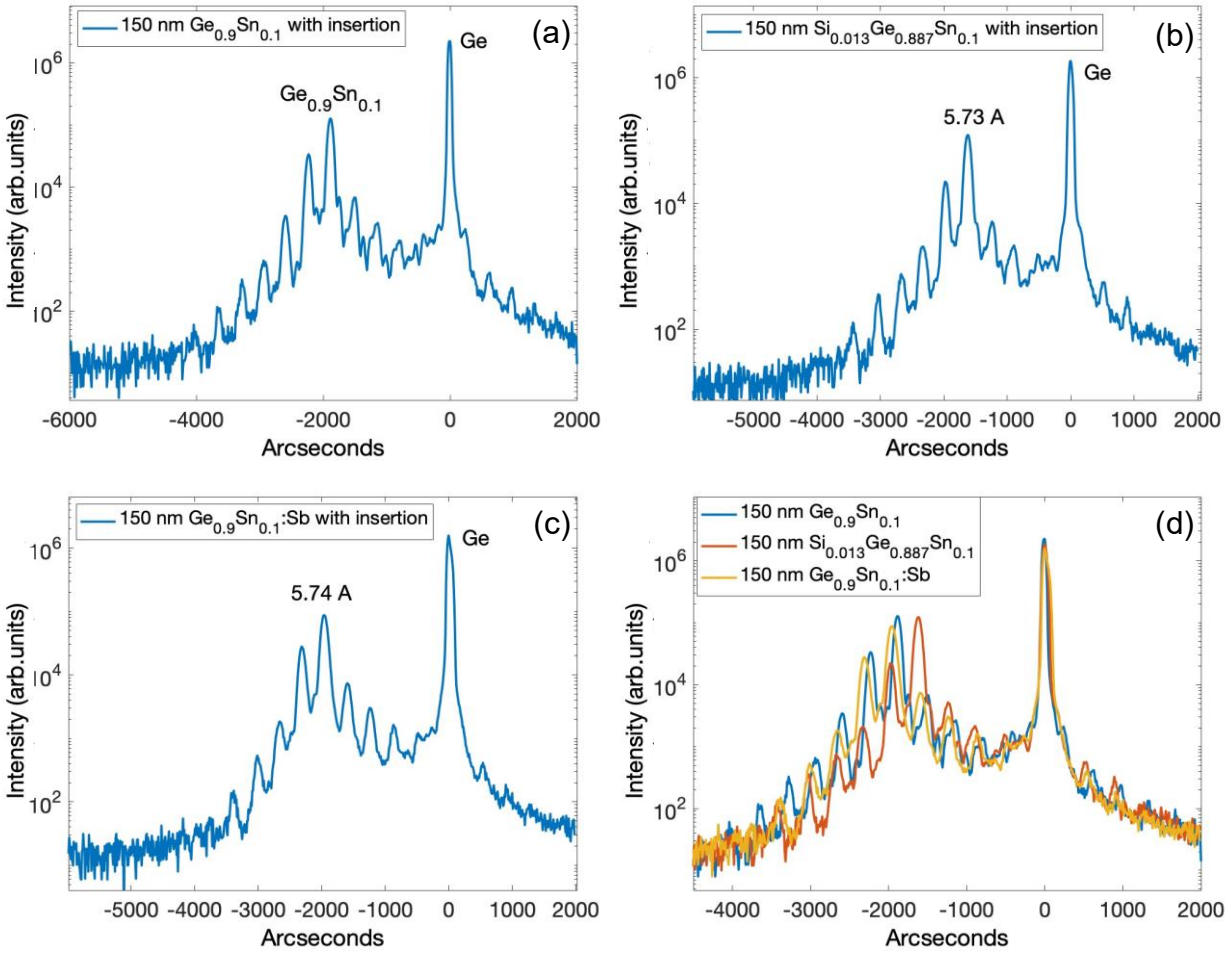

Figure 4-3 (a – c) HRXRD symmetric omega-2theta scans around (004) lattice plane for samples of $Ge_{0.9}Sn_{0.1}$, $Si_{0.013}Ge_{0.887}Sn_{0.1}$ and $Ge_{0.9}Sn_{0.1}$:Sb with Ge insertion layers, respectively; (d) A comparison of three samples.

In summary, in this section, a strain-compensation method applying thin Ge layers to prohibit strain build-up has been implemented in combination with SiGeSn and surfactant to facilitate the growth of high Sn composition GeSn for light emission applications. It has been found that this method is effective for the direct growth of $Ge_{0.9}Sn_{0.1}$ on Ge up to a thickness of 150 nm. The effectiveness of this method will gradually degrade with increasing deposition thickness. With the help of a little amount of Si incorporation or surfactant facilitation, the obtained rms can be reduced to 0.56 nm and 0.76 nm, respectively, which are very low for 150 nm $Ge_{0.9}Sn_{0.1}$ grown on Ge substrates. ECCI measurements were attempted for these three samples, however, the highly contrasted pits (usually as an indicator for TDs) were not observed.

4.3 Ex-Situ Post-Growth Annealing Studies

Inspired by the benefits of thermal annealing in strain relaxation and crystal quality improvement, in this section, the investigations on ex-situ thermal annealing of 500 nm GeSn grown on 250 nm Ge based on Si (100) substrate by MBE designed to serve as a buffer for subsequent GeSn growth for optoelectronic devices are presented. Indeed, the subsequently grown GeSn layer is expected to contain large Sn composition with little compressive strain, which is highly beneficial for the realisation of a high directness of the bandgap. As the built-in compressive strain is an important parameter affecting GeSn crystal structure, this research examines the strain state of the GeSn epilayer after thermal annealing by various methods. It aims at finding appropriate annealing conditions to ensure maximum extent of strain relaxation while avoiding Sn segregation. The annealed GeSn layers can potentially provide a highly relaxed, lattice-matched buffer to the active layer. Moreover, a much thinner platform compared with a thick Ge or compositional-graded (Si)GeSn buffer with several microns thickness can be secured.

4.3.1 Material Growth and Rapid Post-Growth Annealing

As the goal is to grow a high-crystal-quality relaxed buffer for GeSn optoelectronic devices, pre-relaxed GeSn layers were chosen to provide better thermal stability and a Sn composition around GeSn bandgap indirect-to-direct crossover was selected to ensure better lattice match. 500 nm GeSn with a nominal Sn content of 8% was grown on 250 nm Ge buffer on Si (100) substrate by Veeco Gen 930 solid source MBE at a temperature window of 130-150 °C. 130 °C was the target growth temperature, however, due to the heating from the source effusion cells, there was an unintended temperature fluctuation between 130 and 150 °C during the growth. The Ge buffer growth was performed following our previously optimised growth conditions [34]. A 5 nm Ge cap was deposited at the top of GeSn layer to prevent Sn segregation on the surface. After the growth, the samples were cleaved into 8 identical pieces and annealed at temperatures between 300 and 600 °C at step intervals of 50 °C for 5 minutes each in nitrogen ambient conditions in a Solaris 150 Rapid Thermal Processor.

4.3.2 Surface Morphology

10 ×10 μm^2 AFM images of 500 nm GeSn/Ge/Si as-grown and after annealing at different temperatures (300 to 600 ℃) are shown in Figure 4-4 (a – h), respectively. The surface of the as-grown GeSn sample undulates with randomly oriented hills and

pits decorated with numerous tiny white spots, as can be seen in Figure 4-4 (a). It has a rms roughness of 2.60 nm, which is smooth for a 500 nm thick GeSn layer with nominal 8% Sn as the surface roughness grows with GeSn layer thickness and Sn composition [10, 35, 36].

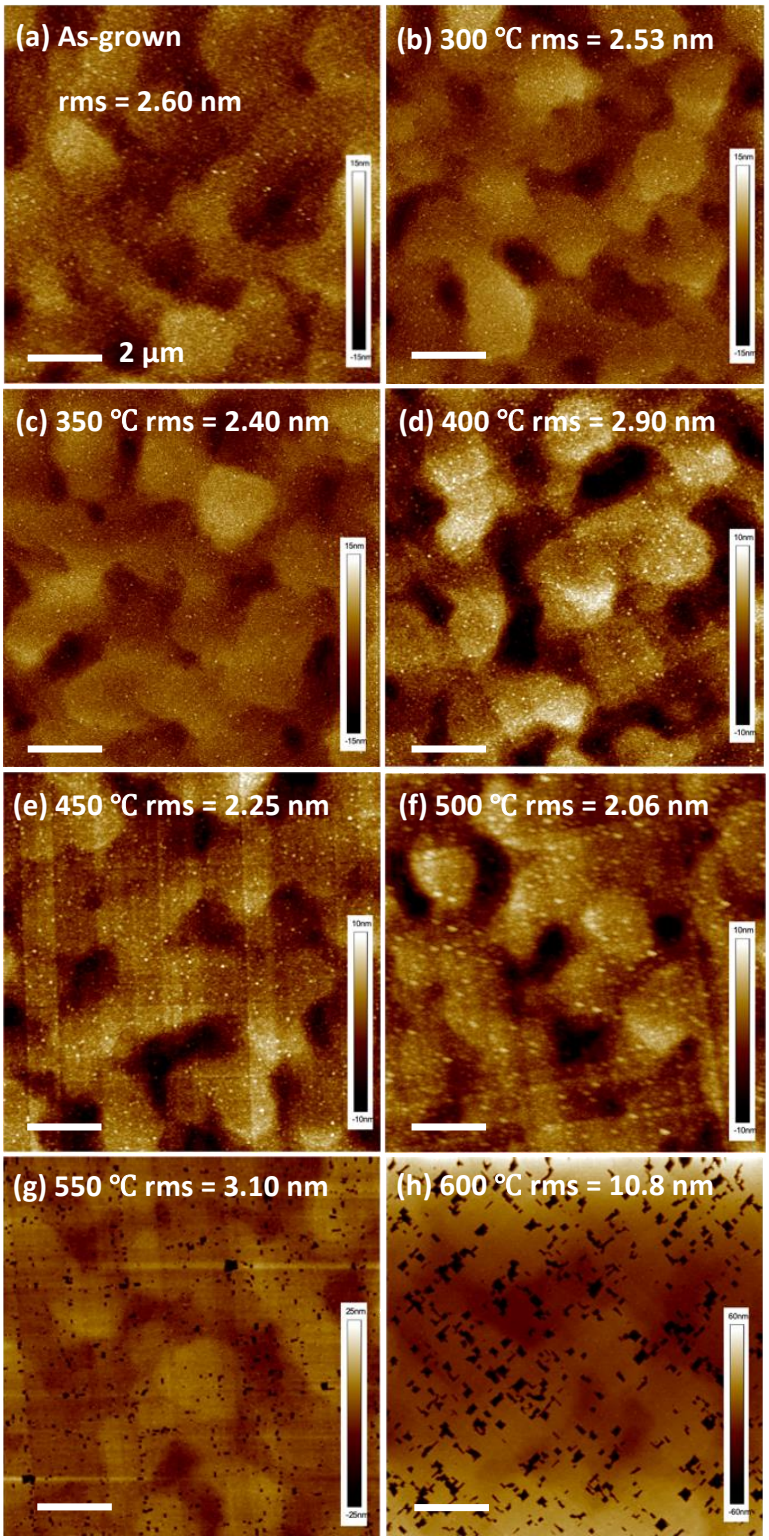

Figure 4-4. 10 × 10 µm² AFM images of the surface of (a) as-grown GeSn with nominal 8% Sn and (b-h) after thermal treatment at various temperatures between 300-600 °C. Root-mean-square roughness is shown in each image. Scale bars are the same of 2 µm as labelled in (a).

The tiny white dots were considered to be two possibilities. One is Sn precipitates because of the metastability of GeSn leading to phase separation of the Sn. There are two different phases of solid Sn precipitates: semiconductor phase α-Sn with diamond structure and metallic phase β-Sn with body-centred tetragonal unit cell [37]. The eutectic point of the GeSn alloy is 232 °C and the allotropic phase transition between α- and β-Sn is 13.5 °C. α-Sn is stable below the allotropic phase transition temperature while β-Sn phase is stable above this point [30]. Except for temperature, the formation and stability of the two phases of Sn crystallites depend heavily on pressure and interface effects [37]. For example, the temperature for the transformation from α-Sn to β-Sn can be elevated by the tensile strain in the precipitates to as high as around 200 °C in $Si_{0.95}Sn_{0.05}$ [38]. In our experiment, the growth temperature is low enough to suppress the Sn segregation, however, during the kinetic epitaxial growth process, Sn atoms may suffer from large compressive strain due to the significantly larger crystal lattice. Then the compressive strain can make the α-Sn to β-Sn transformation happen at decreased temperature, the denser β-Sn phase thus forms clusters and diffuse to the surface, so we can even observe the white dots in the as-grown sample.

Another possibility is Sn-induced surface roughening. There are two primary mechanisms controlling the surface morphology of epitaxial growth: kinetic and strain-induced roughening [21]. Kinetic roughening mainly dominant in low temperature growth as it is due to the lack of energy to cross step edges so that form multiple-level-growth, while strain-induced roughening predominantly affects high temperature strained heteroepitaxy. As we are in low temperature growth regime, kinetic roughening dominates. The nominal Sn composition in our experiment is high, which increases the total strain energy. Relaxation through stain-induced roughening becomes thermodynamically favourable when the energy cost related to increased surface area is overcome by the decrease in film strain energy due to dilatation in interplanar spacings near island peaks [21], i.e. strain enhances the overall roughening rate. In addition, the thermal activation required for strain-induced roughening can also be lowered by the local surface chemical potential gradients provided by the kinetic roughening [21]. An example is that we found similar AFM images of 274 nm $Ge_{0.957}Sn_{0.043}$ and 165 nm $Ge_{0.939}Sn_{0.061}$ grown on Ge in reference [21]. Except for the slightly improved image contrast at the hills and pits, almost no changes were observed in surface morphology for the sample annealed at 300 °C (see Figure 4-4 (b)) compared with the as-grown surface. After annealing at 350 °C,

some indistinct crosshatch patterns (periodic surface undulations) began to show up, as seen in the bottom left corner of Figure 4-4 (c). For samples annealed between 400 °C and 500 °C, obvious crosshatch patterns appeared on the surface (see Figure 4-4 (d – f)). The spacing between adjacent crosshatch lines is around 0.5 – 1 μm. Cross-hatch pattern occurs when the misfit dislocation spacing is smaller than the epilayer thickness, and it has a much larger spacing than the misfit dislocation spacing [39]. In other words, the misfit dislocation spacing in the GeSn epilayer annealed at 350 – 500 °C should be 1 – 2 orders of magnitude smaller than 0.5 – 1 μm. Cross-hatch patterns are reported to result from the nucleation and gliding of the misfit dislocations in the {111} planes [40, 41] and are confirmed to be related to inhomogeneous strain field within the epilayer [39]. In this case, it indicates that by thermal annealing the strain can be relieved through the nucleation and gliding of the misfit dislocations, i.e., preventing the increase in threading dislocations penetrating to and degrading the crystal quality of the active GeSn layer [34]. Except for these crosshatch patterns, the surface morphology remained stable at this annealing temperature window, i.e., 300 – 500 °C. Reduced roughness was observed in the samples annealed at 300 – 350 °C and 450 – 500 °C. However, the surface morphology varied significantly after annealing at 550 °C and above, as can be seen in Figure 4-4 (g – h). 'Broken' surfaces were observed, where the perpendicular crosshatch patterns remained in Figure 4-4 (g), only lined-patterns stood in Figure 4-4 (h), and the GeSn surface character (as seen in the as-grown AFM image Figure 4-4 (a)) faded in both images with numerous black spots on the surface after annealed at 550 °C and enlarged at 600 °C. The corresponding sharp increase in surface roughness for annealing temperature of 550 and 600 °C can be seen in Figure 4-4 (g) and (h). Meanwhile, milky spots on the surface can be seen with the naked eye for these two samples, with a higher density for the sample annealed at 600 °C. These investigations are in good agreement with others' works on GeSn annealing with similar Sn content but with thinner GeSn thickness (between 160 – 200 nm) , where the significant changes in surface morphology were confirmed to be a result of Sn out-diffusion and precipitation on the surface [28, 42]. The black spots in AFM images were believed to be the holes created by Sn out-diffusion. To understand the dynamics of the changing strain state corresponding to the occurrence and disappearance of crosshatch patterns and the broken surfaces, HRXRD (004) symmetric scans and RSMs were applied.

4.3.3 Strain State

First, HRXRD symmetric omega-2theta scans around (004) lattice plane were applied to probe the growth-direction lattice change. Three distinct peaks corresponding to GeSn, Ge and Si are labelled, as can be seen in Figure 4-5 (a). The peak amplitude was normalised to show the effect of thermal annealing, and all the spectra were referenced to Si peak. Sharper and stronger diffraction peaks of GeSn than Ge can be clearly observed, indicating higher crystallinity and larger thickness of the GeSn film. This observation is in contrast with studies on GeSn thermal annealing where thick Ge buffer layers, i.e., few microns are applied to ensure full relaxation of Ge [8, 27] . The obvious asymmetric shape of the Ge peak shown in all samples is believed to be a result of Ge-Si interdiffusion. Peak amplitude, peak integral intensity and GeSn lattice constant of each sample annealed at different temperatures were also extracted and presented in Figure 4-5 (b). The GeSn peak position of the sample annealed at 300 °C did not shift compared with the as-grown sample, but the signal intensity significantly increased (by 58%, calculated from both peak amplitude and peak integral intensity), indicating structural stability and improved crystallinity at this annealing temperature. For samples annealed at 350-450 °C the GeSn peaks shift continuously to larger values, corresponding to smaller growth-direction lattice parameters. The peak amplitude and peak integral intensity decrease with higher annealing temperature at 350 and 400 °C, especially at 400 °C, indicating slightly degraded crystal quality. However, after the annealing temperature reaches 450 °C, the peak amplitude and peak integral intensity slowly recovered to levels half of the as-grown sample. The signal of the sample annealed at 600 °C was completely lost presumably because metallic β-Sn clusters on the surface absorbed the x-rays [37, 38, 43, 44]. Although the transition between α-Sn and β-Sn may also be affected by pressure and interface effects so that α-Sn can persist up to e.g., 200 °C in $Si_{0.95}Sn_{0.05}$ [37], in our experiment, the 600 °C annealing is too high for α-Sn precipitates to sustain.

A clear trend of the decreased lattice parameters in GeSn layers with raising temperature is observed. At first, we considered it to be the effect of Sn segregation during thermal treatment. However, that does not explain the GeSn lattice constant decrease when the annealing temperatures are below 550 °C, especially the sharp drop between 350 and 400 °C. As indicated by the AFM images, those significant changes to the crystal lattice only happened at 550-600 °C annealing temperatures. Moreover, milky spots seen on the wafer surface were observed after high

temperature annealing at 550 and 600 °C. To gain further knowledge of the annealed samples in terms of Sn composition, strain state and crystalline quality, RSMs around (224) lattice plane were adopted as they provide more information.

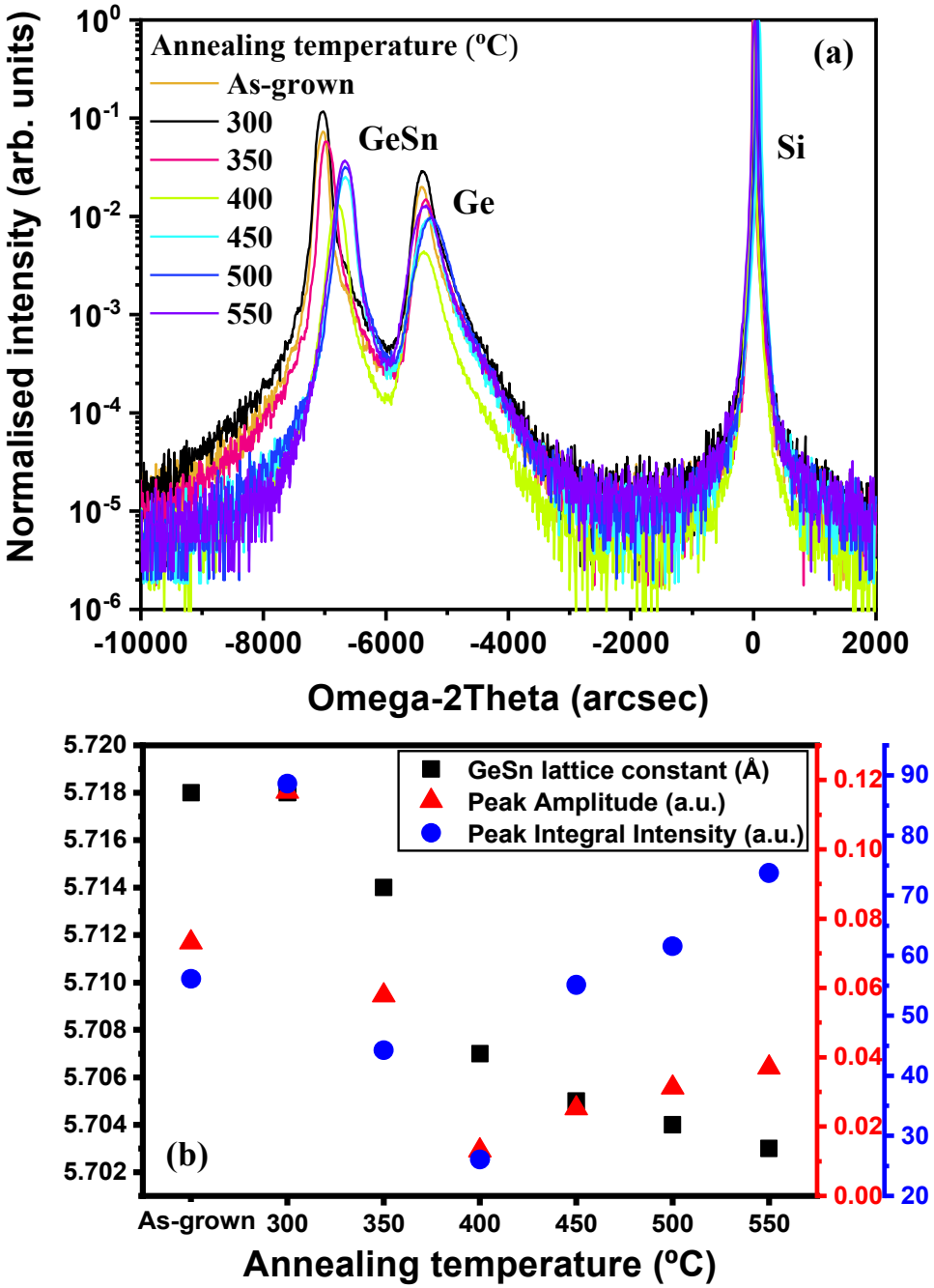

Figure 4-5 (a) XRD omega-2theta scans of GeSn as-grown and annealed at various temperatures. (b) Growth-direction GeSn lattice constant (black squares), peak amplitude (red triangles) and peak integral intensity (blue dots) change with annealing temperature, extracted from (a).

RSMs can supply strain state information about the epilayers intuitively through the angle between epilayer diffraction peak and pseudomorphic-growth line (or strain-relaxed line). It can also be translated quantitatively to the in-plane and growth

direction lattice parameters. The RSM around asymmetric (224) reflection of the as-grown GeSn sample is shown in Figure 4-6. Three peaks corresponding to Si, Ge and GeSn have been labelled at the right-hand side of each peak. One vertical dotted pseudomorphic-growth line indicating a fully strained crystal lattice, where the epilayer has the same lattice parameter with the Ge layer underneath, and one diagonal solid strain-relaxed line suggesting a fully relaxed lattice with cubic structure are marked. From Figure 4-6 it can be intuitively observed that the GeSn epilayer in the as-grown sample is relaxed to some extend as the GeSn peak deviates from the pseudomorphic growth line. This is due to the 500 nm GeSn layer thickness has far-exceeded the critical thickness for the onset of strain relaxation.

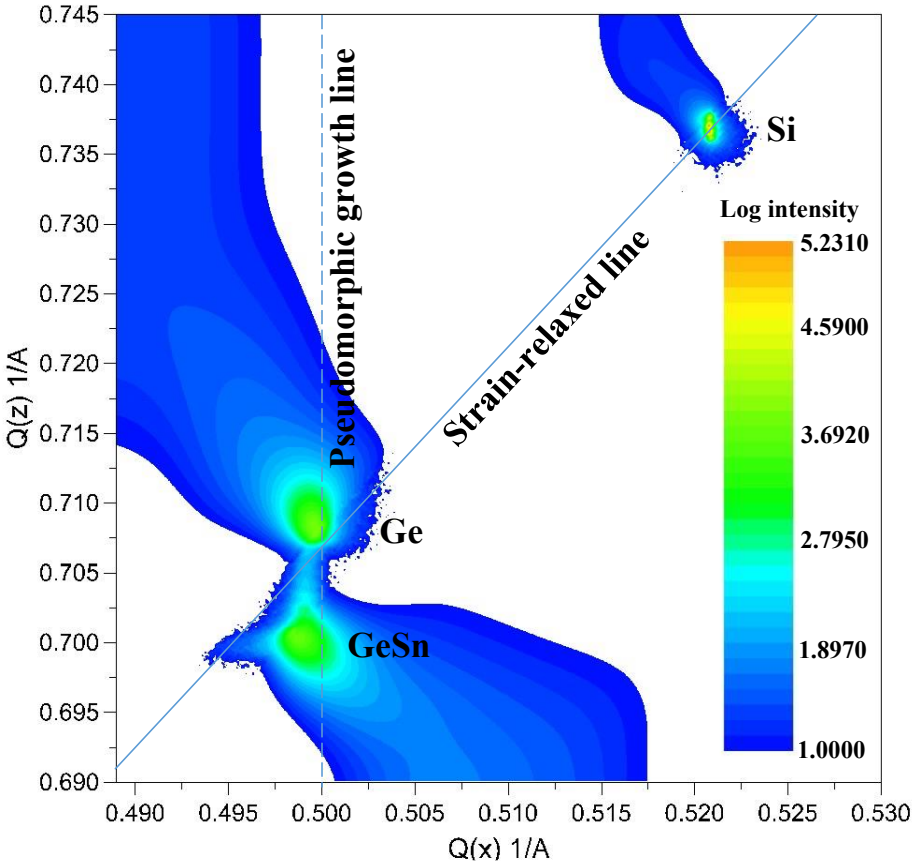

Figure 4-6. X-ray diffraction reciprocal space map around (224) lattice plane of as-grown GeSn. Form this map, in-plane (a_i) and growth direction (a_g) lattice constants can be calculated by $a_i = 2\sqrt{2}/Q(x)$, $a_g = 4/Q(z)$. Q(x) and Q(z) correlate to Omega tilt and d spacing of the peak, respectively.

The impacts of different thermal annealing temperatures between 300-600 °C to GeSn layer are presented in the RSM measurements of Figure 4-7 (a – g). All the peak intensities of the RSMs in Figure 4-7 (a – g) were set to the same range (log intensity from 1.0000 to 6.0000) so that a comparison of the peak profile could be presented. The peak profile can be defined as the coloured area of each peak. After

thermal annealing at 300 °C the GeSn peak is close to the pseudomorphic-growth line, indicating large compressive strain within the GeSn epilayer, as shown in Figure 4-7 (a). In Figure 4-7 (b) when the annealing temperature was increased to 350 °C, the GeSn peak started to move towards the strain-relaxed line. Improved crystallinity of GeSn was also observed as indicated by the shrunken peak profile. The peak positions of GeSn keep moving steadily to the strain-relaxed line after annealing at 400 and 450 °C, as shown in Figure 4-7 (c) and (d), respectively. In summary, an increase of strain relaxation with rising annealing temperature between 350-450 °C was observed, and nearly full degree of relaxation was achieved after the annealing temperature reaches 450 °C. GeSn peaks sit around the strain-relaxed line for samples annealed at 450-600 °C (see Figure 4-7 (d – g). However, another clear observation is that the peak profiles of Ge and GeSn are significantly enlarged upon annealing temperature hitting 400 °C. These enlarged profiles are accompanied by the strain relaxation processes as the GeSn peaks shift towards the strain-relaxed line, proving the onset of strain relaxation induced by thermal annealing and are also consistent with the observations in AFM crosshatch results. This phenomenon is recognised as a mosaic spread process where the peak profiles become enlarged because of the slight misorientations of the crystal lattice. The in-plane (a_i) and growth-direction (a_g) lattice parameters of Ge and GeSn were extracted from RSMs, and the bulk lattice constant (a_b) of GeSn was calculated considering the Poisson ratio (μ = 0.28, the Poisson ratio of Ge) by [42]:

$$a_b = \frac{a_g + 2a_i\mu}{1+2\mu} \qquad \text{Equation 4.3}$$

The bulk GeSn lattice constants and corresponding Sn composition calculated by applying Vegard's law are shown in Figure 4-7 (h). In contrast with the lattice constants decreasing with rising annealing temperature obtained from symmetric (004) scans, there is an upward trend of GeSn bulk lattice constants calculated from RSMs, except at 300 °C and 600 °C. The shift of GeSn lattice constant towards Ge at 300 °C annealing is counter-intuitive, and the increase of GeSn lattice constant at 550 °C is also unexpected as Sn out-diffusion has happened at this temperature as inferred from the AFM images.

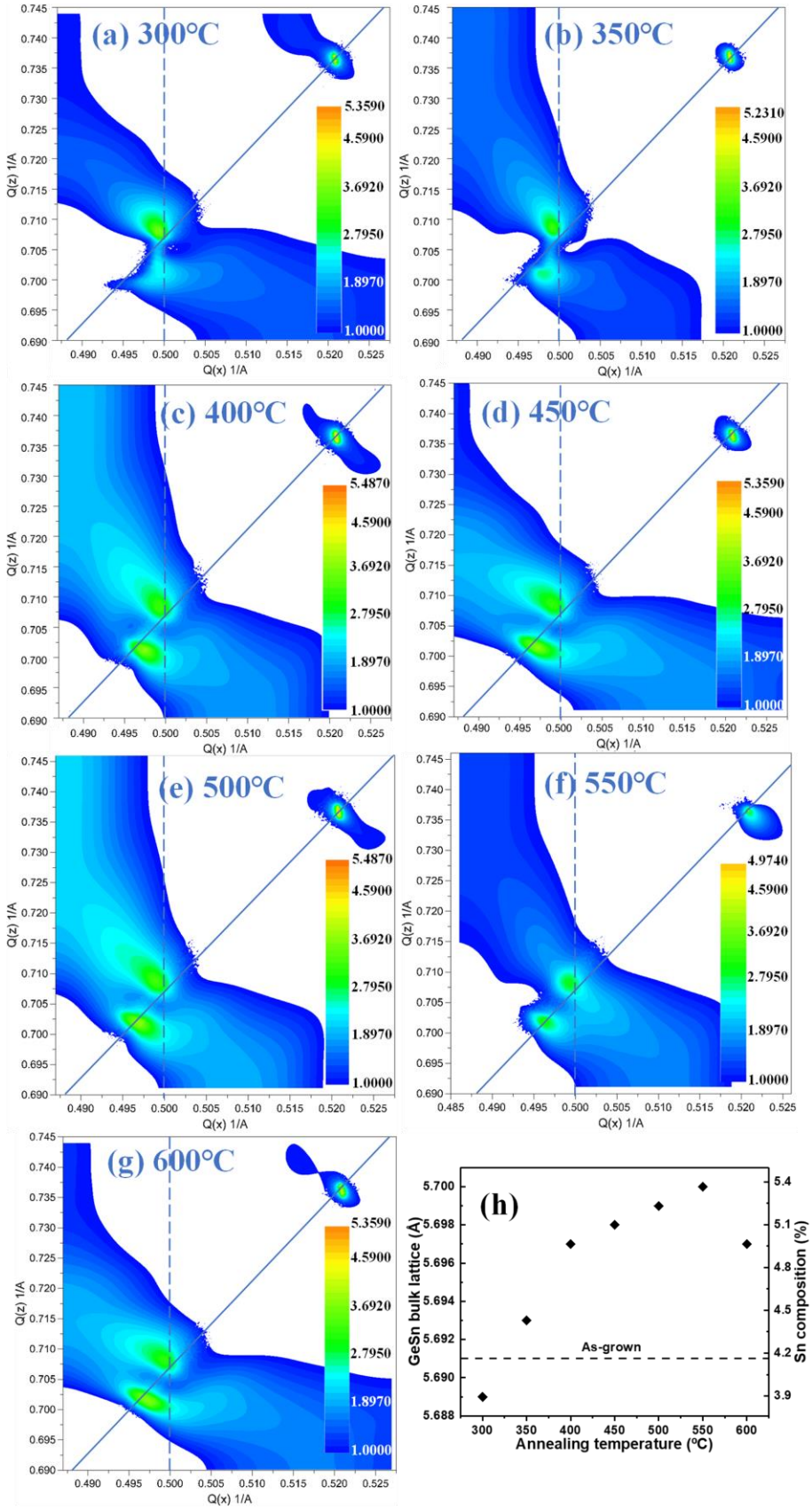

Figure 4-7 (a – g) Reciprocal space maps around (224) reciprocal lattice point of GeSn samples annealed at different temperatures between 300-600 °C. All the maps were set at the same log signal intensity (from 1.0000 to 6.0000) to compare the crystal quality via the mosaic spread. The scale bars show the log intensity range of the maps. (h) Calculated GeSn bulk lattice constants with increasing annealing temperature.

To provide possible explanations to these observations, in-plane and growth direction lattice constants of Ge and GeSn are summarised in Figure 4-8 (a – b). It can be seen from Figure 4-8 (a) that the 250 nm Ge buffer is under tetragonal tensile strain both before and after thermal annealing. The Ge in-plane lattice constant kept growing while the growth-direction parameter shrank correspondingly despite some fluctuations under thermal annealing between 300-500 °C, until annealing temperature reached 550 °C breaking this trend. The most pronounced Ge lattice parameter changes happened at 300 °C and 550 °C. Correspondingly, the GeSn epilayer is under tetragonal compressive strain before and throughout the thermal processing as shown in Figure 4-8 (b). The GeSn in-plane lattice constants keep growing with higher annealing temperatures between 350 and 550 °C while the growth-direction lattice constants are rather stable. 300 and 600 °C annealing caused significant in-plane lattice constant shrinkage of GeSn. At 300 °C the Ge in-plane lattice constant increased the most, indicating enlarged in-plane strain, which we suspect to be a result of the interaction between GeSn and the underlying Ge, as 300 °C annealing should not make significant difference to Ge, but it will change the behaviour of GeSn, especially the Sn diffusion. This provides some hints to explain the decreased lattice constant of GeSn under 300 °C annealing based on the postulation that the thermal energy stored in GeSn layer was consumed by inducing strain in the underlying Ge. At 550 °C the tensile-strained Ge turned to relax close to its bulk value. This observation is in line with our expectations and can be explained by the decreased GeSn lattice at the GeSn/Ge interface inducing less tensile strain on Ge. As for the increased in-plane GeSn lattice constant at 550 °C, one possibility is that the Sn out-diffusion left many vacancies at the GeSn lattice, the local strain was reduced by the combination of Sn atoms with vacancies [20], leading to expanded lattice constants. The increase in the total change of lattice constant from the sum of Ge and GeSn both in in-plane- and growth-direction and the raised strain relaxation at 550 °C, as presented in Figure 4-8 (c) and (d), respectively, support this assumption. Another important observation in our experiments is that the Sn segregation process under high temperature annealing, i.e., 550-600 °C is unequivocally different from the results of the pioneering work in this topic where a sudden Sn segregation inducing a stable low-Sn-composition (1%) phase within temperature change of around 20 °C after reaching the critical annealing temperature was observed for pre-relaxed GeSn [8]. From our results, the Sn segregation process is comparatively slow, with a final Sn

composition of 5%. Indeed, our results agreed with earlier work on the gradual Sn segregation process, and they reached a final Sn composition of 4.1% for a 160 nm GeSn grown on Ge/Si [42]. These contrasting behaviours were considered to derive from different growth conditions, i.e., chemical vapour deposition (CVD) or MBE growth as the growth temperature, and dynamics were different, underneath buffer layers in terms of thicknesses and defect conditions [27] and annealing processes where ex-situ rapid thermal annealing or in-situ gently-ramped annealing were adopted.

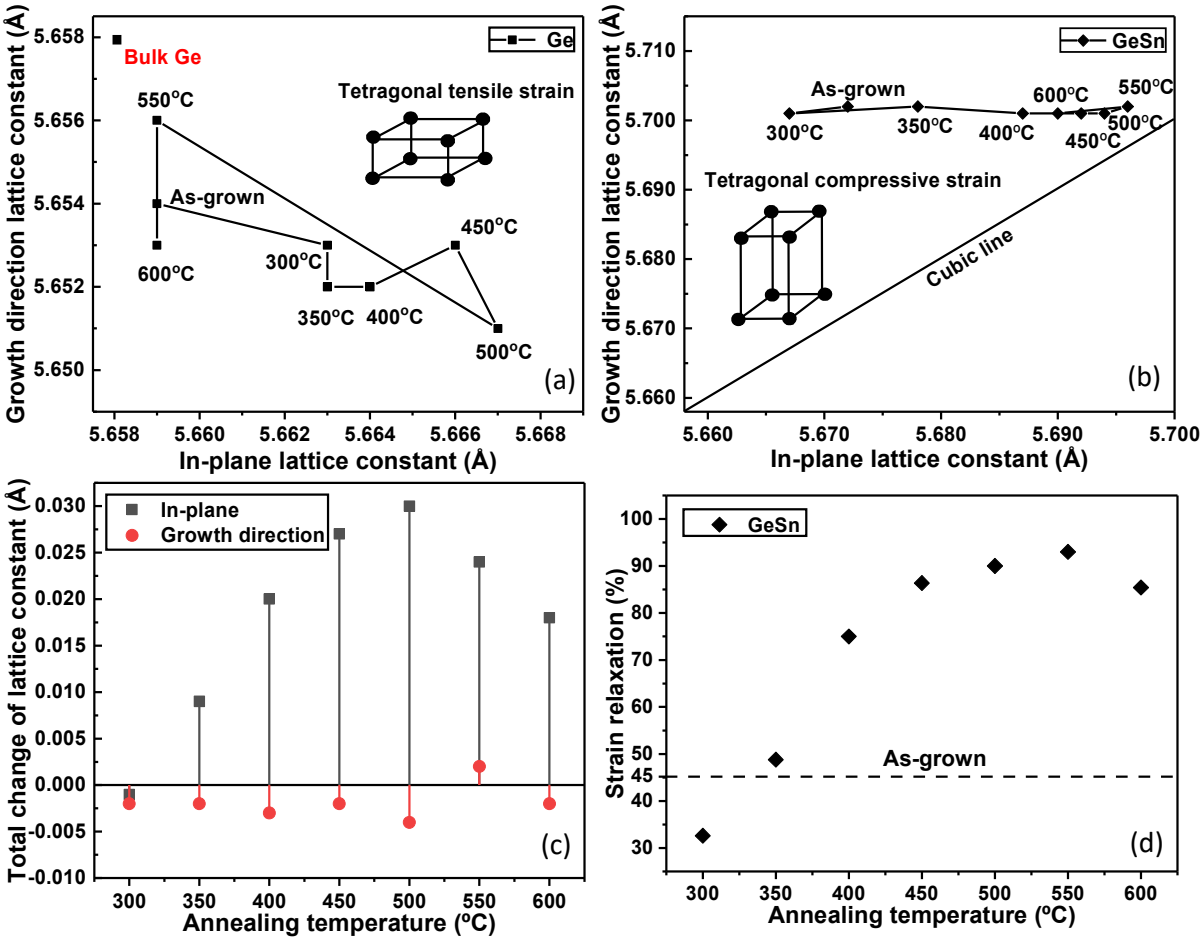

Figure 4-8 In-plane and growth direction lattice constants of (a) Ge buffer and (b) GeSn under different annealing temperatures. (c) A total change of lattice constant in Å. (d) Strain relaxation with annealing temperature measured from RSMs.

In summary, ex-situ rapid thermal processing was applied to 500 nm nominal 8% Sn composition GeSn samples grown on 250 nm Ge on Si (001) substrate by MBE at temperatures between 300-600 °C for 5 minutes each, aiming at finding the feasibility of using this annealed high-Sn-content GeSn layer as a buffer for GeSn laser devices. It was found from AFM images that the surface was slightly improved at 300-350 °C,

450-500 °C annealing, while the featured-GeSn surface was destroyed after annealing temperature reached 550 °C, indicating Sn-segregation process. Strain states within GeSn layer were probed quantitatively and qualitatively by HRXRD. It was found that below 600°C with increasing annealing temperature, the strain relaxation increased steadily, and peaked at 550 °C of 93%, despite the counter-intuitive decrease in 300 °C, which was considered to result from the interaction between GeSn and the underneath Ge layer. However, different behaviours with others' work for 'pre-relaxed' GeSn layer where they reported sudden Sn segregation and a sharp transition to a low-Sn-composition phase on critical annealing temperature were observed in our experiments, relatively gradual reduction in lattice constant after annealing temperature reaching 550 °C and a final Sn composition of 5% was found. These results show that although the thermal stability of GeSn varies significantly with Sn composition, strain state, underneath buffer and crystal quality, thick annealed GeSn layers can be used as buffer layers for GeSn-based optoelectronic devices to provide large extent of strain relaxation while maintaining crystal quality upon delicate selection of annealing conditions. An annealing temperature of 500 °C applied to a 500 nm GeSn buffer of nominal 8% Sn was the best fit in our case to provide matched-lattice parameters, strain relaxation and good crystal quality without Sn segregation for higher Sn composition GeSn active layer.

4.4 In-Situ Low-Temperature Thermal Treatment of Composition-Graded GeSn Buffer

In this section, a novel in-situ low-temperature thermal treatment is introduced to the growth of compositional-graded GeSn buffer layer for the realisation of subsequent high crystal quality high Sn composition GeSn active layer growth. Significant surface quality improvements have been verified with no Sn segregation on the surface observed. The couple Omega-2theta scans and reciprocal space maps (RSMs) reveal the Sn incorporation well-match the nominal values and that in the in-plane direction, the growth is pseudomorphic without strain relaxation, which indicates less introduction of crystal defects accompanied by strain relaxation. These results provide an innovative approach for growing high-Sn composition GeSn with improved surface quality, which is vital for the realisation of high-quality GeSn-based optoelectronic devices.

In general, thermal annealing is not favourable for GeSn-based devices as the thermal budget is notoriously low due to the low solid solubility of Sn in Ge and the

huge lattice mismatch. As introduced in Section 4.2 that most of the research interests on thermal annealing have been devoted to the ex-situ post-growth annealing for device fabrication considerations, in-situ annealing to facilitate GeSn growth is seldomly reported. The growth temperature of GeSn is very low (below 200 °C) and for high Sn compositions, e.g., 10 %, the growth temperatures have always been below 150 °C. Higher growth temperature is frequently shown to cause Sn segregation and epitaxial breakdown. Under such circumstances, in-situ thermal annealing is not considered beneficial for GeSn growth by the majority. To the best of the author's knowledge, there are two research papers addressing the in-situ annealing of GeSn films under ultra-high vacuum chamber. Improved crystallinity has been reported and enhanced GeSn infrared device performance by in-situ annealing is predicted by Zhang *et al* [29]. However, the annealing temperature used was 600 °C, which is a very high temperature for GeSn-based materials that could lead to severe Sn segregation. Actually, from their XRD results, a Sn composition of less than 2% has been found for the sample with a nominal Sn composition of 9%. Besides, the obtained rms roughness of the $Ge_{0.914}Sn_{0.086}$ is in the range of 8.16 nm to 19.58 nm, which is probably an indication of Sn segregation on the surface and not favourable for device fabrication requirements such as the electrode deposition. The other paper reports the behaviour of amorphous $Ge_{0.894}Sn_{0.106}$ under in-situ and ex-situ annealing at different temperatures [45]. In contrast to the expectation of the authors, in-situ annealing at 350 °C did not lead to a significant reduction of Sn composition, most of the Sn remain within the lattice, and substantial extent of crystallisation happened at temperatures higher than 400 °C. This enhancement in crystallinity with high in-situ annealing temperature (far beyond the eutectic temperature of GeSn of 231 °C) is in consistency with the results from the former paper. However, in the latter paper, significant phase segregation is reported for in-situ annealing at 500 °C, leading to a dramatic decrease in Sn composition and an observation of liquid Sn phase.

Inspired by the ex-situ annealing studies in section 4.2 and the above in-situ annealing studies in the literature, in this section, the in-situ annealing was performed at relatively lower temperatures, i.e., just several tens of degrees higher than the growth temperatures to prevent phase segregation. And this method is combined with compositional-graded GeSn buffer to achieve a high-crystal quality and high-Sn composition GeSn buffer for the subsequent GeSn active layer growth.

4.4.1 Rheed Observation During Growth

For the in-situ annealing studies, first two samples were grown: one is a graded-GeSn buffer grown on 500 nm Ge on Si substrate consisting of 150 nm $Ge_{0.97}Sn_{0.03}$, 150 nm $Ge_{0.95}Sn_{0.05}$ and 100 nm $Ge_{0.92}Sn_{0.08}$ and annealed at 180 °C, 180 °C and 130 °C, respectively, whose schematic structure is shown in Figure 4-9; the other one is a reference sample with the same GeSn epitaxial layers without the in-situ annealing processes and grown on a Ge buffer on Si substrate. The growth procedures of the Ge buffer layers followed the best Sb-doped Ge on Si growth described in Chapter 3. For the $Ge_{0.97}Sn_{0.03}$ and $Ge_{0.95}Sn_{0.05}$ growth, a large growth rate of 1.57 Å/s was used, and the substrate temperature was selected to be 140 °C, which can provide a better crystal quality while ensuring the prevention of Sn segregation. The growth temperature for $Ge_{0.92}Sn_{0.08}$ was 100 °C. The selection of in-situ annealing temperatures is also based on the Sn composition, the higher Sn composition, the lower annealing temperature shall be chosen to prevent phase segregation. Therefore, the annealing temperatures for $Ge_{0.97}Sn_{0.03}$ and $Ge_{0.95}Sn_{0.05}$ were chosen to be 180 °C, while that for $Ge_{0.92}Sn_{0.08}$ was selected to be 130 °C. 180 °C and 210 °C annealing to the top $Ge_{0.92}Sn_{0.08}$ layer have been examined to cause severe Sn surface segregation in a separate experiment. On the other hand, if the annealing temperature was only slightly higher than the growth temperature (e.g., smaller than 10 °C higher), from RHEED no pattern change was observed.

Annealing @ 130 ℃ for 10 minutes
100 nm $Ge_{0.92}Sn_{0.08}$ @ 100 ℃
Annealing @ 180 ℃ for 10 minutes
150 nm $Ge_{0.95}Sn_{0.05}$ @ 140 ℃
Annealing @ 180 ℃ for 10 minutes
150 nm $Ge_{0.97}Sn_{0.03}$ @ 140 ℃
20 nm Ge @ 140 ℃
500 nm Ge buffer
Si (001) substrate

Figure 4-9 Schematic growth structure for the sample with low-temperature in-situ annealing.

The growth of each GeSn layer and the annealing processes were investigated in-situ by RHEED, as shown in Figure 4-10. After finishing the 500 nm Ge buffer growth on Si, smooth and streaky 2 × 2 patterns were observed, symbolising the surface flatness after the Ge buffer growth, which has been proved by AFM studies in Chapter

3. A rms roughness of around 1 nm is typically obtained after the 500 nm Ge buffer growth. Then, just after a few seconds of deposition of the $Ge_{0.97}Sn_{0.03}$ layer, the 2 × patterns completely vanished, and the main patterns transformed from streaky lines to dashed lines, as presented in Figure 4-10 (a). The degree of line broken increased with increasing deposition thickness, and the shape of the fundamental patterns gradually changed towards spotty dashes. The main patterns were very bright. However, this situation changed dramatically when the in-situ annealing proceeded. When the substrate temperature reached above 160 °C, the RHEED patterns suddenly changed from dashed 1 × 1 patterns to streaky patterns, with several reconstruction patterns in between the fundamental patterns. As the background of the RHEED was a bit cloudy around the main patterns, it was difficult to distinguish the patterns clearly, but they were highly likely to be 4 × 4 patterns, which can be seen in Figure 4-10 (d). It was also noted that the setting temperature of annealing was 180 °C, however, the actual temperature overshot to 220 °C, and the ten-minute annealing actually happened at 220 °C. After that, the substrate was cooled to 140 °C for the next layer of $Ge_{0.95}Sn_{0.05}$ growth. It was found that just as the first GeSn layer, almost immediately after the start of the $Ge_{0.95}Sn_{0.05}$ layer, the diffraction patterns disappeared and the fundamental patterns become dashed lines, as depicted in Figure 4-10 (b). The ‘dash’ lines are shorter compared to the $Ge_{0.97}Sn_{0.03}$ layer, indicating a rougher surface. After the thermal annealing procedure, the surface became the same as that of the first GeSn layer after annealing. Streaky lines with reconstruction patterns were resumed, but the brightness of the patterns was slightly decreased, in Figure 4-10 (e). The growth of the last layer, $Ge_{0.92}Sn_{0.08}$ was carried out at 100 °C after cooling down from the second annealing step. The as-grown $Ge_{0.92}Sn_{0.08}$ layer shows spottier RHEED patterns, as seen in Figure 4-10 (c), representing the growth morphology shift from two-dimensional towards three-dimensional mode. The patterns are still very bright without the appearance of the ring-shape patterns, which means the grown film should still be crystalline. The annealing temperature was selected to be 130 °C, but in reality, it overshot to around 160 °C. Better temperature control can be realised by applying a smaller temperature ramp rate, however, this will add a variable to the experiment and can be investigated separately in the future. An instant RHEED pattern change happened at around 150 °C, see Figure 4-10 (f), where the streaky patterns were partially recovered to connected

dashed shapes, and weak reconstruction patterns between the fundamental patterns have been observed. The patterns were bright.

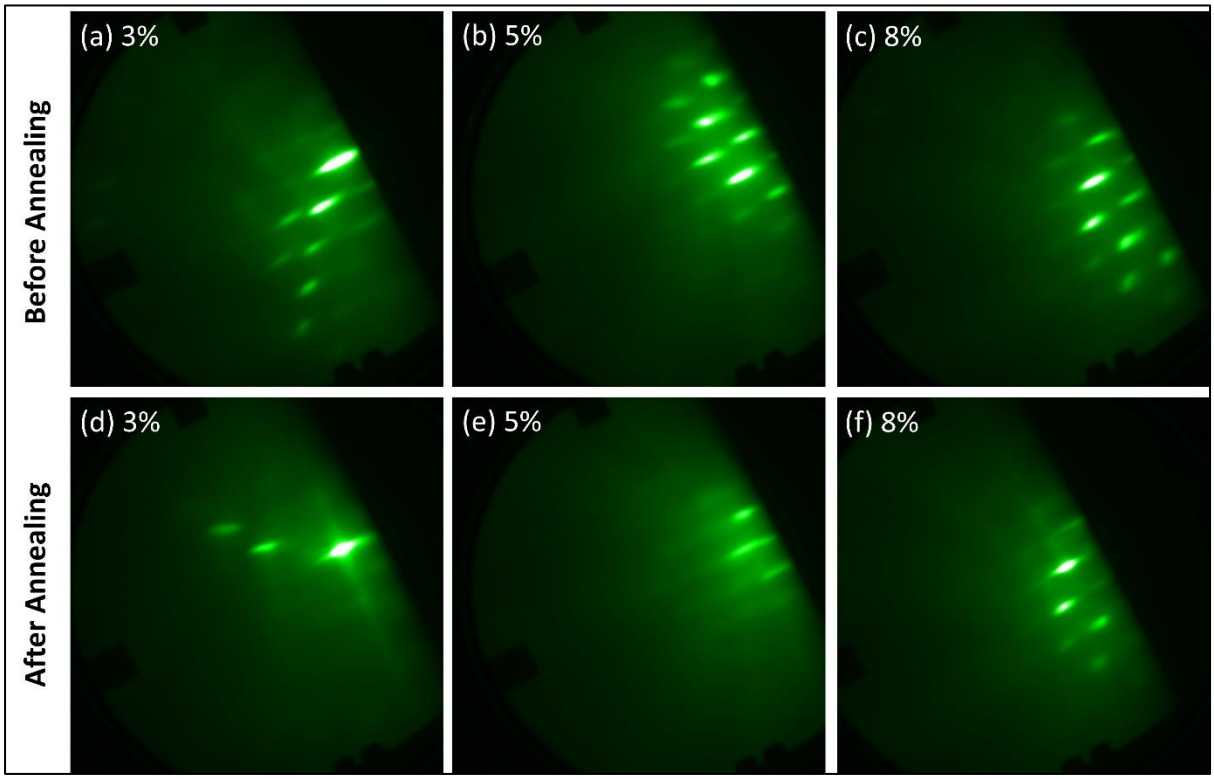

Figure 4-10 RHEED observations for nominal (a) 3% (b) 5% and (c) 8% Sn GeSn layer before in-situ low-temperature annealing and that of samples with nominal Sn compositions (d) 3% (e) 5% and (f) 8% after in-situ low-temperature annealing.

4.4.2 Surface Morphology Improvement

The surface morphology of the two samples were characterised by AFM images, as shown in Figure 4-11. Compared with the 500 nm $Ge_{0.92}Sn_{0.08}$ layer directly grown on Ge buffer on Si, as discussed in section 4.3.1, where the surface is featured in hills and valleys decorated with numerical white tiny dots, the growth applying graded GeSn layers present much flatter surface morphology, they exhibit surfaces just like Ge grown on Si. For samples both with and without in-situ low-temperature annealing, the surface roughness is lower than 3 nm, and the surface morphologies are similar with the surface of Ge grown on Si substrate. Remarkably, the sample with low-temperature in-situ annealing has a low rms roughness of 1.9 nm, estimated from 10 × 10 μm^2 AFM images, as can be seen in Figure 4-11 (b).

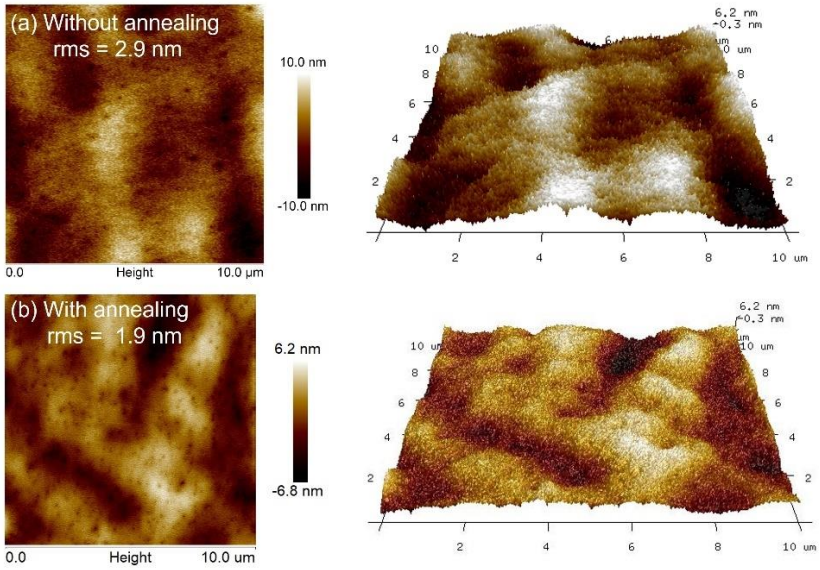

Figure 4-11. AFM images of 10 × 10 µm^2 for the samples (a) without and (b) with low-temperature in-situ annealing.

4.4.3 Strain State

Sn incorporation has been first investigated by high-resolution XRD omega-2theta scan around (004) plane. As shown in Figure 4-12, for both the reference sample and sample with in-situ annealing, well-defined narrow peaks for different Sn composition GeSn have been observed, indicating high crystal quality of the GeSn layers. The peak position of Ge for both samples represents a compressive strain of 0.14% (as labelled next to the Ge peak in Figure 4-12). Considering the asymmetric shape of the Ge peak, the slightly smaller Ge lattice is likely to be attributed to the Ge/Si interdiffusion induced by the repeated thermal cycles. From the GeSn peak positions, Sn compositions of 7.48% ,4.68% and 3.13% are found for the reference sample, while for the in-situ annealed sample the Sn compositions are 7.64%, 4.9% and 2.6%, corresponding to the nominal values of 8%, 5% and 3%, respectively. The Sn compositions obtained from XRD omegas-2theta scan along (004) plane for the nominals 8% and 5% agree well for the reference sample and the annealed sample, which are slightly lower than the nominal values. The small difference between the nominal value and the actual composition may come from the fact that when opening the shutter, the heat from the single-zone crucible dissipates to the chamber and causes a decrease in the composition. Therefore, usually marginally overtemperature is applied to match the nominal Sn composition. In addition, the incorporation of Sn is affected by compressive strain within the lattice. For the nominal 3% layer, however, after in-situ annealing the peak shifts to the smaller lattice side, and an insignificant

decrease in intensity has also been observed. This may indicate the phase segregation, therefore, another sample with $Ge_{0.97}Sn_{0.03}$ only was grown with in-situ annealing to further confirm the status of phase segregation and will be discussed later. For these two graded GeSn buffer samples, asymmetric RSMs around (224) lattice planes were analysed to further investigate the strain in both growth direction and in-plane direction.

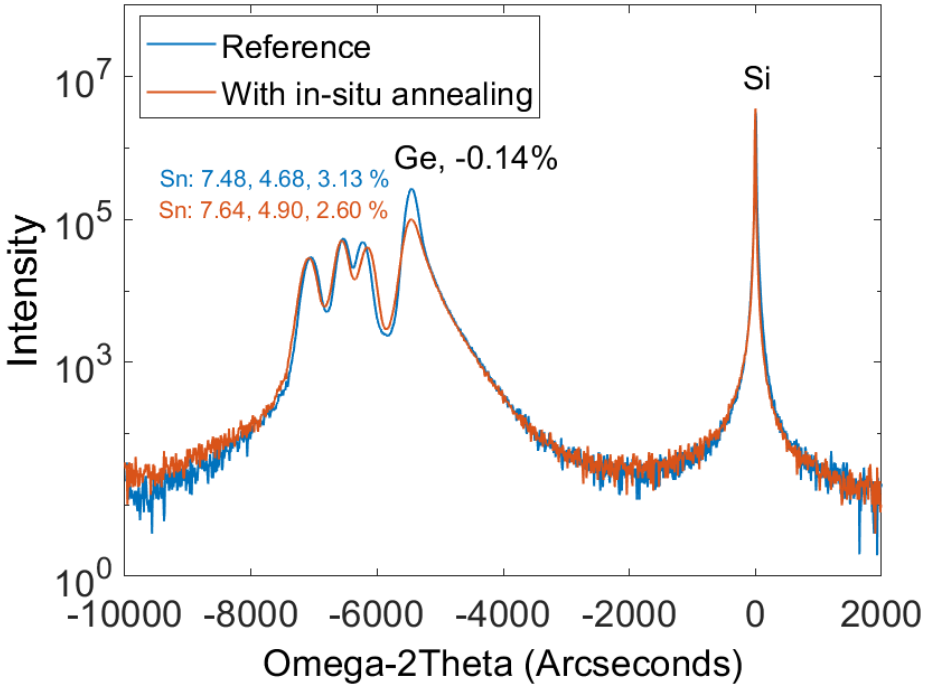

Figure 4-12 HRXRD symmetric omega-2theta scans around (004) lattice plane of the reference sample and the sample with in-situ annealing.

The RSMs of the reference sample and the annealed sample are shown in Figure 4-13 (a) and (b), respectively. The peak positions of Si, Ge and GeSn have been labelled in the right-hand side of the corresponding peaks in the figure. There is no significant GeSn peak position shift between the two samples, indicating the low-temperature in-situ annealing did not induce significant strain relaxation or phase segregation. In addition, the growth of GeSn in the in-plane direction is almost completely pseudomorphic for both samples, as can be concluded from the same *Q(x)* values (Omega tilts, which correlates to the in-plane lattice parameter) of GeSn peaks as that of Ge. The lattice parameters of Ge and GeSn with different Sn compositions both in in-plane direction and growth direction have been extracted from the RSMs and summarised in Table 1. It can be concluded that for both reference sample and in-situ annealed sample, the Ge buffer layer is tensile-strained in the in-plane direction and compressively strained in the growth direction, therefore the Ge buffer is under

tetragonal tensile strain, which should predominantly originate from the GeSn layers above. Whereas for the GeSn layers for both samples, tetragonal compressive strain is observed, particularly, the in-plane direction is completely strained by the Ge layer underneath.

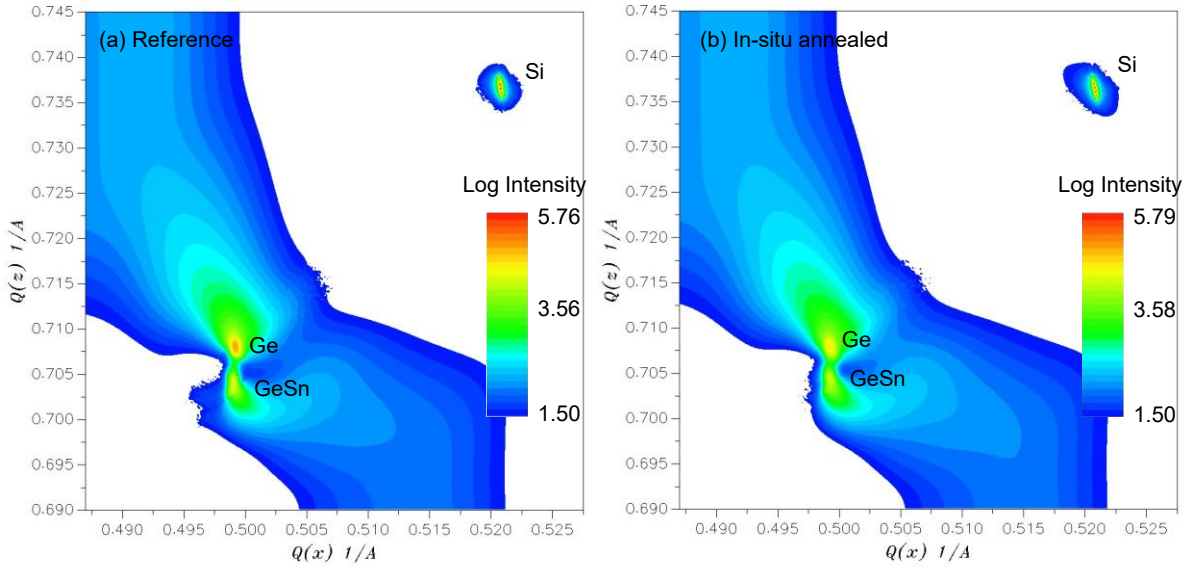

Figure 4-13 Reciprocal space maps of the reference sample (a) and the in-situ annealed sample (b) along (224) lattice plane. Form these maps, in-plane (a_i) and growth direction (a_g) lattice constants can be calculated by $a_i = 2\sqrt{2}/Q(x)$ and $a_g = 4/Q(z)$, respectively.

Table 4-1. Lattice Parameters, Sn Composition and Strain Relaxation Calculated from Reciprocal Space Maps. $N_{Sn\%}$ is nominal Sn composition, $M_{Sn\%}$ is measured Sn composition and $\varepsilon_{GeSn,R}$ is the strain relaxation of GeSn.

Sample	$a_{Ge\ \parallel}$	$a_{Ge\ \perp}$	$a_{Ge\ bulk}$	$N_{Sn\%}$	$a_{GeSn\ \parallel}$	$a_{GeSn\ \perp}$	$a_{GeSn\ bulk}$	$M_{sn\%}$	$\varepsilon_{GeSn,R}$
Ref	5.666	5.653	5.658	3	5.667	5.681	5.676	2.24	0
	$\varepsilon_{Ge,R}$ Tetragonal tensile strain			5	5.667	5.684	5.678	2.49	0
	0.14%	-0.09%	0%	8	5.667	5.689	5.681	2.87	0
Ann.	5.665	5.652	5.657	3	5.665	5.678	5.673	1.87	0
	$\varepsilon_{Ge,R}$ Tetragonal tensile strain			5	5.665	5.681	5.675	2.12	0
	0.12%	-0.11%	-0.02%	8	5.665	5.684	5.677	2.37	0

As the ultimate goal is to grow high Sn composition GeSn on this graded-GeSn buffer, normally in the in-plane direction lattice parameters are preferred to be relaxed for the subsequent growth. However, as the solid solubility of Sn in Ge is less than 1%, the relaxation of GeSn film is easily accompanied by Sn clustering. From the previous experience, even with the Ge strain compensation method, the growth of 400 nm $Ge_{0.9}Sn_{0.1}$ directly on Ge substrates suffered from phase segregation, although the growth was likely to be crystalline (observed from RHEED). Therefore, the strain relaxation process needs to be controlled to ensure the crystalline growth of the

higher-composition GeSn [11]. In the following part of this section, the effects of in-situ low temperature annealing are evaluated by 1) probing the surface morphology and strain just after the $Ge_{0.97}Sn_{0.03}$ growth to examine the phase segregation. 2) doubling the total thickness of the GeSn gradient layers for strain relaxation analysis.

As discussed earlier for Figure 4-12 that the reason for the peak position shift of the nominal $Ge_{0.97}Sn_{0.03}$ layer in annealed sample remains unclear, another sample of 300 nm $Ge_{0.97}Sn_{0.03}$ applying the in-situ annealing method every 100 nm was grown to examine the phase segregation status. The growth structure is shown in Figure 4-14 (a). As the growth was monitored in-situ by RHEED, the temperature of the last annealing step was elevated to 220 °C because no observable degradation of the streaky patterns or dimmed background were found, and higher temperature may enhance the effects of the method under investigation. No surface Sn clusters are observed from AFM examination and a low surface roughness of 0.466 nm is obtained from the 10 × 10 μm^2 AFM image, as shown in Figure 4-14 (b). HRXRD symmetric omega-2theta scan around (004) lattice plane of the sample is shown in Figure 4-14 (c). The peak positions of the Ge and GeSn have been labelled in the figure, and a Sn composition of 3.45 % is estimated from the lattice parameter extracted from symmetric XRD scan. From the RSM in Figure 4-14 (d), the growth is completely strained in the in-plane direction, while in the growth direction, the lattice constant is 5.68 Å, which equals a Sn composition of 3.1 %. Based on these results, no sign of phase segregation is found, which is contrary to the case in the graded GeSn buffer grown on Si substrate, making one to relate the potential of phase segregation to underneath Ge buffer layer. As it has been reported in [8] that the threading dislocation network is a preferred diffusion pathway for Sn precipitates, in the case of this study, one possible explanation for the peak shift in the first 400 nm of the sample is segregation on the surface. Under annealing, the Sn precipitates diffuse through threading dislocations to the $Ge_{0.97}Sn_{0.03}$/Ge interface so that they are not probed by AFM.

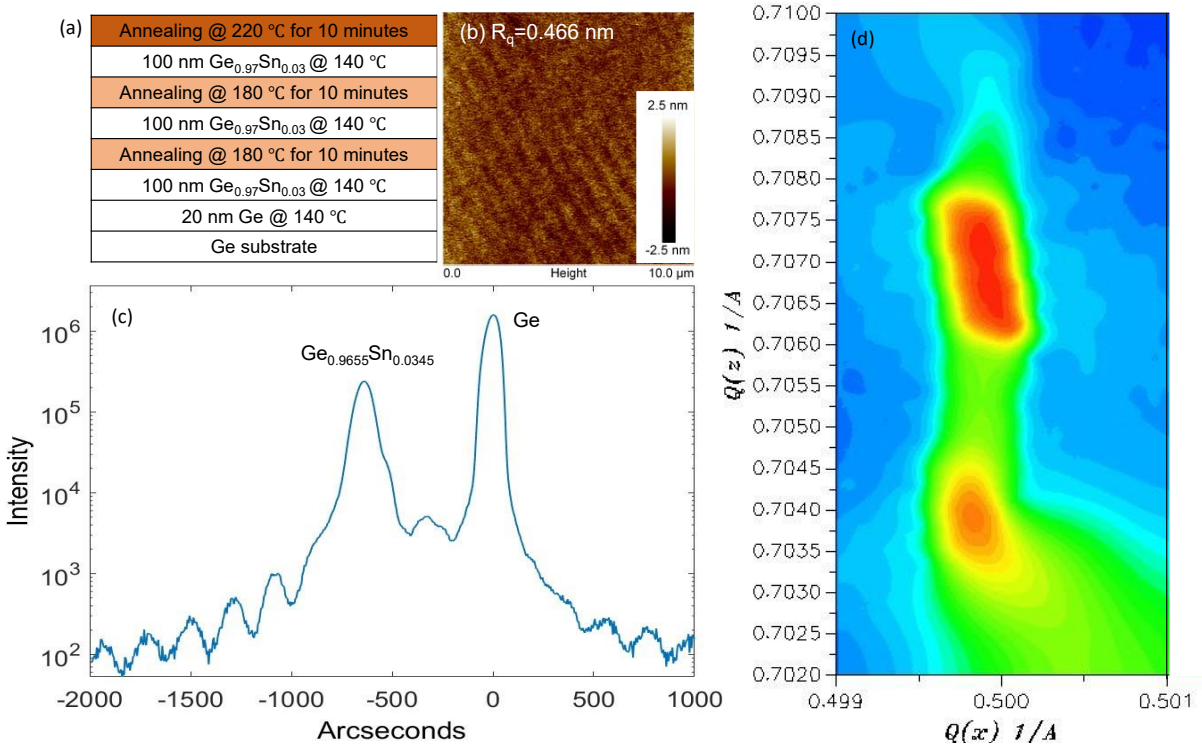

Figure 4-14 (a) Growth structure of 300 nm $Ge_{0.97}Sn_{0.03}$ on Ge substrate with in-situ low temperature annealing method. (b) 10 × 10 µm² AFM image of the sample. (c) HRXRD symmetric omega-2theta scan around (004) lattice plane of the sample. The peak positions of the Ge and GeSn have been labelled in the figure, and the Sn composition estimated from the lattice parameter has also been marked in the figure. (d) HRXRD reciprocal space map around (224) lattice plane of the sample.

Another sample with a total thickness of 800 nm whose growth structure is shown in Figure 4-15 (a), was grown on Si substrate applying the in-situ low temperature method to investigate the strain relaxation by this method. The temperatures for annealing for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.95}Sn_{0.05}$, and $Ge_{0.92}Sn_{0.08}$ are 200 °C, 180 °C and 130 °C, respectively. Although a higher surface roughness of 3.07 nm compared to the 400 nm annealed sample has been probed by 10 × 10 µm² AFM image, as shown in Figure 4-15 (b), it is still comparable to that of the 400 nm reference sample without annealing (R_q = 2.9 nm), and there is no phase segregation observed on the surface. However, significant peak shifts are found for the GeSn layers compared to the reference and 400 nm annealed samples, as shown in the HRXRD omega-2theta scan in the (004) plane in Figure 4-15 (c). The calculated Sn compositions are 2.59 %, 4.19 % and 6.80 %, respectively for the nominal $Ge_{0.97}Sn_{0.03}$, $Ge_{0.95}Sn_{0.05}$, and $Ge_{0.92}Sn_{0.08}$ layers. The peak shift for the nominal $Ge_{0.97}Sn_{0.03}$ layer can be explained by the threading dislocation facilitated Sn diffusion towards the interface with Ge, as just mentioned. For the nominal $Ge_{0.95}Sn_{0.05}$ and $Ge_{0.92}Sn_{0.08}$ layers, the peak shifts towards smaller lattice side are possible to be accounted by the extended duration or cycles of annealing and increased strain accumulation during the continuous growth.

RSM in the (224) plane shown in Figure 4-15 (d) reveals the completely pseudomorphic growth of the GeSn layers as they have almost identical in-plane lattice constants with the underlying Ge buffer layer, i.e., they are fully strained to match the Ge crystal lattice.

It can be concluded from the latter two samples that although the in-situ low temperature annealing method leads to the decreased lattice parameter of the nominal $Ge_{0.97}Sn_{0.03}$ layer grown on Si substrate, which is likely to be explained by the enhanced Sn precipitation through the dislocation network originated from the Ge/Si interface, the surface quality of the subsequent higher-composition GeSn layers can be significantly improved by this method. In other words, the large strain induced by continuous Sn incorporation is partially released through the downward Sn diffusion to the lower interface. The duration and number of cycles of in-situ low-temperature annealing applied can be further optimised to avoid phase segregation and improve surface quality at the same time.

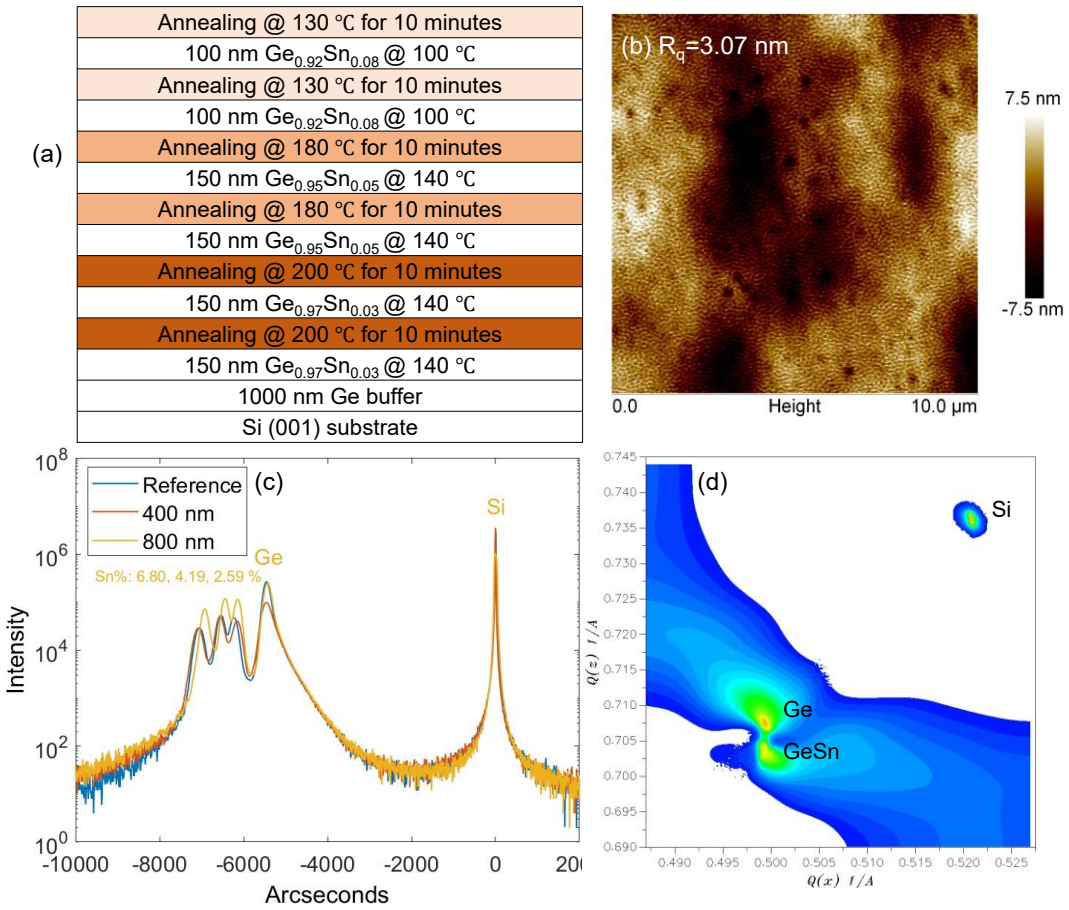

Figure 4-15 (a) Growth structure of graded GeSn layers with a total thickness of 800 nm with in-situ low temperature annealing method. (b) 10 × 10 μm² AFM image of the sample. (c) HRXRD symmetric omega-2theta scan around (004) lattice plane of the 800 nm sample with in-situ annealing and those of the reference sample and the annealed sample of a total thickness of 400 nm. The peak positions of the Ge and GeSn have been labelled in the figure, and the Sn composition estimated from the lattice parameter has also been marked in the figure. (d) HRXRD reciprocal space map around (224) lattice plane of the sample.

4.5 GeSn/Ge Multi-Quantum Wells (MQWs) Grown on Si Substrates

4.5.1 Surface and structural analysis

In this section, the growth and characterisation of MQW structure consisting of ten repeats of $Ge_{0.9}Sn_{0.1}$/Ge (10 nm/20 nm) based on the in-situ annealed graded GeSn buffer layer grown on Si are presented, showing the potential of this method for achieving high crystal quality GeSn active region for light emission purposes. The schematic growth structure is shown in Figure 4-16 (a). After growing the 400 nm graded GeSn buffer with the in-situ low temperature annealing method on Ge/Si substrate, the MQWs were grown at a substrate temperature of 100 °C, followed by the growth of 65 nm Ge cap layer at the same temperature. The surface roughness obtained from 100 μm^2 AFM image (Figure 4-16 (b)) is 2.71 nm.

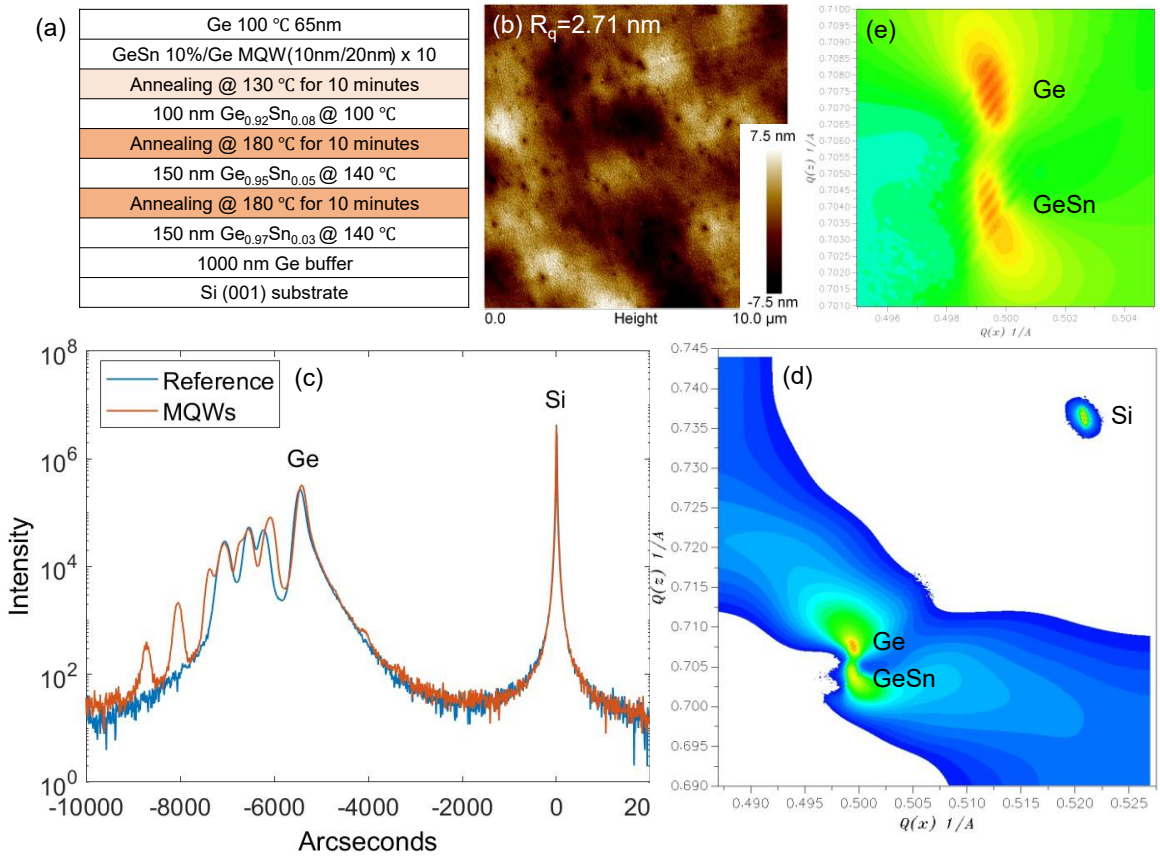

Figure 4-16 (a) Growth structure of GeSn/Ge MQWs on graded GeSn layers with a total thickness of 400 nm with in-situ low temperature annealing method. (b) 10 × 10 μm^2 AFM image of the sample. (c) HRXRD symmetric omega-2theta scan around (004) lattice plane of the MQW sample with a reference to un-annealed graded GeSn buffer on Ge/Si substrate. (d) HRXRD reciprocal space map (RSM) around (224) lattice plane of the sample. (e) Enlarged RSM showing the Ge buffer and GeSn peaks.

A crystal quality check was performed by XRD single scan around the (004) plane, as shown in Figure 4-16 (c). With reference to the unannealed graded GeSn buffer layer on Ge/Si substrate, the peak positions for nominal Sn compositions of 5 % and 8 % GeSn layers agree very well with the reference sample. Multiple satellite

diffraction peaks can be observed symbolising the precise spatial periodicity of the crystal structure. HRXRD RSMs (Figure 4-16 (d) and enlarged RSM (Figure 4-16 (e)) in the (224) lattice plane reveal the pseudomorphic growth nature of the structure, which may be a sign of the high crystal quality, as strain relaxation will lead to defects.

4.5.2 TEM investigation of the MQWs

High-resolution scanning transmission electron microscopy (STEM) observations were performed by Dr. Mateus Gallucci Masteghin at University of Surrey to further investigate the material quality of the MQWs, as shown in Figure 4-17. Different layers can be easily distinguished from the grey scale of the image. The more greyish colour refers to Ge and the lighter regions corresponds to Sn-containing layers, which have been labelled in Figure 4-17. Sharp interface between the layers have been found, confirming the existence of composition contrast. The thicknesses of the graded GeSn buffer layers are inconsistent with the nominal values. No threading dislocations have been observed from the entire image. The normalised grey scale of the MQW region has been extracted from the image and presented in Figure 4-18, indicating the correct thicknesses of QWs and barriers and the sharp interface.

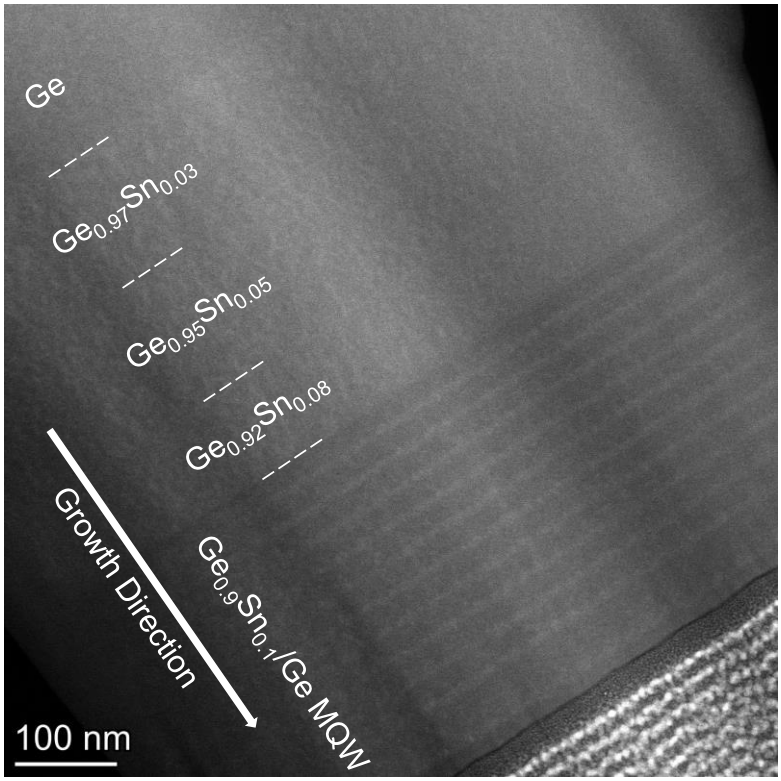

Figure 4-17. STEM image of the MQWs sample.

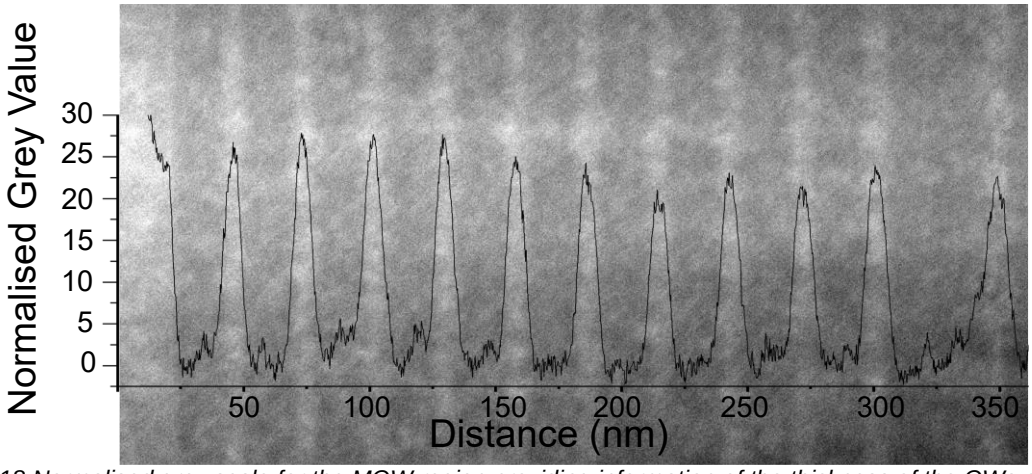

Figure 4-18 Normalised grey scale for the MQW region providing information of the thickness of the QWs and the spatial separation between them.

Higher magnification TEM images showing the interfaces between different composition GeSn layers and that with Ge buffer have been shown in Figure 4-19. Figure 4-19 (a) is a larger scale image. Grey scale contrast can be clearly seen for Ge and GeSn layers, while the difference between each GeSn layer is not obvious. Marked regions in orange, green and blue are areas where smaller scale high-resolution images are taken. Specially, higher magnification images for the interface of Ge/$Ge_{0.97}Sn_{0.03}$ ($Int_{Ge,3}$) are shown in Figure 4-19 (b)(e), that of $Ge_{0.97}Sn_{0.03}$/$Ge_{0.95}Sn_{0.05}$ ($Int_{3,5}$) are shown in Figure 4-19 (c)(f), and that of $Ge_{0.95}Sn_{0.05}$/$Ge_{0.92}Sn_{0.08}$ ($Int_{5,8}$) are presented in Figure 4- (d)(g). It is found that at $Int_{3,5}$ and $Int_{5,8}$, there are dark-contrast lines decorated with a faint bright-contrast line on the left, which are hints for GeSn phase segregation. Thermally driven downward precipitation during low temperature annealing rather than the abrupt Sn flux increase during the growth is the most probable reason to account for the observed phase segregation because the surface characterisation demonstrates no surface segregation, as shown in section 5.4.1. The atomic scale observations Figures 4- (e – g) demonstrate the impressive high quality of the layers where no defects are found. This can be attributed to the pseudomorphic growth nature suppressing the defect generation through relaxation. Figure 4- (f) and (g) confirm the existence of the composition contrast areas while leaving the rest of the layer defect-free. This phase segregation down to the lower interface may also provide a path for strain relaxation and will not affect the active region.

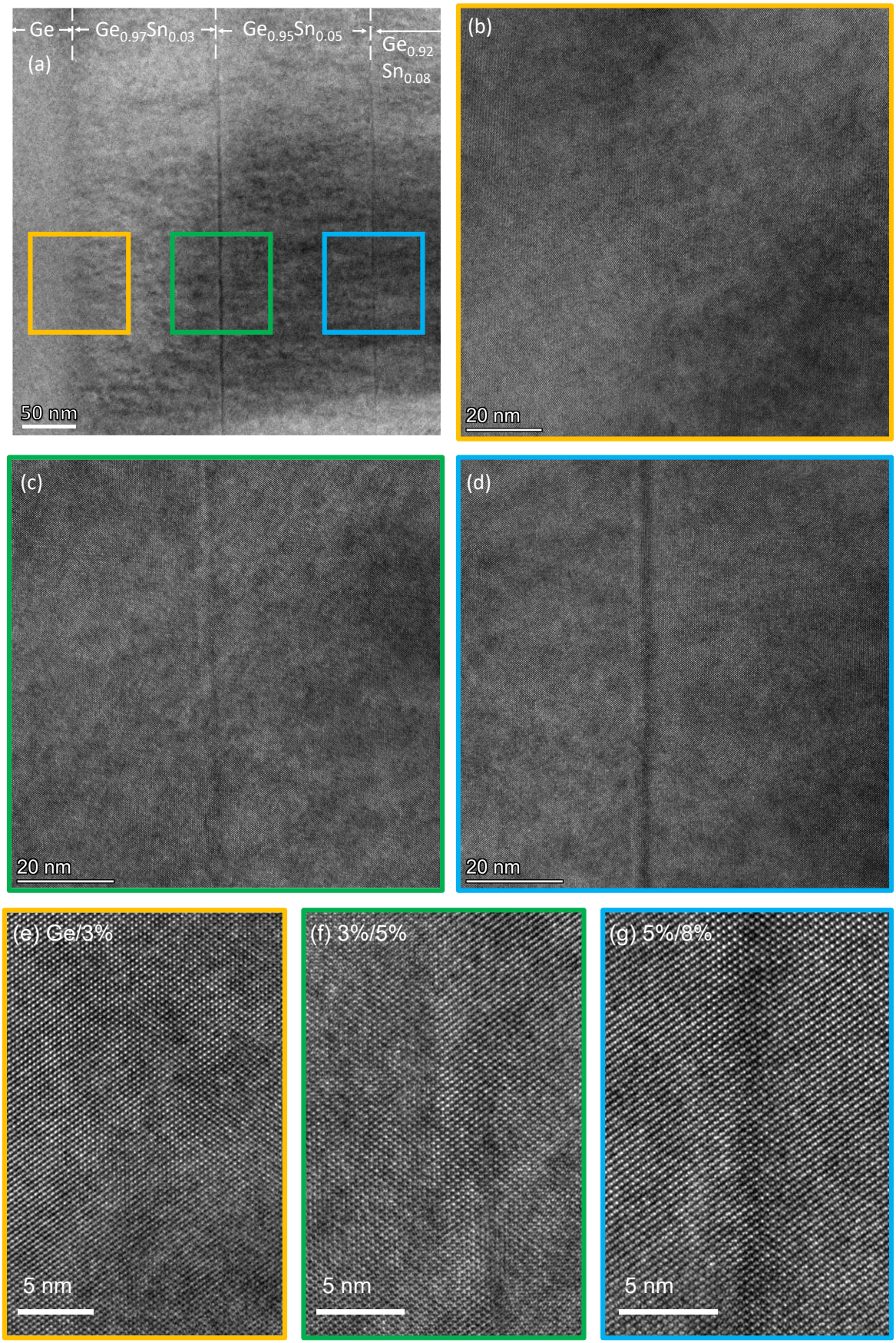

Figure 4-19 Higher magnification TEM images showing the interfaces between different composition GeSn layers and that with Ge buffer. (a) is a larger scale image marking the areas where higher-resolution images are taken. Orange, green and blue coloured boxes are used to refer to the interface of Ge/$Ge_{0.97}Sn_{0.03}$ (b)(e), $Ge_{0.97}Sn_{0.03}$/$Ge_{0.95}Sn_{0.05}$ (c)(f), and $Ge_{0.95}Sn_{0.05}$/$Ge_{0.92}Sn_{0.08}$ (d)(g).

Figure 4-20 (a) shows high resolution MQW region of the sample. Well defined QWs equally spaced between Ge barriers can be seen. The horizontal brighter marks that run across all layers are the curtain effect from focused ion beam polishing. The darker regions are $Ge_{0.9}Sn_{0.1}$ QWs and undulations along the layers are due to height difference either because of bending (very thin and long lamella) or the curtain effect in a TEM. In enlarged QW image Figure 4-20 (b) Ge and $Ge_{0.9}Sn_{0.1}$ QWs have been labelled. As the precisely controlled thickness achieved by MBE growth, no defects are detected among the MQWs. This have been further confirmed by the fast Fourier transform (FFT) images (Figure 4-21 (a)) taken from the larger-scale STEM image (Figure 4-21 (f)) and those from the interfaces of each layer (Figure 4-21 (b – e)). If any defects exist, they will present in between the diffraction patterns, which is not observed in any of the FFT images in Figure 4-21, symbolising the high crystal quality of the grown film.

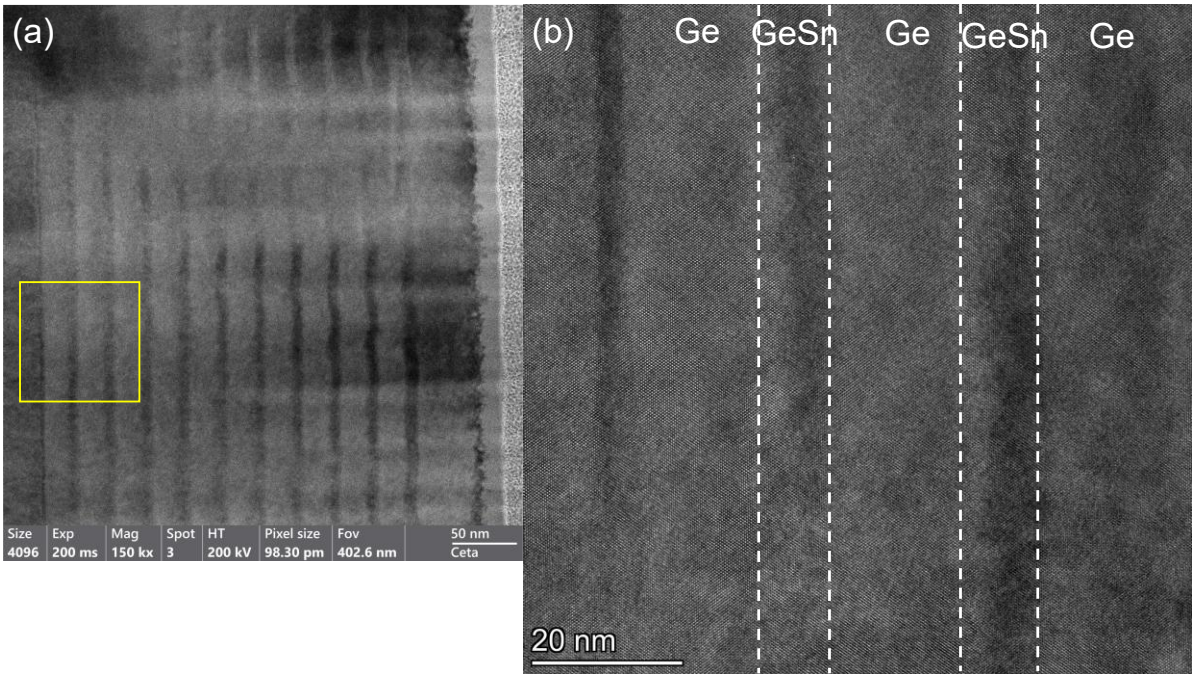

Figure 4-20 (a) High resolution TEM images of the MQW region and (b) a higher magnification image close to the bottom of the MQW region marked in the yellow box of (a).

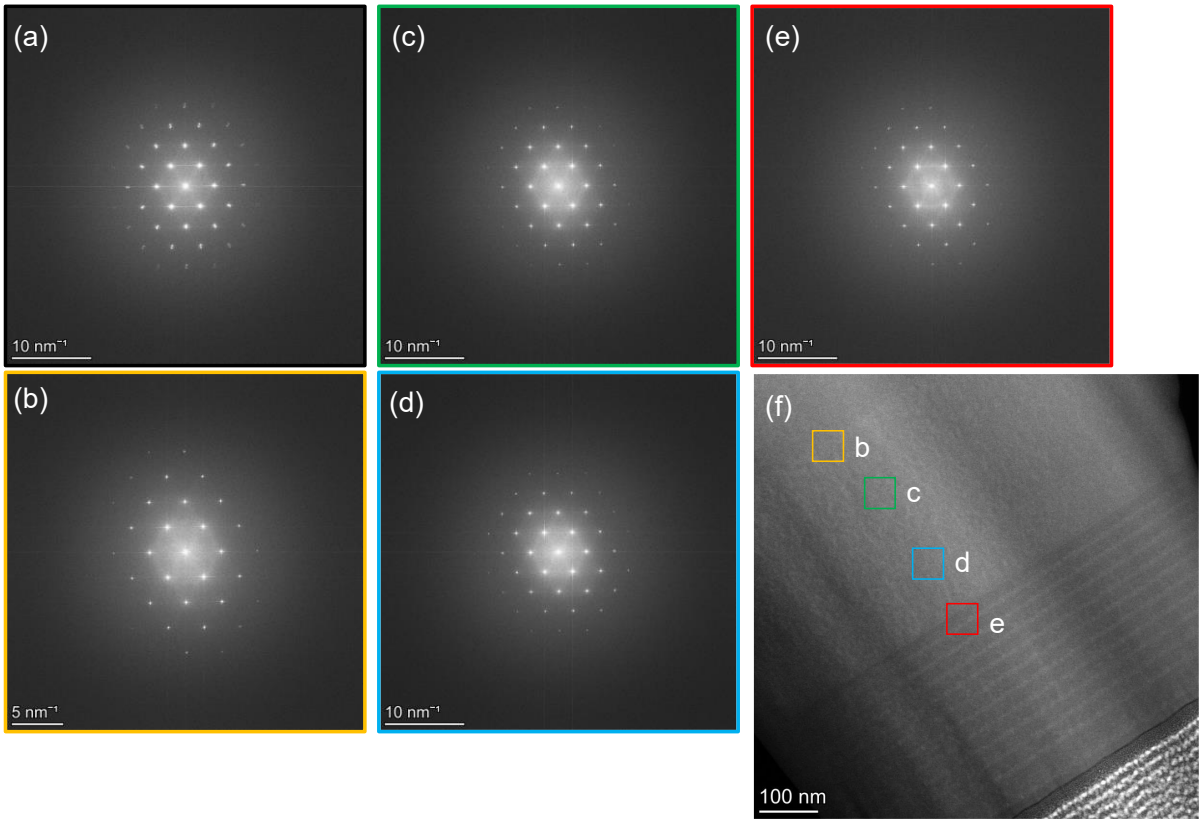

Figure 4-21 (a) Fast Fourier transform patterns obtained from the whole image (f); and (b – e) at the interfaces between the layers labelled in the corresponding coloured boxes in the larger scale STEM image (f).

4.6 Summary

The first part of work in this chapter investigates the growth optimisation of applying a strain-compensation method realised by inserting an ultra-thin Ge layer among GeSn layers. The accumulated strain in the GeSn layer can be recovered almost immediately after the start of the Ge insertion layer growth. Reduced surface roughness can be gained for the growth of GeSn layer with a Sn composition of 10 %. Facilitated by Sb surfactant, the rms roughness of 150 nm $Ge_{0.9}Sn_{0.1}$ grown on Ge substrate can be further reduced to 0.76 nm. As a promising barrier material for GeSn active region, $Si_{0.013}Ge_{0.887}Sn_{0.1}$ grown by this method presents a rms as low as 0.56 nm.

The second part of work in this chapter focuses on the ex-situ rapid thermal annealing studies on 500 nm nominal $Ge_{0.92}Sn_{0.08}$ samples grown on Ge/Si substrates, aiming at finding the feasibility of using this annealed high-Sn-content GeSn layer as a buffer for GeSn laser devices. It was found from AFM images that the surface quality was slightly improved at 300-350 °C, 450-500 °C annealing, while the featured-GeSn surface was destroyed after the annealing temperature reached 550 °C, indicating Sn-segregation process. Strain states within GeSn layer were probed quantitatively and

qualitatively by HRXRD. It was found that below 600°C with increasing annealing temperature, the strain relaxation increased steadily, and peaked at 550 °C (93%), despite the counter-intuitive decrease in 300 °C, which was considered to result from the interaction between GeSn and the underneath Ge layer. However, different behaviours with others' work for 'pre-relaxed' GeSn layer where they reported sudden Sn segregation and a sharp transition to a low-Sn-composition phase on critical annealing temperature were observed in our experiments, relatively gradual reduction in lattice constant after annealing temperature reached 550 °C and a final Sn composition of 5% was found. These results show that although the thermal stability of GeSn varies significantly with Sn composition, strain state, underneath buffer and crystal quality, thick annealed GeSn layers can be used as buffer layers for GeSn-based optoelectronic devices to provide large extent of strain relaxation while maintaining crystal quality upon delicate selection of annealing conditions. An annealing temperature of 500 °C applied to a 500 nm GeSn buffer of nominal 8% Sn was the best fit in our case to provide matched-lattice parameters, strain relaxation and good crystal quality without Sn segregation for higher Sn composition GeSn active layer.

The third part of this chapter develops an in-situ low temperature annealing method for the growth of graded GeSn buffer layers on Ge/Si substrates. A direct transition from spotty patterns symbolising three-dimensional growth mode to streaky reconstruction patterns are found upon low temperature annealing during growth. Surface quality improvement has been confirmed by AFM, where a rms roughness reduction of 1 nm can be achieved. The growth mode revealed by XRD RSM is pseudomorphic and the lattice parameters calculated from XRD agree with the nominal values. MQW structure based on this annealed buffer demonstrates high crystal quality, as characterised by TEM observations at atomic level. Although thin layers of phase segregation can be found at the interfaces between each layer GeSn, this segregation is found to only diffuse downwards without affecting the upper layers, which are thought to be the most significant region for device applications.

Methods developed and investigated in this chapter can find their applications in GeSn-based mid-infrared photodetectors, lasers, two-dimensional localisation investigations, quantum transport studies for quantum information processing.

4.7 References

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Chapter 5.

C-band InAs/InAlGaAs QD Lasers Grown on InP Substrates

5.1 Introduction

5.1.1 Background

Today's data centres together with data networks consume around 5 – 12 % of the global electricity supply and account for around 1 % of the greenhouse gas emissions, with the ever-growing number of internet users and traffic, where the internet traffic has increased 20-fold since 2010 [1]. In the long term, this energy consumption expansion could remain uncertain distressing to society and environment [1-3]. Remarkably, in massive high performance data centres, over 50 % of the power consumption is used in information transmitting instead of processing. Optical interconnect technology provides an ideal solution to addressing the power consumption challenges by introducing photon-based communications into integrated circuits. Moreover, Si photonics applying abundant low-cost Si as the common platform for light generation, modulation and detection is gaining great research and commercial interests and huge global investments for the development of not only photonic communications, but also emerging markets such as face recognition and LiDAR for autonomous vehicles. Therefore, the demand for high performance active optical elements with large bandwidths in the 1.55 μm C-band optical communication

window, including semiconductor lasers, optical amplifiers, mode-locked lasers, modulators, etc. are dramatically rising [4-8].

Semiconductor lasers with self-assembled zero-dimensional nanostructure QDs have attracted considerable attention because of their superior properties, for instance high temperature stability [9], low lasing threshold [10-12], high tolerance to optical feedback and low-chirp operation [13]. Most importantly, the high tolerance of QDs to threading dislocations makes them critical for the integration of semiconductor lasers to Si-based platforms. Recently, highly efficient 1300 nm InAs/GaAs QD lasers epitaxially grown on Si with low lasing threshold have been achieved thanks to the reduced sensitivity of QDs to defects and the enhanced in-plane carrier confinement in the QD laser structures [14]. They are extremely promising for intra-data centre interconnects (<10 km) and on chip core-to-core communications. However, GaAs-based InAs/GaAs QD lasers are technically difficult to meet the wavelength requirements for long-haul optical communication. Compared with InAs/GaAs QD systems typically emitting at wavelengths up to around 1.3 μm [15, 16], InAs QDs grown on InP substrate have a wider range of applications as they can produce a wider and longer wavelength range from 1.4 to 2.5 *μ*m [17-21] for use in sensing and fiber optic telecommunication systems [8, 22]. Especially, the InAs/InP QDs emitting in the lowest optical fibre loss C-band window 1550 nm, where the lowest loss is only around 0.2 dB/km, is preferred for inter-data centre communication (10-80 km), metro or long-haul connections (> 80 km). Additionally, 1550 nm is in an eye-safe wavelength regime where light is strongly absorbed and scarcely reaches the retina, which makes it inherent in advantages to be used in human interface devices, e.g., wearable devices and face recognition and industrial sensors and controls. Its capability of safely emitting higher power and ranging longer distances also show clear attraction for LiDARs used in automotive applications. Except for inherent application advantages, from the aspect of epitaxial integration, InP-based semiconductor lasers can also provide significant benefits. For example, the reduced thermal expansion coefficient mismatch between InP and Si will render the resultant devices less prone to thermal cracks, as well as a relatively low surface recombination velocity.

5.1.2 QD vs QDash

However, despite substantial research and industrial interests, the development of InAs/InP QD lasers is slow compared with the 1.3 μm InAs/GaAs based QD lasers,

and breakthroughs few and far between. The epitaxial growth challenges are inherent in the InAs/InP material system in the following ways: (1) there is decreased lattice mismatch between InP and InAs (3.2%), which means the QDs are theoretically formed with thicker deposition [23] compared to 1.3 μm InAs/GaAs (7.2%) QDs and the growth is substantially different under moderate strain conditions and the QD nucleation is much more complex. (2) The QD growth on InP typically involves quaternary compounds as the energy barrier layer, mainly InAlGaAs and InGaAsP. The anisotropic strain field and surface diffusion of indium atoms or the As/P exchange at the QD/barrier interface of the quaternary complicate the QD growth dynamics. Quantum dashes (QDashes) rather than dot morphology are easily to occur during QD growth [4] due to the mentioned two challenges. The homogeneity of the InAs/InP QDs is therefore inferior to the InAs/GaAs QD system. Besides, as QDashes are elongated in the $[\bar{1}10]$ direction losing one dimension of carrier confinement, the linewidth of PL spectra of QDashes are therefore usually broader, potentially deteriorating the laser performance. A typical room temperature (RT) PL FWHM is about 70 meV and seldom lower than 60 meV [4, 24]. Although the development of InP-based QDash lasers has been reported [25, 26] and electrically-pumped continuous-wave lasing on native substrate [27] and on the more demanding Si substrate [28] has been achieved as well as showing some interesting benefits including the reduced carrier diffusion length suppressing the sidewall surface recombination [27], truly zero-dimension dot morphology QD lasers with high homogeneity are still of prime demand. To date, the lasing threshold of 1550 nm InAs/InP QD lasers remains one and two order of magnitude higher than their 1.3 μm InAs/GaAs counterparts both on native substrate [29, 30] and on Si substrates [22], respectively.

To improve the performance of 1.55 μm InP-based QD lasers, several stringent requirements must be achieved corporately: 1) round dot morphology over QDashes; 2) the RT emission wavelength should be around 1.55 μm; 3) the dot uniformity should be as high as possible to ensure higher laser gain, which can be examined by the FWHM of the RT PL; 4) High QD ensemble quality. This can be confirmed by the strong PL intensity; 5) a high dot density is also desired for higher laser gain. Besides, the thermal degradation of the optical properties is another important characteristic for assessing the QD quality. A quick optical property degradation upon temperature elevation generally indicates a poor electron confinement ability pointing to

uncontrolled QD morphology and crystal defects. Therefore, the criteria for PL measurements are preferred to be fulfilled at RT to guarantee the functionality at low temperatures.

5.1.3 Growth mechanism of QDs

The epitaxial growth of QDs is a non-equilibrium thermal dynamic process and very sensitive to the temperature, growth rate, thickness, etc. It can vary significantly with the growth conditions as well as the inherent properties in the material system such as the lattice mismatch between the epilayer and substrate and the surface energy. To meet the aforementioned criteria, great research efforts have been made. For InAs QDs deposited on InP (001) substrates formed from Stransky-Krastanov (SK) growth mode, because of the non-equivalent InAs nanocrystal facets along [110] and [$1\bar{1}0$] directions originating from the zinc blend crystal structure, the anisotropic surface energy favours the formation of the particular crystal facets, and the elongated QDashes is thus energetically preferred. This surface effect is complemented by the moderate lattice mismatch InAs/InP system, as well as supported by the existence of a very stable (114) A surface, as calculated from density function theory [31]. The A- and B-type surface denote the type of termination atom. In the case of InAs, A-type surface is In-terminated, and B-type is As-terminated. The surface (114) A is also frequently reported experimentally for InAs QD deposited on InP (001) substrates [31-33]. Consequently, at low deposition thicknesses, the InAs QD growth on InP (001) substrate always tends to form elongated structures having (114) A facets parallel to the elongation axis [$1\bar{1}0$] [31]. Higher indices substrate InP (311) B is demonstrated to be helpful for achieving high QD density with small QD size, and improving the uniformity compared with the growth on (001) substrates [34, 35]. However, this type of substrate is not compatible with the standard laser fabrication and photonic integration fabrication line, for which (001) substrates are favoured, restricting its broader applicability [36].

In addition, As_2 flux over As_4 is reported to be beneficial for obtaining round-shape QDs and has now been widely adopted. As As_4 cracks into two As_2 molecules on the epitaxial surface, a direct supply of As_2 will skip this step and leave stable As-terminated atomic steps decreasing the extent of anisotropic migration of indium adatoms along the [$1\bar{1}0$] direction [37]. Besides, elevating V/III ratio in collaboration with As_2 growth mode can largely supress the formation of QDashes and result in an

increase in QD size [37] or height in particular [38, 39], rising the activation energy from ground states to higher energy levels of the QDs and preventing the thermal escape of carriers thus improve the laser performance [39]. However, the optimal V/III ratio is also correlated to deposition thickness, growth temperature, growth rate, etc., and a large overpressure will also lead to the broadening of the PL FWHM, deteriorating the emission efficiency.

Another important growth technique is applying growth interruption just after the QD deposition step, to allow the ripening of the QDs and change the morphology from dashes to QDs [38, 40, 41]. The elongation is observed to reduce with increasing duration of growth interruption, more round-shaped dots with enlarged heights can be obtained. PL red shifts are also reported due to the increased QD dimensions. This technique is therefore an efficient way to tune the emission wavelength of the QDs. Due to the different strain within the material system, the InAs/InP system should be to some extent more kinetically limited than the InAs/GaAs system. Methods such as a high V/III ratio, a large growth rate or a fast and more uniform nucleation [38, 42] are documented to be effective to suppress the anisotropic QD morphology. Under these growth parameter optimisations, a narrow PL FWHM of 17 meV measured at 10 K has been reported in the literature [38], high characteristic temperature T_0 lasers working up to 195 °C and 120 °C under pulsed and continuous excitation, respectively, have been achieved based on these morphology-improved QDs [43]. However, the PL is measured under very low excitation power density of 0.2 A/cm^2, and it is difficult to compare the obtained linewidth with the literature as there is possibility that the QD ensemble is only partially excited.

A further technique to control the QD morphology dispersion widely used for InAs/GaAs QDs is the indium-flush (In-flush) technology [44]. In this method, a layer of the thickness of average dot height of GaAs is used to partially cap the QDs and allow the exposure of the large dots, after the deposition of a layer of self-assembled QDs. Then the substrate temperature will be elevated to remove any trace of indium on the epi-surface so that the subsequent QD layer growth is unaffected. For InAs/InP system, the In-flush technique evolutes into two variants, which are also called ‘double-cap’ method. The differences lie in the ‘flush’ step where As/P exchange is involved and whether temperature elevation is needed depends on the use of phosphorus or arsenic supply. The As/P exchange is first observed during the InP capping layer growth of QDs, which significantly changes the island size [34]. Later,

in order to intentionally tune the emission wavelength from 1.77 μm to 1.55 μm, annealing under P flux is applied, the resultant PL blue shift shows clear dependence of annealing duration. Therefore, the same group managed to use this method to both control the emission wavelength as well as the QD height dispersion by applying the two-step capping process [21]. When the first InP capping layer is deposited, it will grow in the spacings between the QDs as the InAs island top undergoes strain relaxation and is not energetically favourable for adatoms to attach to [21]. After that a growth interruption under P overpressure is presented during which the exposed InAs will form InP due to strain mismatch-induced As/P exchange and migrates off to the InP first capping layer. This mass transport process won't terminate until unprotected InAs reach the same thickness with the first capping layer [45]. A PL linewidth reduction from 70 meV to 50 meV [21] and a broad area laser with a low lasing threshold of 170 A/cm^2 [46] are achieved by different research groups on (311)B substrates using this growth technique.

The other double cap approach is the same rationale with the In-flush technique used in InAs/GaAs material system with elevated temperature after the first partial capping layer. Here the first capping layer does not need to be InP consequently, which can be lattice matched InAlGaAs or InGaAsP, etc. However, although double-cap method is applied on InP (001) substrates, the PL linewidth remains above 70 meV at room temperature [47, 48], when small substrate offcut angles exist it can be lower to around 63 meV [49, 50]. As a result, further growth optimisation is required for the development of the high performance InP-based 1.55 μm lasers.

5.2 InAs/InAlGaAs/InP QDs Growth Optimisation

5.2.1 Pre-growth Substrate Treatments and Self-assembled QDs Growth

The substrates used in this study is n-type InP (001) (± 0.5°). Before the epitaxial growth, they were first degassed at 400 °C for one hour in the preparation chamber. Then, they were heated to ~ 500 °C and stayed for one minute to remove any surface oxides. Ideally, P overpressure should be used to protect the surface, in our case As_2 flux was used. Phosphorous desorption from the surface under As_2 protection can be observed from microscope, which can be improved by P overpressure protection. During the deoxidation process, a RHEED pattern shift from (2×2) to (4×2) reconstruction can be observed symbolising an improved surface morphology and the

start of the deoxidation. Holding at high temperature for too long will destroy the substrate surface, which can be revealed by the dimmer RHEED intensity and the disappearance of the 4× patterns. The growth structure of the calibration samples is shown below in Figure 5-1. It consists of 500 nm lattice-matched $In_{0.524}Al_{0.476}As$, InAs QDs sandwiched by 100 nm $In_{0.528}Al_{0.234}Ga_{0.238}As$ barrier layers, another 200 nm $In_{0.524}Al_{0.476}As$ and 100 nm $In_{0.528}Al_{0.234}Ga_{0.238}As$ for the subsequent growth of uncapped surface QDs for AFM measurements. The InAlAs and InAlGaAs layers were grown at 510 °C and 500 °C, respectively.

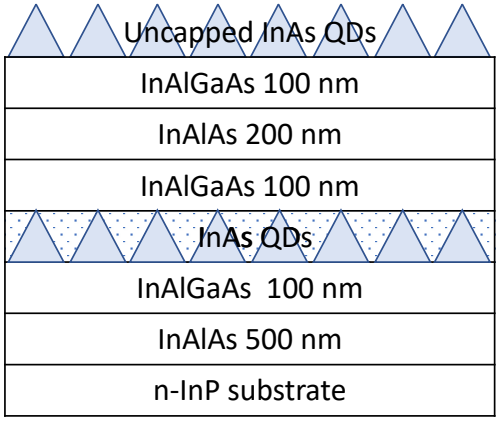

Figure 5-1 Schematic growth structure of InAs/InAlGaAs QDs grown on InP substrate for calibration.

The growth of InAs QDs on InAlGaAs lattice-matched to InP follows the SK growth mode. In this study, the InAs QD layer was grown under As_2 mode. The QD growth temperature, V/III ratio and deposition thickness were varied for the investigation of their effects on the QD quality.

5.2.2 Effects of Deposition Thickness

In this section, the effects of deposition thickness on QD morphology and PL emission are investigated in detail. In general, the deposition thickness affects not only the size and distribution of QDs, but also the resultant optical properties. In the case of InAs/InP material system, it also has a significant impact on the QD ensemble morphology due to the reduced lattice mismatch boosted anisotropic surface energy. In principle, higher deposition thickness will result in larger QD size and longer emission wavelength. On the other hand, smaller QDs have higher emission energy thanks to the increased quantum confinement energy. However, too thick QD layer will result in an increase in the density of defective large QDs, which act as non-radiative recombination centres depleting the carriers for light emission.

To change the nominal deposition thickness of InAs, changing the deposition duration or the In growth rate are the two options. The effect of varying the deposition duration is straightforward but more contamination-related point defects may be involved during the elongated growth duration. The other option is to increase the In growth rate, which is more favourable in the growth that requires non-equilibrium conditions. In the InAs/InP QD growth, more limited kinetics is preferred to suppress the adatom migration following the anisotropic surface strain field, therefore a high In growth rate of 0.42 ML/s is used in this study, compared with the typical InAs/GaAs QD growth rates of around 0.15 ML/s.

As a starting point, a substrate temperature of 485 °C and a V/III ratio of 18 were used for the QD growth. The growth sequence is that after the growth of InAlGaAs barrier, a 15-second growth interruption was inserted to change the substrate temperature from 500 °C to 485 °C and As pressure for QD growth. Then InAs were deposited with different thicknesses of 6.4, 5.5, 4.5, 4, 3.5, 3 ML, respectively. After that a growth interruption of 10 seconds was applied to facilitate the QD formation. Following this is the direct deposition of InAlGaAs layer and at the same time the substrate temperature was increased to 500 °C with a temperature ramp of 10 °C/min. The surface QDs growth procedure is the same with the buried QD layer. After the growth of the surface dots, the substrate was immediately cooled down under As protection.

The plane-view and 3D 1 μm ×1 μm AFM results are shown in Figure 5-2 (a – f). It can be clearly seen that there are a mix of QDs and QDashes present on the surface and more QDashes over QDs for smaller deposition thickness. A closer investigation reveals that for 6.4 ML InAs deposition the QDs are packed closely with QDashes fill in their spacings. The QD and QDash densities are $\sim 4.3 \times 10^{10}/cm^2$ and $5\times 10^{9}/cm^2$, respectively. For a deposition thickness of 5.5 ML, almost no QDashes are observed. The QDs present well-defined round shape despite some size fluctuations are found. A high density of $\sim 4.4 \times 10^{10}/cm^2$ is obtained while that of QDash is only around $8 \times 10^{8}/cm^2$. A further decrease of thickness result in the presence of more QDashes than QDs and a reduction of QD density.

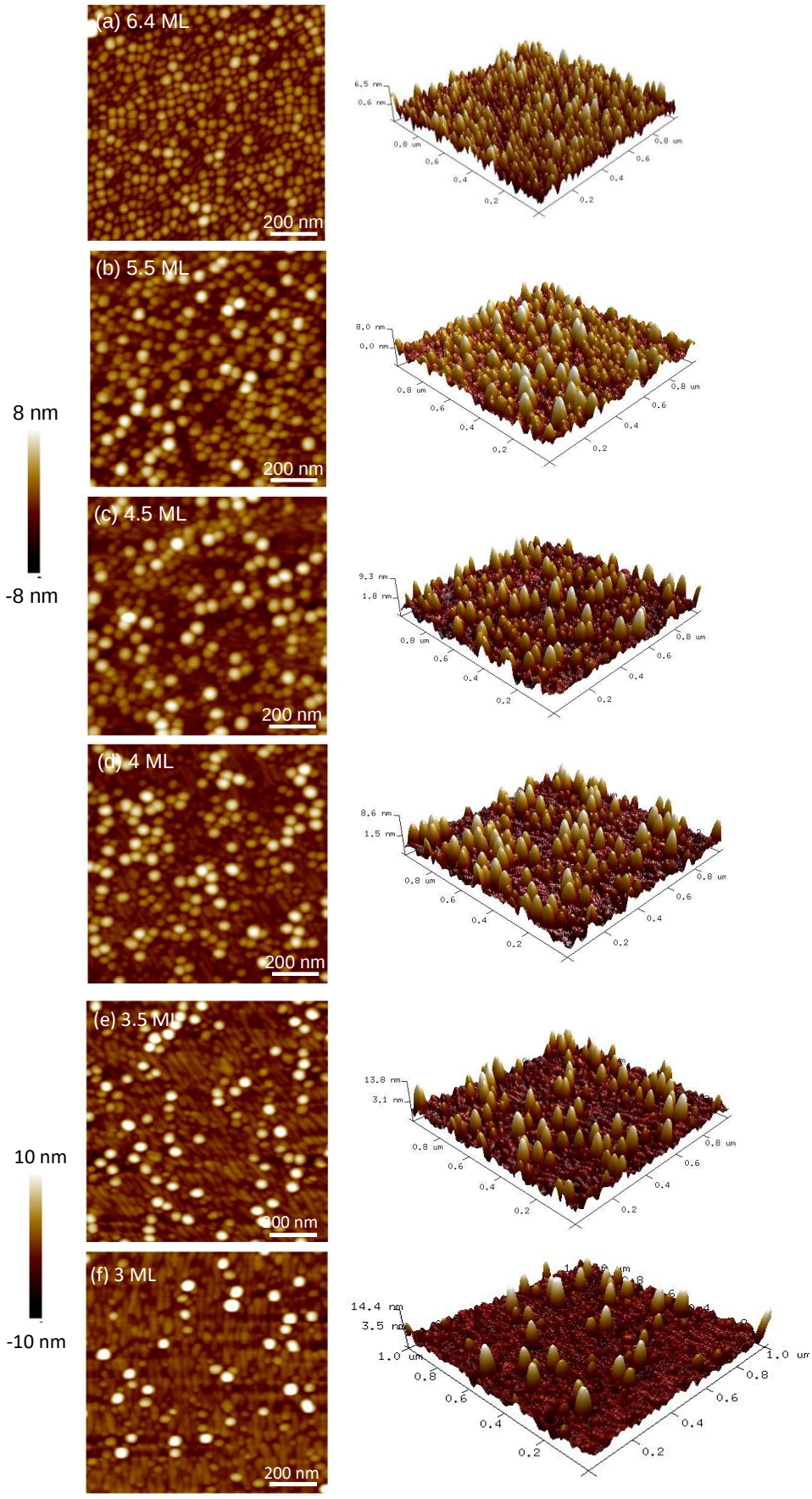

Figure 5-2 1 μm ×1 μm AFM images showing the QD morphology of samples with deposition thicknesses of (a) 6.4 ML (b) 5.5 ML (c) 4.5 ML (d) 4 ML (e) 3.5 ML (f) 3 ML.

The QD and QDash densities are compared and shown in Figure 5-3 (a). As mentioned earlier, the zinc-blend InAs nanostructure has two non-equivalent energy facets along [110] and [1$\bar{1}$0], which drives the formation of the elongated structures. This mechanism is especially favoured by the lower-mismatch InAs/InP system. QD structure is reported to occur after 3 ML of InAs deposition, before which only ordered QDashes were observed [31]. At higher deposition thicknesses, the elastic relaxation is to some extent limited by the further growth of the elongated structure, the formation of more isotropic QD structures is therefore more efficient in relaxing the strain. Besides, from the 3D AFM images of the samples, it can be seen that for larger deposition thickness, the QDs are shorter. This phenomenon is also reported by Ponchet *et al* that by increasing the deposition thickness of InAs from 1.5 ML to above 2.5 ML, the QD volume is five times smaller [51]. This phenomenon indicates that the QD size is not only dominated by the surface transport, but that the QD nucleation also plays an important role. It is known that coherent islands are generated from the elastic relaxation through free surface creation and substrate distortion. As the deposition thickness increasing, the island coverage will rise and the strain relaxation through the substrate is limited because the adjacent islands will start to interact. The large islands thus transform into smaller islands as the case shown in this study.

The PL measurements are also performed on the samples with variable deposition thickness, as shown in Figure 5-3 (b). The PL emission wavelength and FWHM are also summarised as a function of deposition thickness in Figure 5-3 (c) and (d), respectively. As expected, the emission wavelength increases with increased deposition thickness due to the reduced confinement energy. Remarkably, the PL intensity of the 3.5 ML deposition is the highest, whereas from 4 ML onwards, the PL intensity decreases slightly with increased deposition thickness. PL intensity degradation can be a clue for the creation of non-radiative recombination centres possibly caused by partial strain relaxation [26, 42]. The obtained PL FWHM is in the range of 85 – 100 meV, indicating non-uniformity of the QD ensembles. In addition, the shape of the PL linewidth Figure 5-3 (d) trend is particularly similar with the QDash density Figure 5-3 (a), presumably suggesting that the existence of QDashes broadens the PL linewidth. In summary, the QD morphology is well defined at higher deposition thicknesses and the PL emission wavelength increases linearly with the deposition thickness. The uniformity of the QDs still needs to be improved. Considering the QD morphology, density and PL linewidth, at deposition temperature

of 485 °C, 5.5 ML is selected as the optimum deposition thickness for further improvements.

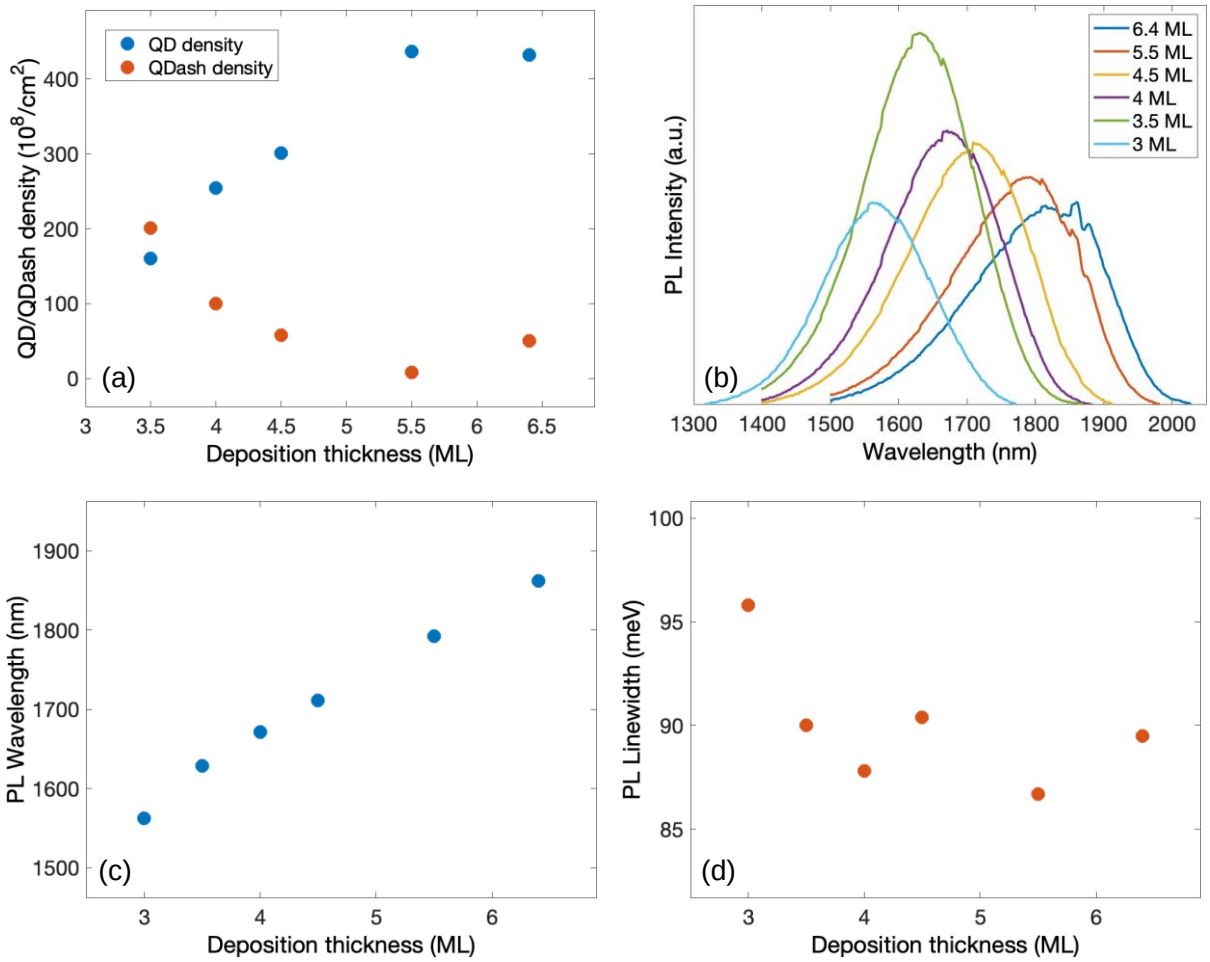

Figure 5-3 (a) QD and QDash densities of samples as a function of deposition thickness; (b) A comparison of PL intensity for samples with variable deposition thickness; (c) PL peak emission wavelength and (d) PL FWHM of samples as a function of different deposition thickness.

5.2.3 Effects of Deposition Temperature

In this section, the effects of deposition temperature on QDs are studied. In general, lower QD deposition temperature results in a higher QD density thanks to the suppressed adatom migration on the surface. At higher temperatures, when the adatoms have more energy to migrate on the surface, they tend to join the already nucleated islands rather than form a new one. For smaller dots formed on the surface, they also have a tendency to incorporate with adjacent large dots, which is called a coalescence process. Consequently, it turns out that below a certain critical deposition thickness, lower deposition temperature will be helpful for increasing the QD density as well as promote uniformity, while above such critical thickness, a lot of dots have already formed, higher deposition temperature becomes beneficial for controlling the QD uniformity. Too high temperature will result in In re-evaporation and a reduction of

sticking coefficient lowering the QD density. However, on the other hand, high temperature is beneficial for PL emission as low-temperature-induced point defects can be removed. The QD growth is a far-from-equilibrium process, therefore understanding the growth dynamics is a necessity for the optimisation of the QD density, morphology, and emission properties as a unity.

For the optimisation of InAs/InP QDs in this section, two sets of samples with deposition thicknesses of 4.5 ML and 5.5 ML were first grown at different temperatures. Their morphological and optical properties are shown in Figure 5-4 and 5-5, respectively. For the 4.5 ML InAs QD deposition (Figure 5-4 (a)), a mix of dashes and dots is presented for the lower deposition temperature of 475 °C. For the deposition temperature of 485 °C (Figure 5-4 (b)), the majority of the nanostructures obtained is QDs. However, further increasing the growth temperature to 495 °C (Figure 5-4 (c)), results in high density of QDashes, and the number of QDs is even lower than that deposited at 475 °C. The QD density increase at 485 °C compared to 475 °C is anomalous as usually higher QD density is expected at lower deposition temperature. From the AFM results in Figure 5-4 (a – c), it can be seen that 475 °C results in surface undulations while the samples deposited at 485 °C and 495 °C appear flat. This surface undulation may provide a clue for the low QD density. At low temperature, the In adatoms will have insufficient migration energy to uniformly cover the whole surface so that they may accumulate at some areas causing the nucleation of large islands, whereas 485 °C is proper for the enhanced migration. In addition, the presence of high density of QDashes at lower deposition temperature supports the hypothesis that elongated structures are the most efficient way of relaxing the mismatch strain in the InAs/InP material system because any migration process that requires excess energy is suppressed. Although whether the QDs are formed above the QDashes or transformed from the QDashes remains unclear, the author tends to believe the former because of the following. As can be seen from Figure 5-4 (c), at elevated deposition temperature of 495 °C, the QDashes are still present with a few QDs. The reduced dot density can be explained by the increased re-evaporation of the QDs and coalescence process. The QDashes are still present and more ripened and remain ordered, probably providing a hint that they are formed at an earlier stage and are stable. The PL linewidths of the three samples are all higher than 90 meV, and the emission wavelength are far beyond 1550 nm, as shown in Figure 5-4 (d) and (e), respectively, which means the dot ensemble are highly dispersive and needs further improvements.

In addition, the PL intensity of the samples grown at different temperatures are shown in Figure 5-4 (f), and it is observed that although the QD density of the sample grown at 485 °C is much higher than the rest, its PL intensity is the lowest, indicating the existence of defective QDs deteriorating the optical properties.

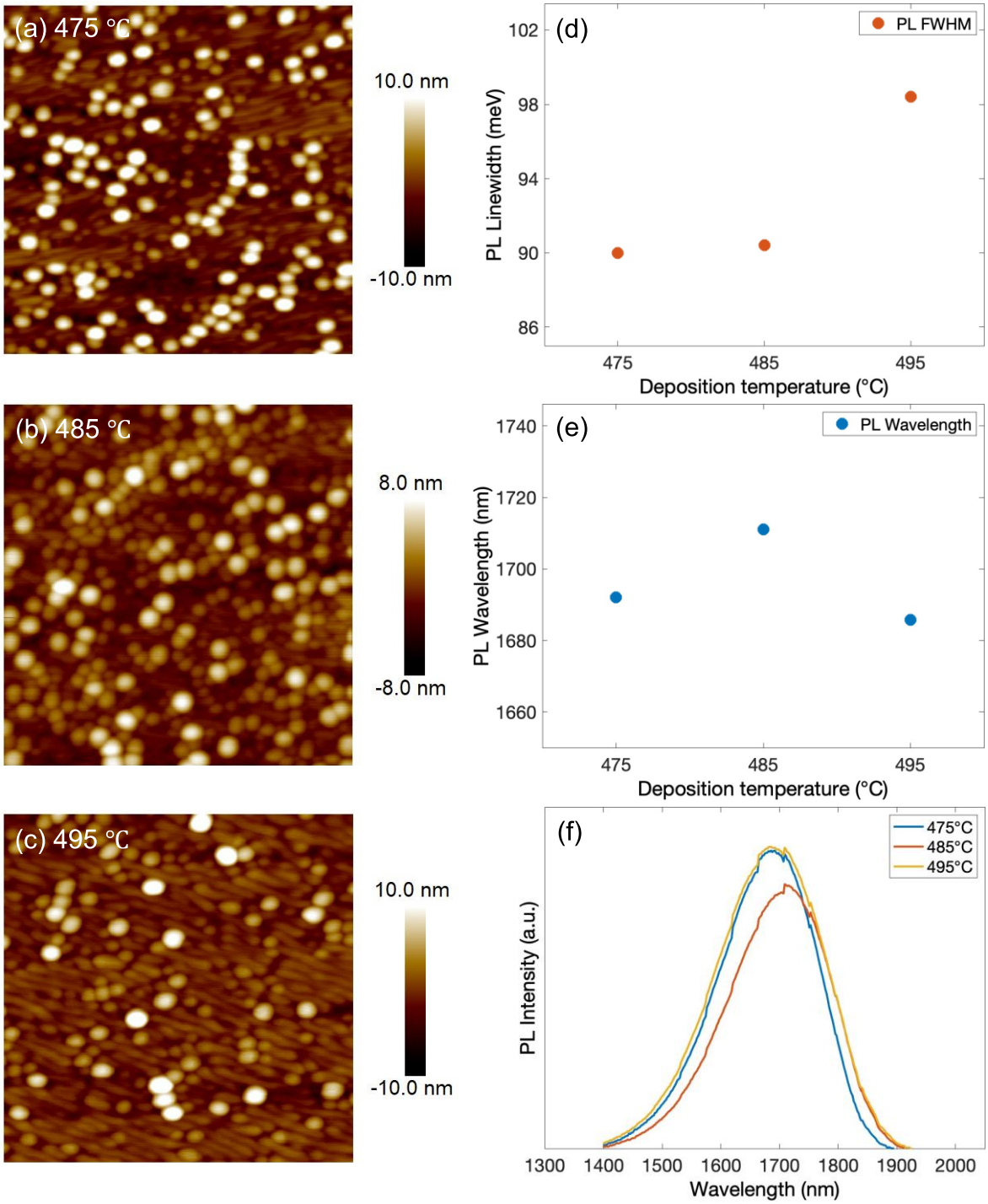

Figure 5-4 (a – c) AFM images of 4.5 ML InAs QDs grown at 475 °C, 485 °C and 495 °C, respectively; (d) PL linewidth (e) PL emission wavelength and (f) PL intensities of 4.5 ML QD samples grown at various temperatures.

Different growth temperatures of 475 °C and 485 °C (as from 4.5 ML QD sample, the growth temperature of 495 °C deteriorated QD density, which might be a result of

excessive In evaporation) were also performed for 5.5 ML InAs QD growth to compare the effects of deposition temperature at different QD thickness. The AFM results are shown in Figure 5-5 (a) and (b). At this slightly higher deposition thickness, both deposition temperatures result in a majority of dot morphology. However, the sample deposited at 475 °C shows a lot of large dots, which are the white dots in Figure 5-5 (a), and the surface is not as flat as the sample deposited 485 °C. Besides, the sample deposited at 485 °C has a much higher dot density (436/μm^2) than that deposited at 475 °C (286/μm^2), as summarised in Figure 5-5 (c). However, the PL FWHM is also higher for the sample deposited at 485 °C compared to 475 °C, which is 86.7 meV and 80.9 meV, respectively. This indicates that the higher dot density is accompanied by a higher dot size dispersion. The PL intensity with wavelength of the samples grown at different temperatures is also shown in Figure 5-5 (d). The PL intensities are identical and the emission wavelength redshifts from 1759.4 nm to 1792.4 nm with elevated deposition temperature.

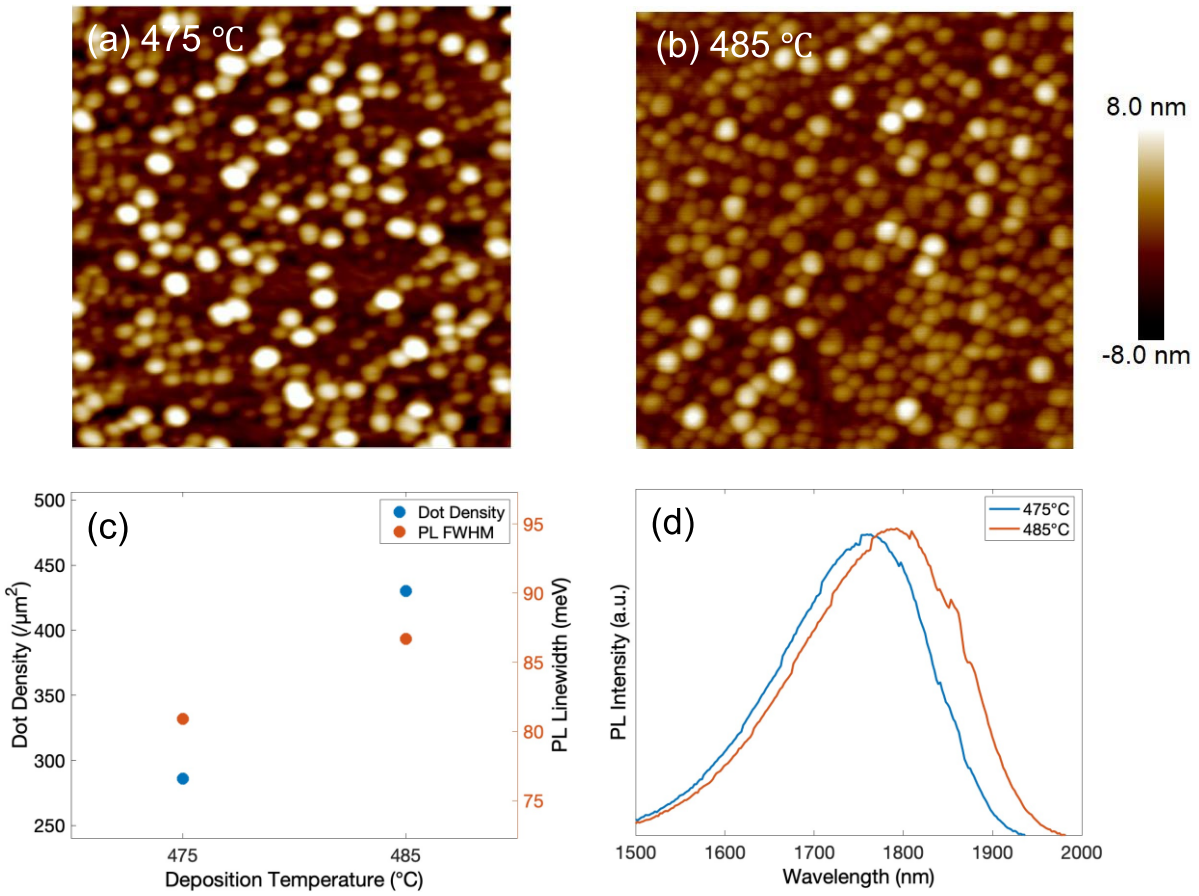

Figure 5-5 (a – b) AFM images of 5.5 ML InAs QDs grown at 475 °C, 485 °C, respectively; (c) Dot density and PL linewidth and (d) PL intensities of 5.5 ML QD samples grown at various temperatures.

By comparing the results of these two sets of samples with different growth temperatures, it can be concluded that the achievement of QD morphology over

QDash is closely related to both InAs deposition thickness and temperature. The effects of deposition temperature will build up on the effects of deposition thickness in the following way. As discussed previously, when the deposition thickness is low, QDashes are first formed as an efficient way of strain relaxation. With the increase in the deposition thickness, further growth of the elongated structures will be limited due to the interaction of the adjacent nanostructures and the supressed relaxation through the substrate. Then dot will start to nucleate to further relax the strain. Based on this 'QDash-like' wetting layer, low-temperature-induced low In atom mobility is likely to cause non-uniform and increased nucleation of the large QDs whereas the uniform QD nucleation is suppressed. This results in the appearance of the mix of QDs and QDashes for the sample deposited at 475 °C with 4.5 ML InAs and the situation was improved when the substrate temperature was elevated to 485 °C. Too high growth temperature stimulates QD coalescence and QD re-evaporation that reduce the QD density therefore for the sample grown at 495 °C high density of QDashes come back. As for the 5.5 ML deposition samples, the same reasons cause the lower QD density for the 475 °C sample.

However, if we compare the PL intensities of samples with a deposition thickness of 5.5 ML InAs grown at 475 °C and 485 °C, it can be seen from Figure 5-5 (d) that although the sample grown at 485 °C has much higher QD density than that at 475 °C, they present almost the same PL intensity. Consequently, another set of samples with thicker InAs were deposited at 475 °C to obtain higher dot density and potentially, more intensive PL emission. A comparison of the AFM and PL results of 4.5 ML, 5.5 ML and 6.4 ML InAs deposited at 475 °C is shown in Figure 5-6. As expected, that more QDs present on the surface with increasing deposition amount intuitively from the AFM images in Figure 5-6 (a – c) and confirmed by the densities from 184/μm^2 to 340/μm^2, as shown in Figure 5-6 (d). The PL intensities compared in Figure 5-6 (e) demonstrate a decreasing trend with increasing thickness, which may be related to the large quantity of defective dots. The emission wavelength increase with increasing deposition thickness and the PL linewidth shows an almost linear decrease from 90 meV to 76.6 meV with increasing deposition thickness, which can be observed from Figure 5-6 (f) and (g), respectively. These PL results infer that at the deposition temperature of 475 °C, the increase of deposition thickness will result in the PL intensity degradation, but more dots are obtained with better uniformity. The PL intensity degradation with increasing thickness is normally related to increased

number of defects present in the QDs. While the improved QD uniformity might be results of the ripening of the dots and more transformation of the dashes to dots during strain relaxation. With these results in mind, another attempt of 6.4 ML InAs grown at 465 °C was carried out and compared with the best results so far aiming at even lower PL FWHM and high dot density.

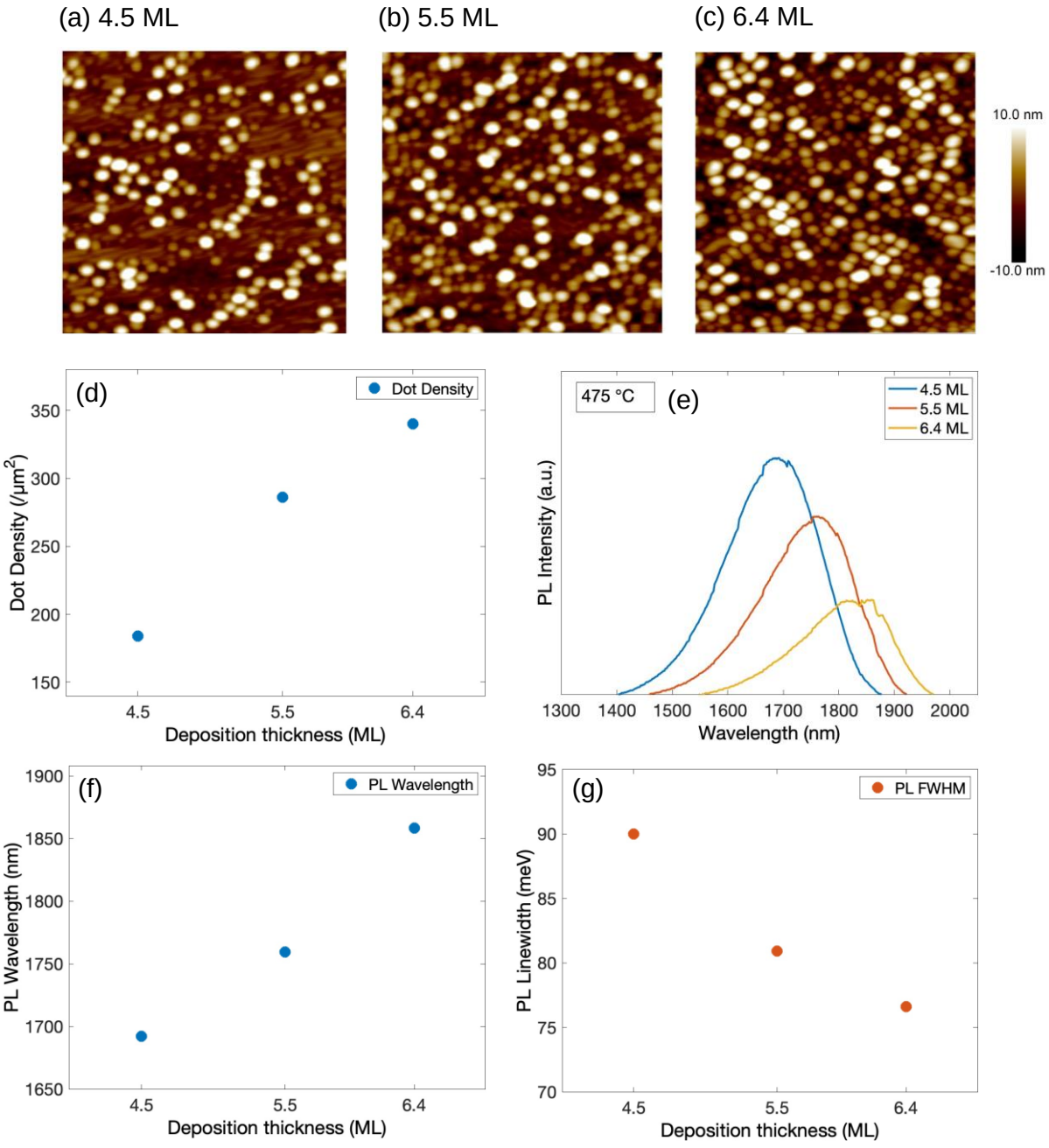

Figure 5-6 A comparison of the AFM results (a – c), dot density (d), PL intensity (e), PL emission wavelength (f) and PL FWHM (g) of 4. 5 ML, 5.5 ML and 6.4 ML InAs deposited at 475 °C.

The QD morphology and PL results of samples of 5.5 ML InAs grown at 485 °C, 6.4 ML InAs grown at 465 °C, 475 °C and 485 °C are compared in Figure 5-7 to find the optimal deposition thickness and temperature for further growth optimisation. All the

four samples show a high QD density in the range of 300 – 450/μm^2. The sample of 6.4 ML InAs deposited at 485 °C has a QDash density of ~ 50/μm^2, the sample of 5.5 ML InAs deposited at 485 °C demonstrates a negligible QDash density of ~ 8/μm^2. For samples of 6.4 ML deposited at 475 and 465 °C, the surface height undulation is large so that counting the number of QDashes becomes unreliable. As for the QD density, the highest is still the sample of 5.5 ML InAs deposited at 485 °C, which is 436/μm^2. The PL intensities are shown in Figure 5-7 (e), the sample of 5.5 ML InAs deposited at 485 ° also shows the highest intensity, while for the samples with 6.4 ML InAs, the PL intensities decrease with decreasing growth temperature. The lowest PL intensity is only a quarter of that of the highest sample deposited at 485 °C. This reduction in PL intensity with decreasing growth temperature is closely related to the point defects introduced at low growth temperature. Moreover, the low-In-mobility-induced non-uniform nucleation, which enhances the formation of defective large dots may also play a role. The emission wavelength for the 5.5 ML deposition is the closest to 1.55 μm, at 1792 nm. The PL FWHM for the four samples is summarised in Figure 5-7 (f), showing that the sample grown at 465 °C has the lowest linewidth, i.e., the emissive components have the best uniformity. This result can be explained by two reasons: one being the fact that with the same PL energy broadening, longer emission wavelength will present a lower FWHM; the other reason is that the defective large dots are not emissive, the sample grown at 485 °C has a larger number of emissive dots with a slight size variation compared with the sample grown at 465 °C, which presents many defective dots with the remaining dots possessing a better uniformity. From the perspective of dot density, emission wavelength and crystal quality, the sample of 5.5 ML InAs grown at 485 °C is selected as an optimal condition for additional optimisation, because the size variation can be manipulated further by the In-flush technique.

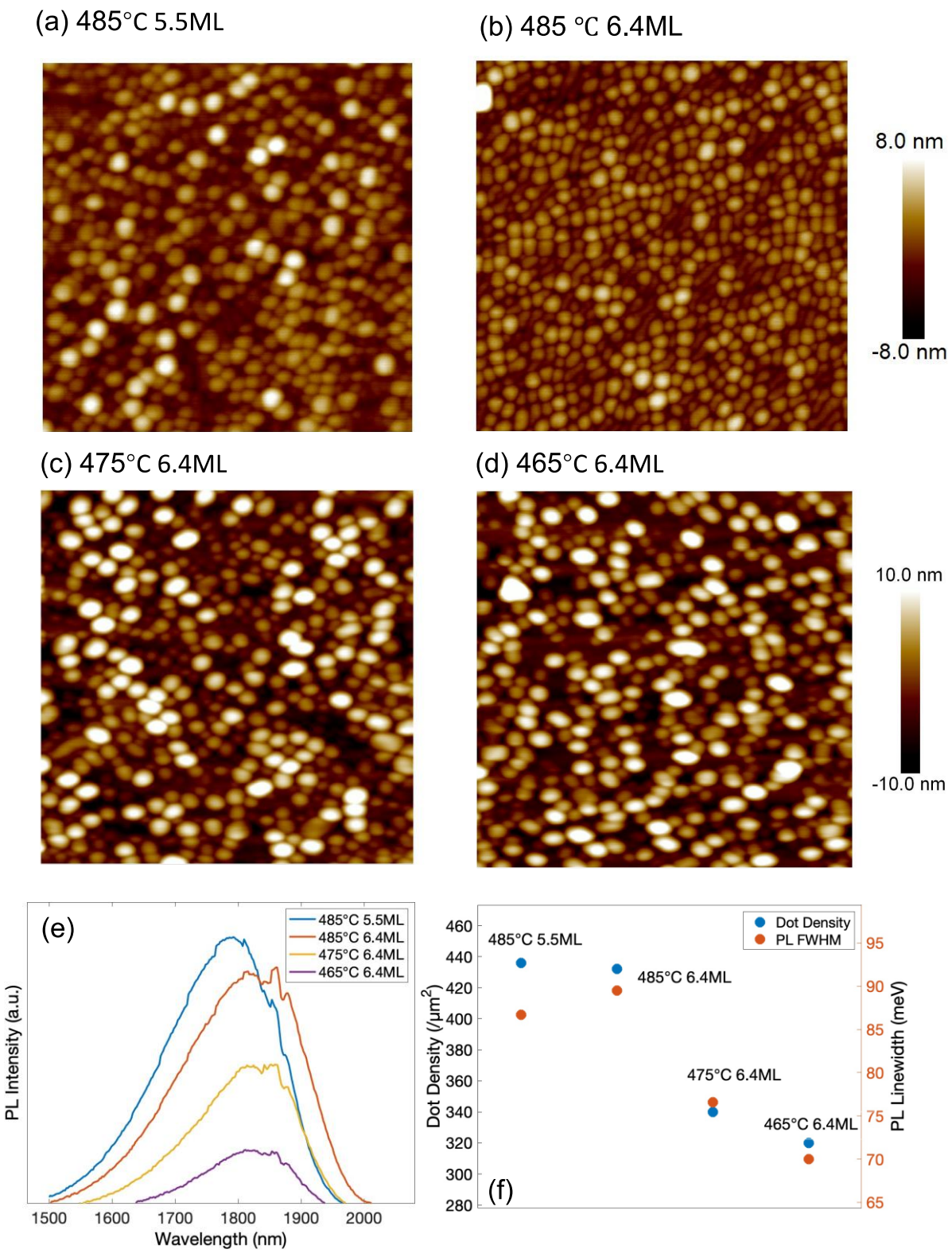

Figure 5-7 (a –d) AFM images of samples of 5.5 ML InAs grown at 485 °C, 6.4 ML InAs grown at 485 °C, 475 °C and 465 °C, respectively; (e) A comparison of the PL intensities and (f) dot density and PL Linewidth of the four samples.

5.2.4 In-flush Technique

In this section, the effects of In-flush technique on QD size uniformity control are discussed and optimal In-flush conditions are selected for the multi-stack QD growth. For this purpose, 5.5 ML InAs grown at 485 °C was used for all the samples in this study. The schematic growth structure is shown in Figure 5-8, which is similar with the single dot layer growth except the growth of the InAlGaAs (and GaAs) capping layer. After the active region QD growth, a first capping layer (FCL), which is either a latticed-matched InAlGaAs layer or a combination of InAlGaAs and GaAs layer on the top to control the mass transfer process as well as manipulating the emission wavelength, with a thickness x was deposited at 485 °C to partially cap the QDs, exposing the large undesirable dots. Then the substrate temperature will be elevated to a temperature y to evaporate the exposed excess In from the QDs. Different FCLs and In-flush temperatures were tested to find out their effects on the PL linewidth improvement. The details and results are summarised in Table 5-1. First, a combination of lattice-matched InAlGaAs and GaAs was used as the FCL to investigate the effects of FCL thickness to PL FWHM reduction. 4.4 nm, 2.4 nm, and 1.4 nm InAlGaAs with 0.6 nm GaAs, respectively, were grown as the FCL at a substrate temperature of 485 °C after the QD growth and interruption, then the substrate temperature was elevated to 520 °C with a ramp rate of 30 °C/min under excessive As_2 pressure for one minute. To find the optimal In-flush condition, another two samples with the FCL thickness of 1.4 nm InAlGaAs with 0.6 nm GaAs were grown and the substrate temperatures were increased to 525 °C and 530 °C, respectively, for comparison. The PL emission properties of these samples are shown in Figure 5-9. At the same In-flush temperature of 520 °C, the emission wavelength decreases from 1780.4 nm for the 5 nm FCL to 1603.8 nm for 2 nm FCL, which is as expected because smaller dots are remaining. However, the PL FWHM shows improvement inconsistency. For the 3 nm FCL sample, the PL linewidth decreases to 54.7 meV but the PL linewidth of the 2 nm FCL sample is 60 meV. This indicates that it is highly likely that the substrate temperature 520 °C is not sufficient to evaporate completely the exposed In from the QD, therefore, the dot uniformity improvement is random. This hypothesis is confirmed by the samples with 2 nm FCL annealed at higher temperatures of 525 °C and 530 °C. With the same 2 nm FCL, the PL emission wavelengths of samples annealed at 525 °C and 530 °C keep blue shifting to 1423.5 nm and 1369.1 nm, respectively, indicating 520 °C is insufficient for In-flush purposes. There is a PL FWHM improvement of the sample

annealed at 525 °C compared to 520 °C, which decreases from 60 meV to 48.5 meV. However, for the sample annealed at 530 °C, it increases to 61.5 meV. There are two possible reasons for this PL linewidth increase: one is that 2 nm is too thin so that the QDs are almost completely gone, which can be supported by the significantly reduced PL intensity of the latter two samples; the other reason might be that 530 °C is too high so that concave-top-shaped QDs are formed increasing the size inhomogeneity. In addition, the PL emission wavelengths of these two samples are too short for the C-band communication.

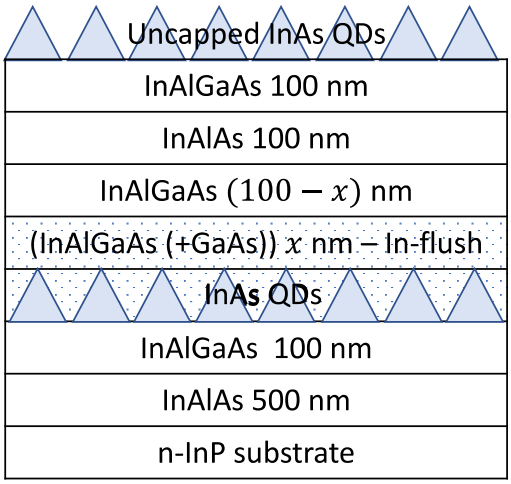

Figure 5-8 Schematic growth structure of samples for In-flush investigations.

Table 5-1 In-flush Conditions and results summary

No.	FCL Thickness (nm)	$T_{In\text{-}flush}$ (°C)	λ_{PL} (nm)	PL FWHM (meV)
1	4.4 InAlGaAs + 0.6 GaAs	520	1780.4	67.2
2	2.4 InAlGaAs + 0.6 GaAs	520	1753.1	54.7
3	1.4 InAlGaAs + 0.6 GaAs	520	1603.8	60
4	1.4 InAlGaAs + 0.6 GaAs	525	1423.5	48.5
5	1.4 InAlGaAs + 0.6 GaAs	530	1369.1	61.5
6	3.4 InAlGaAs + 0.6 GaAs	530	1556.2	58.1
7	4 InAlGaAs	530	1587.4	55.7
8	4 InAlGaAs	540	1522	47.9
9	4 InAlGaAs	550	1477.8	50.3

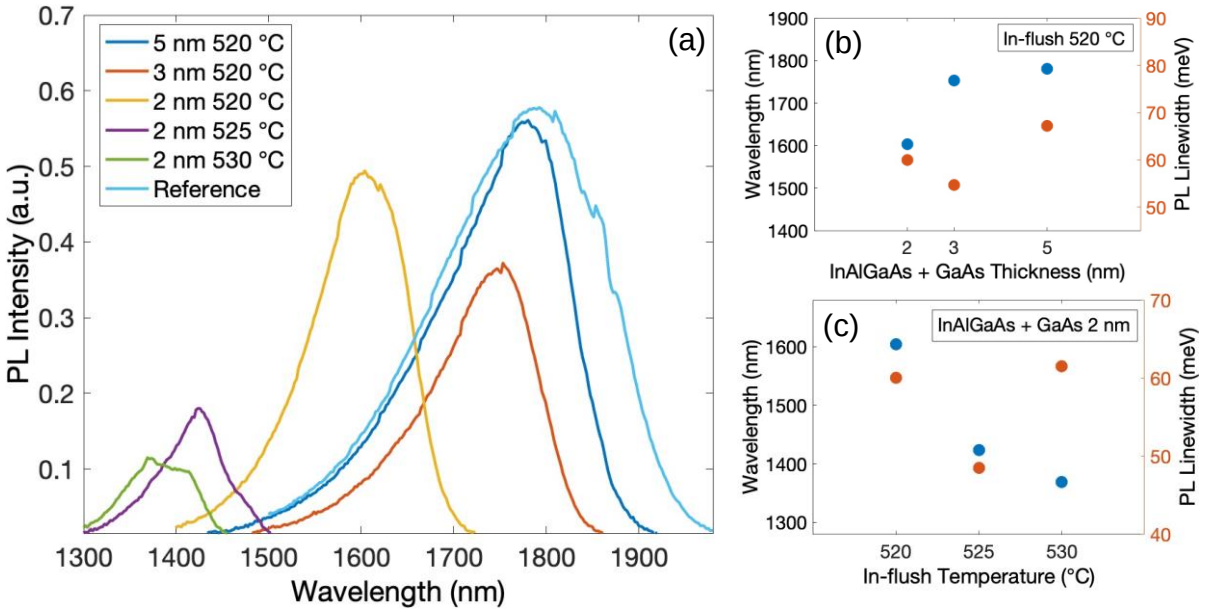

Figure 5-9. (a) The PL intensities applying the In-flush technique of different thicknesses of the first InAlGaAs and GaAs capping layer and at different 'flush' temperatures; (b) PL emission wavelength and FWHM comparison of samples applying the In-flush at 520 °C with different FCL thickness and (c) PL emission wavelength and FWHM comparison of samples applying the In-flush with InAlGaAs and GaAs FCL 2 nm at different temperatures.

For the above-mentioned reasons, thicker FCL of a total thickness of 4 nm were grown and subsequently annealed at 530 °C. The PL emission wavelength is tuned to 1556.2 nm, which is highly desirable and the FWHM is improved to 58.1 meV. To further improve the effects of In-flush technique, InAlGaAs-only FCLs were used to compare with the combination of InAlGaAs and GaAs. 4 nm InAlGaAs lattice-matched to InP FCLs were grown at 485 °C, then the substrates were elevated to 530 °C, 540 °C and 550 °C for comparison. The PL emission results can be seen in Figure 5-10. The application of InAlGaAs-only FCL demonstrates significant advantages over the combination FCL in both PL intensity and PL FWHM for samples annealed at 530 °C. The PL intensity is improved by 140 % for the InAlGaAs-only FCL sample, and the PL FWHM is also improved to 55.7 meV. Further increasing the In-flush temperature to 540 °C results in the lowest PL FWHM so far among all the samples, which is 47.9 meV with an emission wavelength of 1522 nm. An In-flush temperature of 550 °C starts to degrade the PL intensity as well as the linewidth, and emission wavelength blueshifts to 1477.8 nm, which is far from the C-band window.

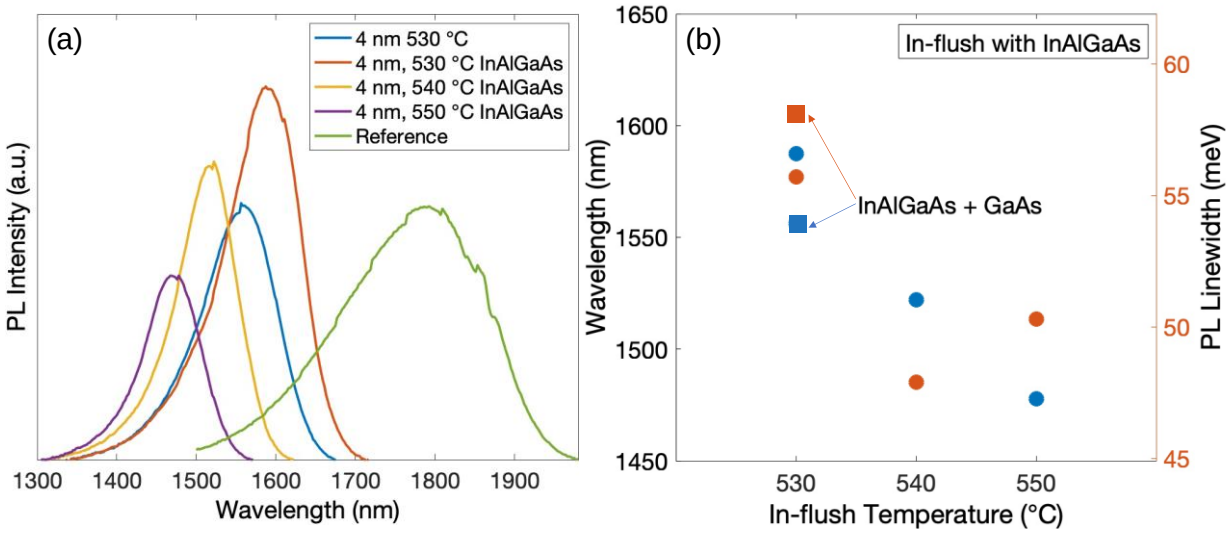

Figure 5-10. A comparison of (a) PL intensity and (b) PL emission wavelength and linewidth for samples with the combination of InAlGaAs and GaAs and InAlGaAs-only FCLs annealed at different tempratures.

In summary, among different FCL materials, thickness and In-flush temperatures, the 4 nm InAlGaAs FCL with an In-flush temperature of 540 °C performs the best effects on QD homogeneity improvement, resulting in a PL linewidth reduction from 86.7 meV of the reference sample without In-flush technique to 47.9 meV, while manipulating the emission wavelength from 1792.4 nm to 1522 nm and the emission intensity is also improved. The successful application of the In-flush technique to the InAs/InP QD growth prove its potential for the achievement of high-performance C-band QD-based optoelectronic devices.

5.2.5 Multi-stack InAs/InP QD Growth

In this section, the growth of multi-stack InAs/InAlGaAs/InP QDs is investigated for laser applications. The growth of QDs has been of great research interests for the development of high-performance QD lasers exhibiting low threshold current density, temperature stability, low chirp, and high modulation bandwidth. However, the low volume of the QDs leads to the excited-state lasing at high temperatures or high thresholds. An efficient way to increase the gain volume is by growing a multi-stacked QD structure. In self-assembled growth regime, since QD formation is manipulated by strain effects, strain accumulation over the layers limits the number of defect-free stacked layers to be grown. In-flush technique is helpful in relieving the strain build-up, therefore suppressing QD size variation during the multi-layer growth. On the other hand, a layer of material lattice-matched to InP is usually used between the QD layers to mediate the strain introduced by the growth of InAs and create a flat surface for subsequent QD layer growth, which is named a ‘spacer layer’. The thickness of the

spacer layer is known to play a critical role in the upper QD layers. Thicker spacer layers have been demonstrated to reduce the upper QD layer density because of size filtering effects whereas thinner spacer layers allow the achievement of constant QD density per layer thanks to the strain mediated vertical alignment of QDs [52]. Figure 5-11 depicts the growth structure of the five-layer QDs. The effects of spacer layer thickness are investigated for five-layer QD samples with 20 nm, 30 nm, and 40 nm, respectively.

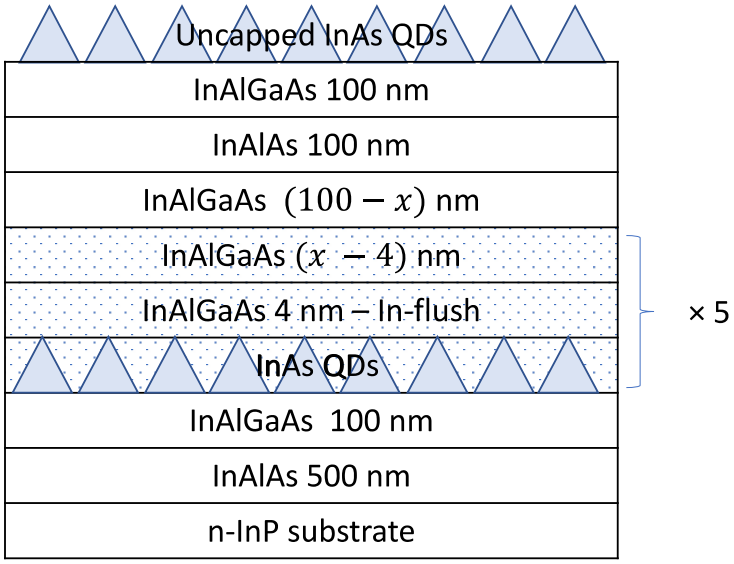

Figure 5-11. The schematic structure of five-layer QDs grown on InP substrates with different spacer layer thicknesses x.

Figure 5-12 (a) presents the PL intensities of the five-layer QD stacks with different spacer layer thicknesses ranging from 20 nm to 40 nm. Compared with the single-layer QD sample, the sample with 20 nm spacer layer demonstrates a much weaker PL intensity. This provides a clue that 20 nm is not sufficient for the InAlGaAs to recover the primarily flat surface, so that the QD growth in the subsequent layers is strongly affected. Usually larger dot size and a smaller density can be found for the upper layers if the strain is accumulated [44]. The emission wavelengths for the samples with different spacer layers are almost the same, around 1530 nm while a lowest FWHM of 50.9 meV is obtained for 40 nm spacer layer (Figure 5-12 (b)). To examine the QD morphology and density of the multi-layer sample, another sample with 40 nm spacer layer was grown with the same conditions and deliberately terminated after the growth of the 5th layer QDs. The AFM images of a single-layer sample and the 5th layer QD shown in Figure 5-13 (a) and (b) respectively demonstrate well preserved QD density and dot morphology.

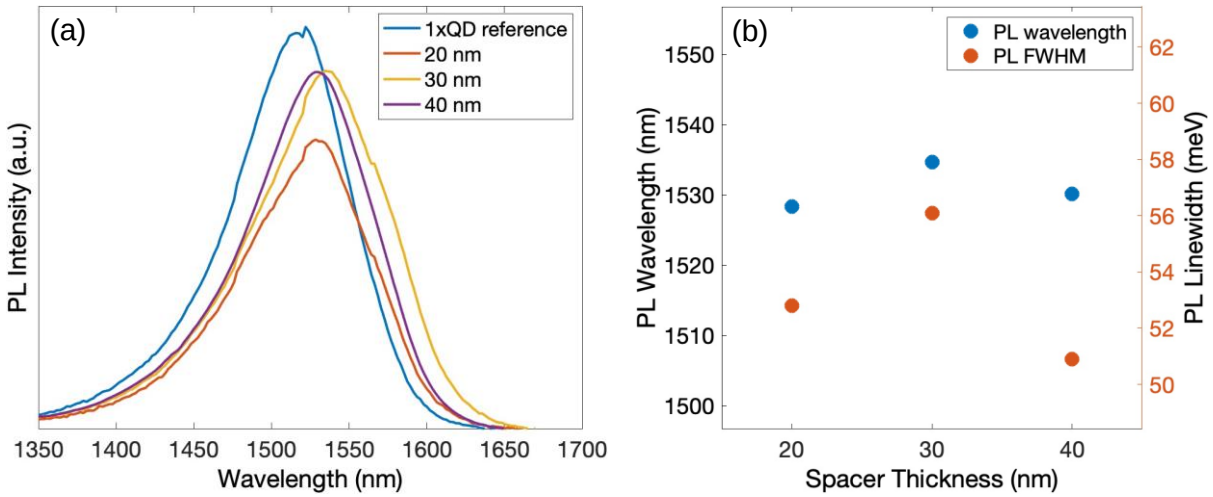

Figure 5-12. (a) PL intensities of five-layer QD structures with different spacer layer thicknesses. The PL of a single-layer QD sample is also shown as a reference. (b) PL emission wavelength and FWHM values for the samples with different spacer layer thicknesses.

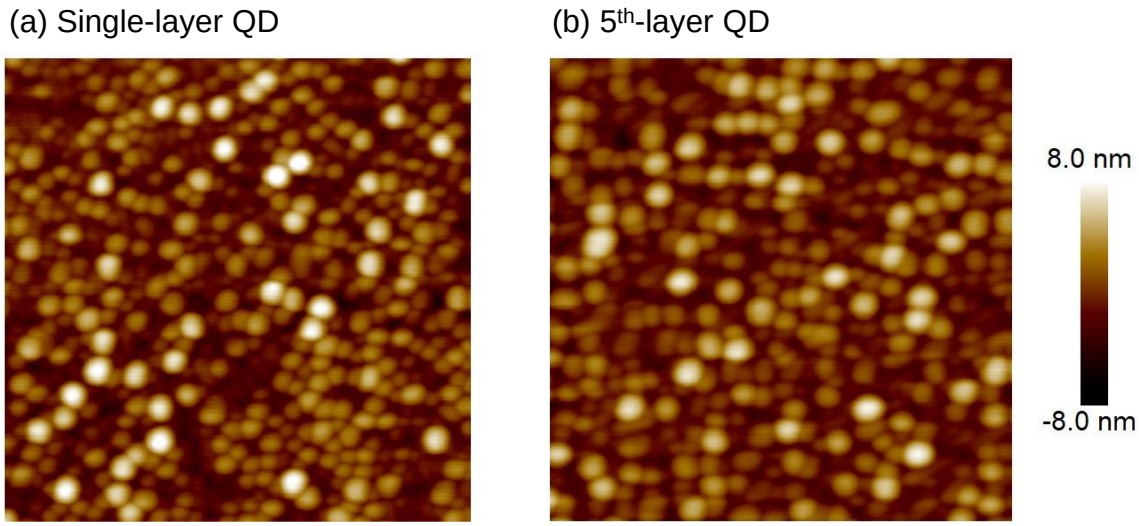

Figure 5-13. AFM images of (a) single-layer QD and (b) the 5th layer of a five-layer QD structure.

5.3 Optically pumped InAs/InP QDs microdisk lasers

Lasers, operating with stimulated emission, can provide coherent light with single frequency, same polarization, propagating direction and phase [53]. Semiconductor lasers are the most important type of lasers, of which the applications are extremely widespread such as in optical communication [54], optical data storage [55] and light detection and ranging (LiDAR) system [56]. Particularly, one of the most significant applications of semiconductor lasers is being used as light sources in optical communications. The recent exponential growth in the amount of network traffic requires higher modulation speed, more compact and energy-efficient light sources for optical interconnects and data centres [57, 58]. Compared with conventional large-scale lasers such as edge emitting ridge-waveguide lasers [17, 59, 60], microscale

lasers can generate coherent light at microscale [11]. Recently, due to their ultracompact footprint, low energy consumption and potentially high modulated speed, microscale semiconductor lasers have been widely studied and developed, which can find lots of applications particularly in optical interconnects and data centres [10, 11].

Microscale whispering-gallery modes (WGMs) microcavity lasers, such as microdisk lasers [61-63], have attracted intense research interest in many applications owing to their ultralow energy consumption, small footprint, and the possibility of dense integration for silicon photonics. Light is strongly confined in-plane by successive total internal reflections at the smooth ring periphery to form the WGMs with high quality factor and small mode volume [64]. Here, an optically pumped thin slab laser structure is designed and grown on InP substrate, as shown in Table 5-2. Table 5-2 shows the detailed epitaxial layer structure with InAs QDs as gain materials (five QDs layers separated by 30 nm $In_{0.528}Al_{0.238}Ga_{0.234}As$ barrier layers), of which the whole thickness of active layer is ~280 nm. The laser structure consists of 10 nm $In_{0.532}Ga_{0.468}As$ and 40 nm $In_{0.524}Al_{0.476}As$ lattice-matched to InP as the cladding layers and 5 repeats of nominal 5.5 monolayers (ML) thick InAs QDs separated by 30 nm $In_{0.528}Al_{0.234}Ga_{0.238}As$ barrier layers lattice-matched to InP. The growth parameters and steps are all optimised growth conditions obtained from the previous section 5.2. The top InGaAs cladding layer was designed as InAlAs layers are easy to oxidise. The PL spectrum of as grown InAs/InP QDs is presented in Figure 5-14, which covers the S band (1460 nm – 1530 nm), C band (1530 nm to 1565 nm), L band (1565 nm to 1625 nm) and U band (1625 nm to 1675 nm).

Table 5-2 Epitaxial structures of optically pumped InAs/InP QDs microdisk lasers.

Layers	Materials	Thickness
Cap layer	$In_{0.532}Ga_{0.468}As$	10 nm
Cladding layer	$In_{0.532}Ga_{0.468}As$	40 nm
×5 Barrier layer	$In_{0.528}Al_{0.238}Ga_{0.234}As$	30 nm
×5 Gain material	InAs QDs	1.7 nm
Barrier layer	$In_{0.528}Al_{0.238}Ga_{0.234}As$	30 nm
Cladding layer	$In_{0.532}Ga_{0.468}As$	40 nm
Cap layer	$In_{0.532}Ga_{0.468}As$	10 nm
Substrate	InP	

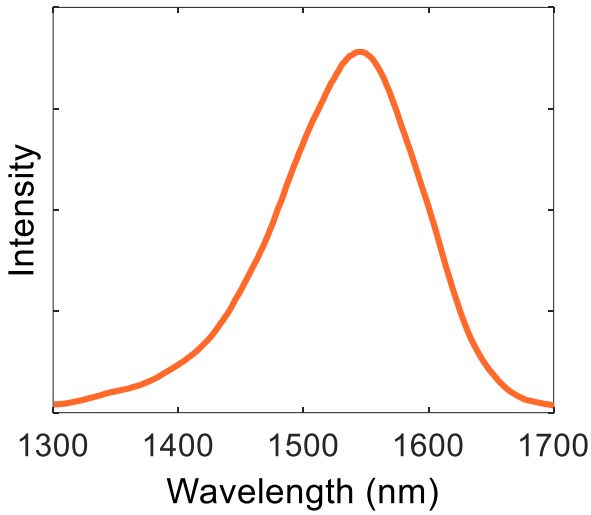

Figure 5-14. PL spectrum of as-grown InAs/InP QDs.

InAs/InP QDs microdisk lasers with diameter around 9 μm were designed at University College London by Dr. Taojie Zhou and fabricated at London Centre for Nanotechnology by Dr. Taojie Zhou and Hui Jia. The main fabrication processes for InAs QDs microdisk lasers are schematically presented in Figure 5-15 (also see Table 5-3 for details).

Table 5-3. Fabrication procedures for optically pumped InAs/InP QDs microdisk lasers.

Step 1.	Wafer dicing and cleaning. The as grown 2-inch wafer was diced into small chips with size 1 cm x 1cm (to test more designs and fabrication processes). The small chips were then cleaned by using acetone and isopropanol to avoid the contaminations.
Step 2.	Hard mask deposition. A layer of SiNx with a thickness of around 150 nm was deposited on the epitaxial wafer by p*lasma enhanced chemical vapor deposition* (PECVD) as the hard mask. A mixture of N_2, SiH_4/N_2 and NH_3 was used to deposit a uniform SiNx film.
Step 3.	Resist spin coating. The wafer was cleaned by using acetone and isopropanol before spin coating, then baked at 115 °C for 5 mins. A layer of 300 nm PMMA A4 electron beam resist was spin coated at a rate of 4000 revolutions per minute (rpm) on the surface of the hard mask and was baked at 180 °C for 90 seconds. To increase the uniformity for lithography process, the backside of the wafer was cleaned by using acetone to remove the adhesive resist.
Step 4.	Subsequently, the electron beam lithography (EBL) was used to define the microdisk pattern in PMMA. Electron beam with current 1 nA and dosage 650 μC/cm^2 was adopted for the lithography process.
Step 5.	After EBL, the wafer was developed in the MIBK:IPA (volume ratio = 1:3) solution for 30 seconds, followed by rinsing in diluted water for 30 seconds.
Step 6.	Dry etching process of hard mask. The microdisk pattern was further transferred from PMMA into the hard mask SiNx by using reactive ion etching (RIE) method with a mixture etching gas of CHF_3 and O_2.

Step 7.	Removing residual resist. O_2 plasma was implemented to remove the remained PMMA by using a plasma asher. The etching rate of PMMA is approximately 12 nm/min, the etching time is around 15 mins.
Step 8.	Dry etching process of III-V materials. The microdisk pattern was transferred from the hard mask into the active region and InP sacrificial layer by inductively coupled plasma RIE (*ICP-RIE*) plasma etching method. The ICP-RIE plasma etching was based on a mixture of BCl_3 and H_2 with 120 W platen power, 600 W coil power, a substrate temperature of 20 °C, chamber pressure at 2 mTorr and etching time of 140 seconds.
Step 9.	Wet etching process of hard mask. The residual SiNx hard mask was removed by soaking the sample in 48% hydrofluoric acid for 5 minutes.
Step 10.	Undercut process. Finally, an undercut process was implemented to form the suspending microdisk lasers, which were obtained by selectively wet etching InP (sacrificial layer) to form mechanically supporting pedestals. The diameter of the supporting pedestals was determined by the wet etching time.

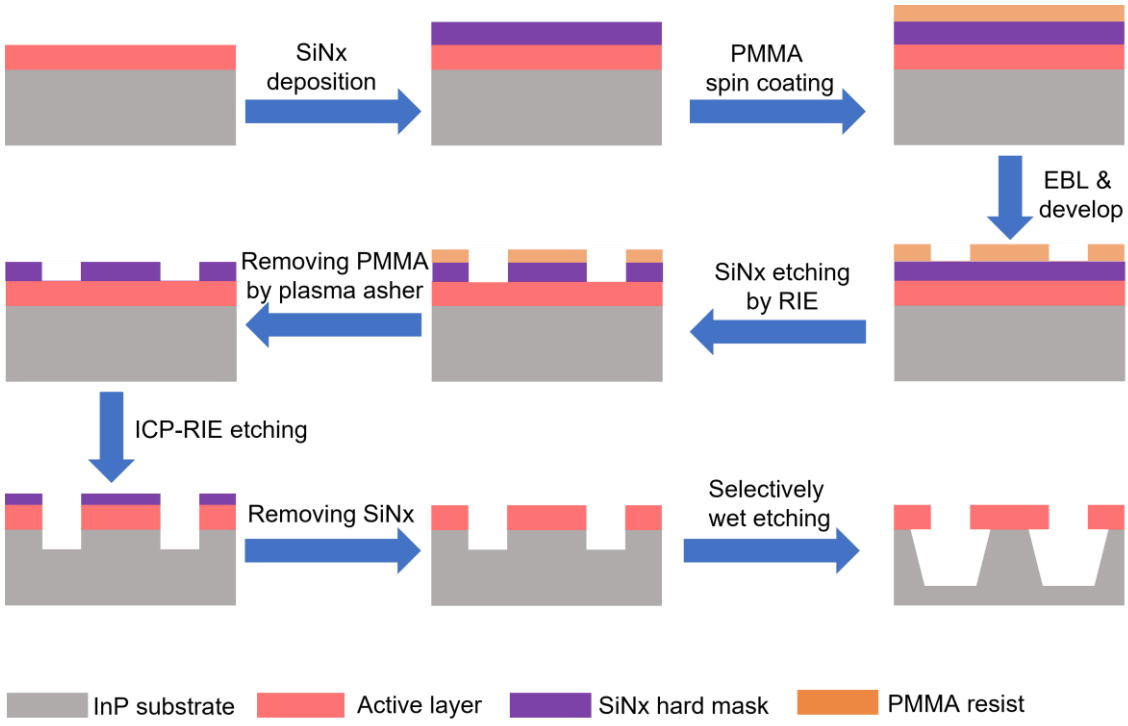

Figure 5-15. Schematic diagram of the key fabrication processes for the InAs/InP QDs microdisk lasers.

Figure 5-16 (a) presents an optical microscopy image of fabricated InAs/InP QDs microdisk laser array after selectively wet etching InP to form supporting pedestals. Owing to the nonuniformity during wet etching process, some microdisks are released from the supporting pedestals. As shown in Figure 5-16 (a), the microdisk labelled as A6B5 is released from the chip. Figure 5-16 (b) displays a tilted SEM image of fabricated InAs/InP QDs microdisk laser array. Figure 5-16 (c) depicts a tilted SEM

image of microdisk cavity before selectively wet etching the sacrificial material InP, showing that the microdisk pattern is transferred into both active layer and InP layer by ICP-RIE plasma etching. Figure 5-16 (d) and Figure 5-16 (e) present a top view SEM image and a tilted SEM image of fabricated microdisk laser, respectively. A small supporting pedestal is shown in Figure 5-16 (e). The distance between the supporting pedestal and the microdisk boundary is more than 3 μm, avoiding the light coupling loss of WGMs from the microdisk into the pedestal. Figure 5-16 (f) shows the enlarged SEM image of the etched sidewall of the microdisk laser, which helps to confine high quality factor (Q-factor) WGMs in the microdisk cavity.

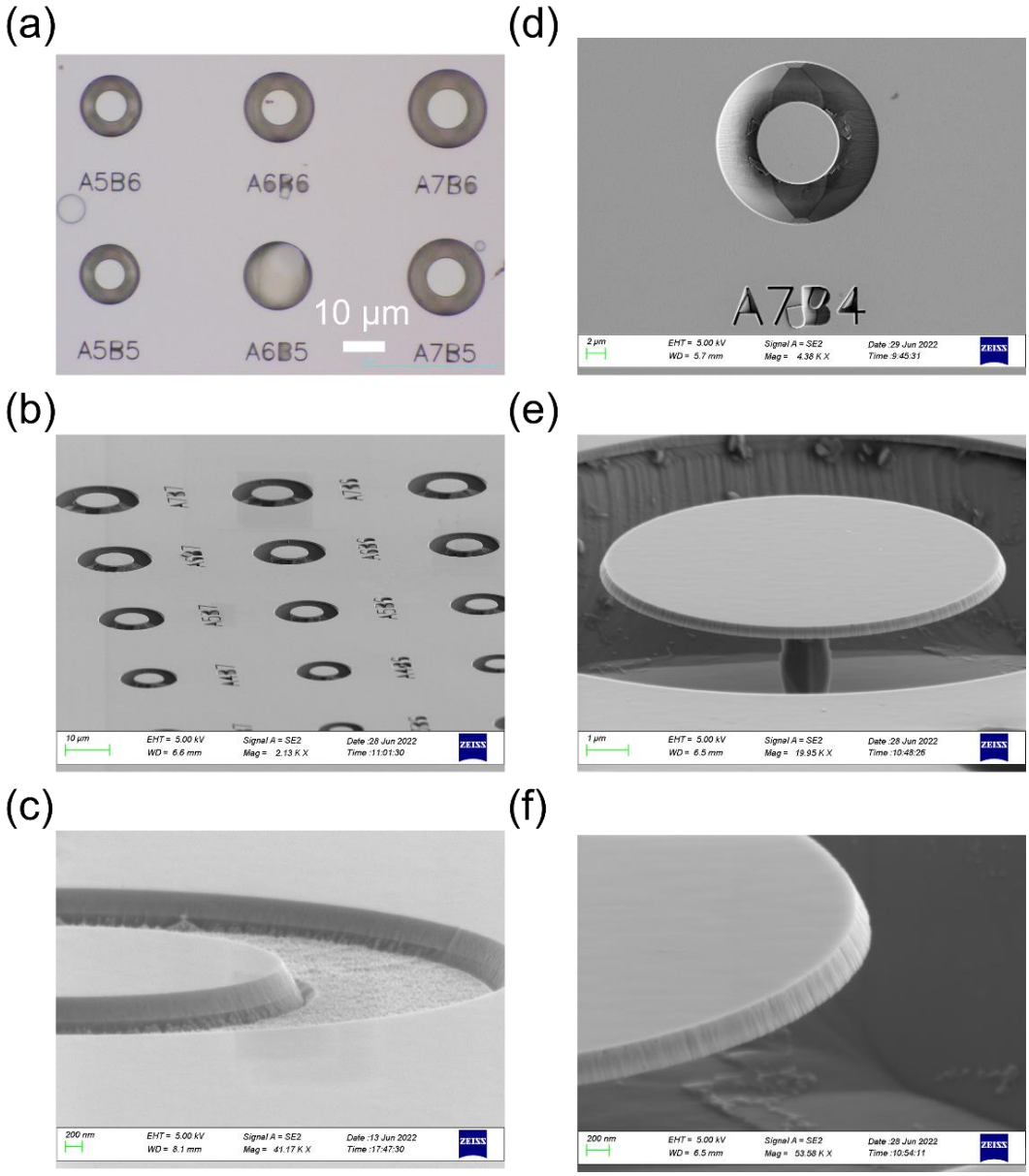

Figure 5-16. (a) An optical microscopy image of fabricated InAs/InP QDs microdisk laser array. (b) A tilted SEM image of fabricated InAs/InP QDs microdisk laser array. (c) A tilted SEM image of microdisk cavity before selectively wet etching InP. (d) A top view SEM image of fabricated microdisk laser. (e) A tilted SEM image of fabricated microdisk laser. (f) An enlarged SEM image of a fabricated microdisk laser.

The fabricated InAs/InP QDs microdisk lasers were optically pumped at room temperature with a micro-PL measurement system in a surface normal pump configuration, as described in section 2.6 in Chapter 2. Figure 5-17 displays a collected lasing spectrum of a microdisk laser with a diameter around 8.4 μm, compared with the spontaneous emission spectra of as grown InAs/InP QDs measured from unpattern region, which indicates that the spontaneous emission background is strongly compressed after reaching lasing threshold. The microdisk lasers can support multi first order WGMs with high quality, resulting in mode competition and multimode lasing emission. As shown in Figure 5-17, the lasing spectra has multi lasing peaks. The free spectral range (FSR) of the microdisk laser with diameter around 8.4 μm can be estimated by using the following equations:

$$FSR = \frac{\lambda^2}{\pi D n_g} \sim \frac{(1603\ nm)^2}{\pi * (8.3\ \mu m) * 2.9} = 36.6\ nm$$

supposing a group index $n_g = 2.9$. The calculated FSR is consistent with the experimental value, as shown in Figure 5-18.

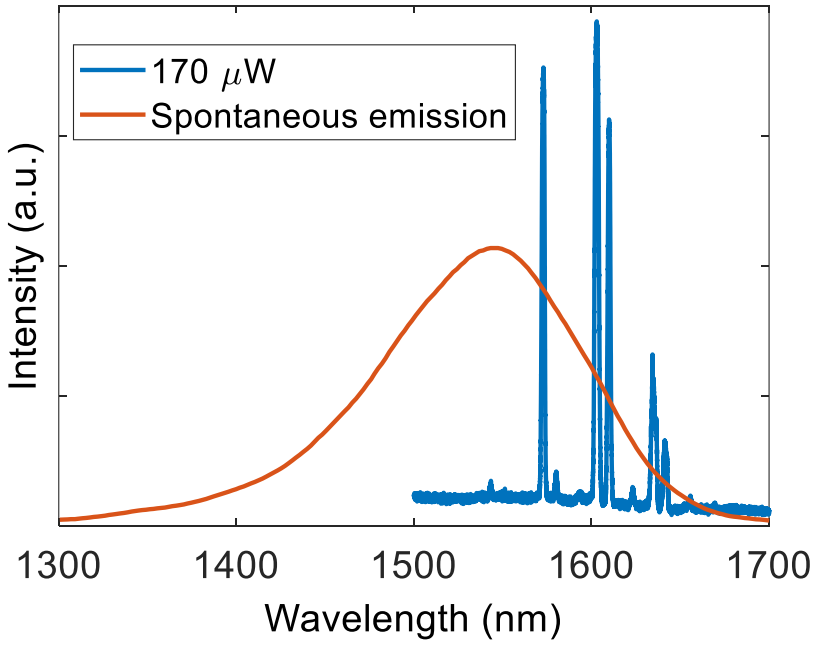

Figure 5-17. The collected spectra (blue) under pumping power 170 μW (above lasing threshold) of a microdisk laser with diameter around 8.4 μm and the spontaneous emission spectra (orange) of unpattern region, showing that the spontaneous emission is strongly suppressed after reaching stimulated emission.

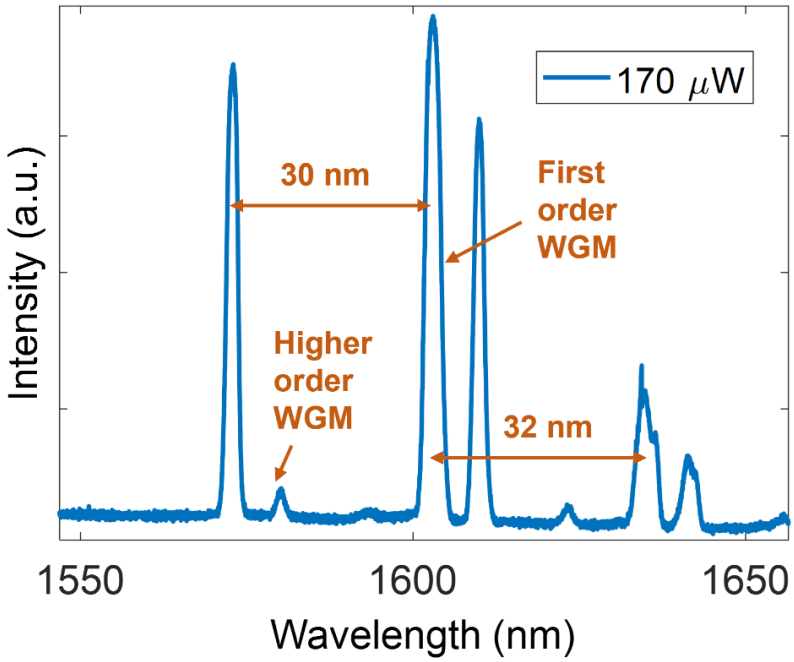

Figure 5-18. An enlarged laser spectra of the microdisk laser, indicating the multimode lasing emission with a value of experimental FSR is around 30 nm.

The strongest lasing peak (around 1603 nm) under high pump powers is chosen for further analysis. Figure 5-19 (a) presents the measured lasing spectra of the microdisk laser with diameter around 8.4 μm, showing a multimode lasing emission of the fabricated microdisk laser. The inset in Figure 5-19 (a) displays an enlarged logarithmic scale plot of the measured spectra around the lasing peak at 1603 nm from low to high pumping powers, showing a signal-to-noise ratio 13.5 dB. Figure 5-19 (b) shows the measured lasing spectra around the lasing threshold, showing that the resonant peaks grown up from the spontaneous emission background. The lasing threshold is estimated from the light in – light out (L-L) curve shown in Figure 5-19 (c). A clear kink in L-L curve can be observed with an obvious '*S*' shape in logarithmic scale shown in Figure 5-19 (d), indicating the transition from spontaneous emission to stimulated emission. A low lasing threshold approximately 30 μW (26.5 W/cm^2) is extracted from the kink point in L-L curve. At high pumping powers (above ~ 70 μW), the lasing intensity of the InAs/InP microdisk laser begins to saturate, which is mainly attributed to the gain saturation.

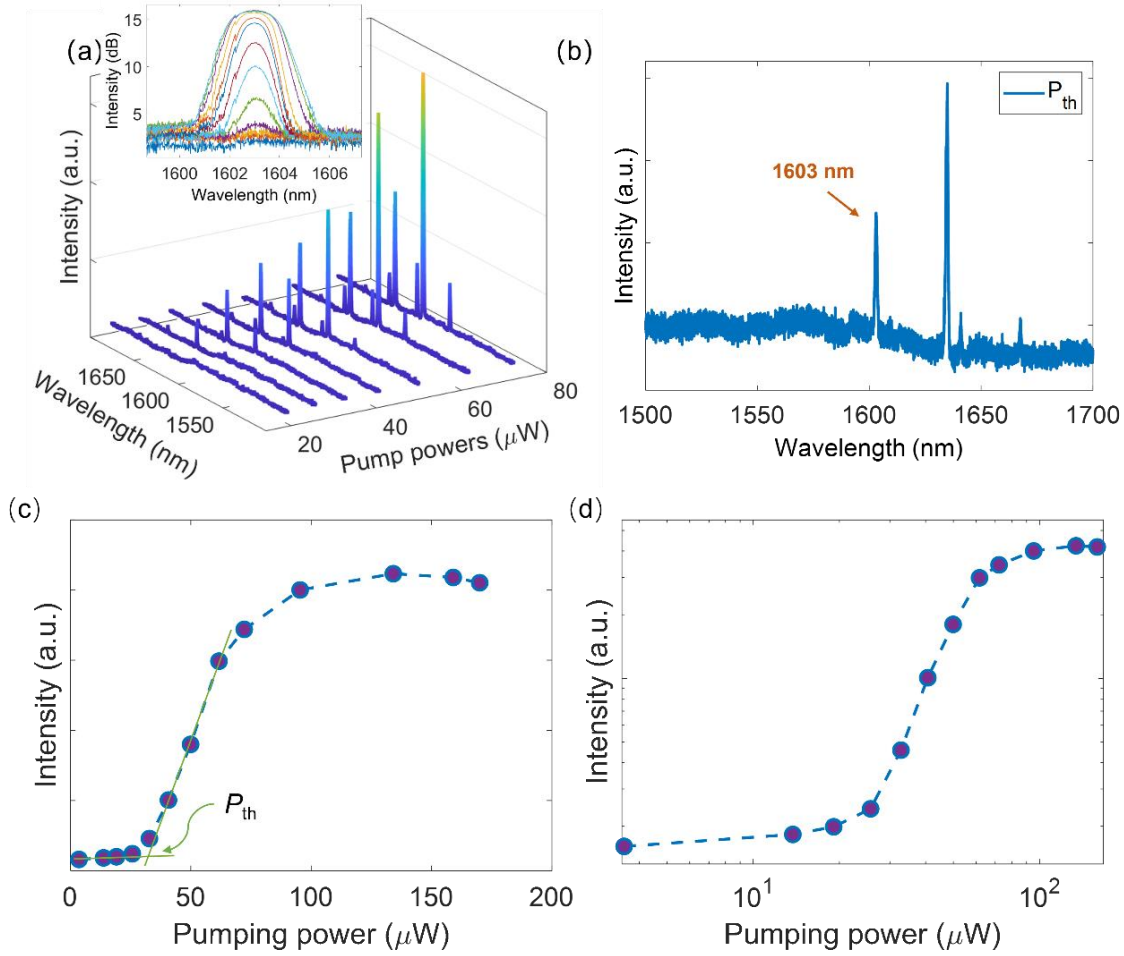

Figure 5-19 (a) Collected lasing spectra under various pumping powers. The inset in (a) displays an enlarged logarithmic scale plot of the measured spectra around the lasing peak at 1603 nm at various pumping powers. (b) The measured lasing spectra near the lasing threshold. (c) and (d) show the L-L curve in linear scale and logarithmic scale, respectively. The logarithmic scale L-L curve shows a 'S' shape, indicating the laser operation and transition from spontaneous emission to stimulated emission.

Q-factor quantifies the temporal confinement of photons in the cavity and cavity loss. The cavity Q-factor of fabricated InAs/InP QDs microdisk can be approximately estimated from the linewidth just below the lasing threshold, where the optical loss by the absorption of the QDs is very weak. The linewidth measured at just below the threshold corresponds to a value of Q-factor ($Q = \lambda/\Delta\lambda$) around 1336, where $\Delta\lambda$ is the linewidth at λ. The quality factor can be further increased by optimising the fabrication processes (e.g., adjusting the ratio of the BCl_3 and H_2 and controlling the etching time in the dry etching process) to achieve a more vertical and smoother sidewall of the microdisks and using the surface passivation method to decrease nonradiative recombination rate.

Figure 5-20 shows the near field intensity profile images measured by using InGaAs camera. Before reaching the lasing threshold, the emission of microdisk cavity is

dominated by spontaneous emission with a relatively uniform intensity distribution as shown in Figure 5-20 (a). After reaching the lasing threshold, stimulated emission dominates and forms WGMs tightly confined along the circular boundary of the microdisk lasers. As displayed in Figure 5-20 (b), light is distributed at the circular boundary with strong speckle patterns, resulting from the high degree of coherent emission. The high performances of the fabricated InAs/InP QDs microdisk lasers with low threshold and small footprint provide a promising route towards the ultracompact, high energy-efficient laser sources for optical interconnects and data centres.

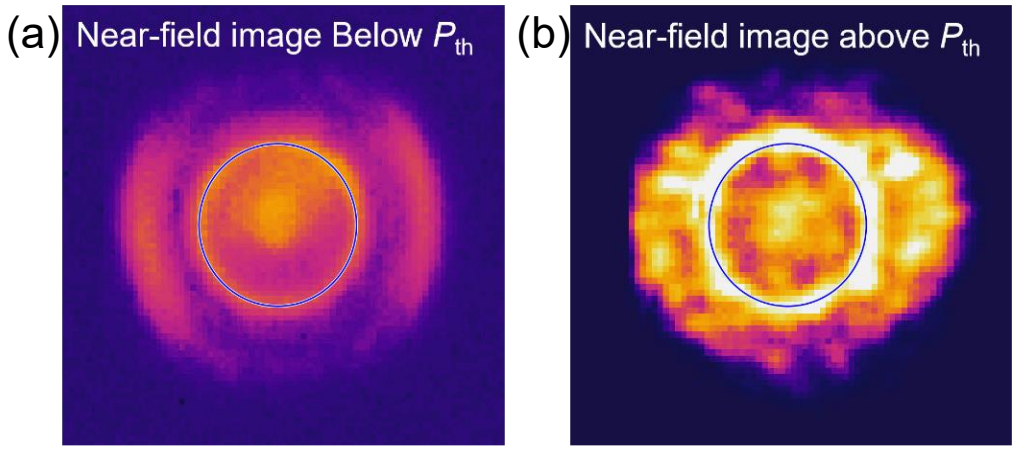

Figure 5-20. (a) and (b) shows the collected near field intensity profile images below and above the lasing threshold, respectively. The bule circle indicates the boundary of the microdisk lasers. The images are measured by using a InGaAs camera.

5.4 Conclusions

This chapter discusses the growth optimisation of InAs/InP QDs aiming at obtaining high density, high uniformity, and dot morphology QDs over QDashes for C-band lasers. The effects of deposition thickness and temperature have been investigated. It is found that a higher deposition amount of 5.5 ML results in the highest QD density and narrowest PL FWHM, further increase or reduction in deposition thickness leads to the presence of more dashes. This behaviour is thought to relate to a combination of the mediated strained InAs/InP material system and the dynamic interaction of the adjacent nanostructures and the supressed relaxation through the substrate. Based on this ‘QDash-like’ wetting layer, low-temperature-induced low In atom mobility is likely to cause non-uniform and increased nucleation of the large QDs whereas the uniform QD nucleation is suppressed. On the other hand, high growth temperatures stimulate QD coalescence and QD re-evaporation that reduce the QD density. An initial optimal growth condition applying 5.5 ML InAs and growth at 485 °C was

developed where a high QD density of 436/μm^2 was obtained. However, the PL FWHM was still quite large (~ 86 meV) and emission wavelength (1.8 μm) was far beyond C band.

The situation is significantly improved by applying the In-flush technique where the excessive In in partially exposed large QDs can be evaporated upon temperature elevation. The first capping layer thickness, material and annealing temperature have been determined. Enhanced PL emission along with a greatly reduced FWHM of 47.9 meV at RT is realised for single layer QD. The emission wavelength is 1522 nm. Five-layer structure with an optimal spacer layer thickness of 40 nm demonstrates a narrow RT PL FWHM of 50.9 meV and an emission wavelength of 1530 nm. The growth optimisation has resulted in a five-layer QD optically pumped microdisk laser emitting at ~ 1.6 μm, with a low lasing threshold of 30 μW and a quality factor ~ 1336. The demonstrated long-wavelength lasers with a low threshold and ultracompact footprint can find potential applications in integrated gas detection and highly localized label-free biological and biochemical sensing.

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Chapter 6.

Conclusions and Future Work

6.1 Conclusions

This chapter concludes the major contributions of this thesis towards the monolithic growth optimisation of buffer layers and development of light sources for Si photonics, by incorporating and improving different systems of Group IV thin films and III-V QD semiconductor materials. Several strategies have been studied for each part of the thesis, however significantly more efforts are needed to enable the monolithic integration of high-performance light sources on Si platforms. Therefore, some insights for further improvements and future work are also included in this chapter.

The study of literature on previous developments on Si photonics has highlighted advantages of the monolithic integration of high-performance light sources as well as other optoelectronic devices on Si over the heterogeneous and hybrid integration methods for data transmission purposes. However, the monolithic growth of the high-performance chosen semiconductors on Si has encountered two major challenges on the material level: on the one hand, the growth of efficient light emitters III-V semiconductors on Si encounters issues of large lattice-mismatch-induced TDs,

polarity-difference-caused APBs and thermal-expansion-incompatibility-induced cracks; on the other hand, as a rising star of direct-bandgap group-IV material, the growth of GeSn is also challenging as a result of the low solubility of Sn in Ge and the large lattice parameter of Sn. Methods tackling the crystal defects during heteroepitaxial growth of III-V on Si are manifold nowadays, such as applying thick III-V buffer layers, SLS and defect trapping layers, using patterned substrates, carrying out Si surface treatments or growing Si buffer, etc., with each of them has its own pros and cons. To contribute to the practical applications, the growth method must ensure a high crystal quality while maintaining an acceptable total thickness to avoid the cracks and enable the evanescent coupling to the waveguide (as in a laser device). It should also be repeatable, feasible and compatible with the mass-production line from the aspect of production ease. Therefore, the first part of this thesis, described in detail in Chapter 3, focused on developing low TD density Ge buffer for both III-V and group-IV semiconductor optoelectronic devices on Si.

The effects of Sb surfactant on Ge on Si growth have been investigated under various growth strategies, temperature, doping densities, and total thickness of the Ge layer. It was demonstrated that there exists an optimal doping density and doping temperature that result in the lowest TD density. The TD density reduction with increasing total thickness of Ge saturates quicker for the undoped samples compared with the Sb-doped samples. The TD reduction effect brought by Sb dopants is related to the elevated TD velocity and better substrate passivation. Other growth parameters such as the application of a temperature-ramp layer between the LT and HT layer, thermal annealing cycles and the type of dopants have been taken into account. It was found that a temperature-ramp layer might be helpful in suppressing the out-diffusion of dopants as well as increasing the chance of TD self-annihilation. More annealing cycles can further reduce the TD density for thicker Ge layers (> 1000 nm). Sufficient dopant supply is required to promote layer-by-layer growth while reducing TD density. A combination of different dopants may further facilitate the mismatch strain relaxation, thus more investigations can be done following this direction. TD densities of ~ 1×10^8 cm^{-2} and 3×10^7 cm^{-2} were realised for 500 nm and 1000 nm Ge layers grown on Si, respectively. These results are comparable to the TD density of ~ 1.8 – 2.2 μm GaAs buffer layer grown on Si substrates [1], therefore demonstrate their potential to serve as a high-quality platform for the monolithic integration of both III-V and group-IV optoelectronic devices on Si substrate for Si photonics.

The first step to produce GeSn-based devices is the growth of high-quality material. The main obstacles in GeSn growth are the difficulties in Sn incorporation, and Sn segregation. The Sn incorporation is reported to be supressed by compressive strain, the accumulation of which is inevitable due to the much larger Sn atom compared with Ge. As a result, increasing the deposition thickness of high-Sn-content GeSn grown on Si can easily lead to epitaxial breakdown (even with less than a hundred nanometre thickness). Reducing the accumulated compressive strain during GeSn growth is thus very important. Chapter 4 presents two promising growth methods for GeSn active devices, one is the insertion of a thin Ge layer to compensate the large compressive strain; and another one is the adoption of a low-temperature in-situ annealing to reduce the strain and enhance Sn incorporation to the Ge lattice sites. Improvements on crystal quality were observed both immediately from RHEED observations and from surface characterisations. TEM investigations revealed high crystallinity of the QWs grown on the in-situ annealed grading GeSn buffer layers. However, due to the low growth temperatures in the MBE chamber, no optical signals were observed for the samples so far, but in later studies, it was found that GeSn detector structure presented better dark currents compared with the Ge detectors grown on Si. It may be because the optimised GeSn growth method not only introduces no further defects, but also the TD density decreases with the overall layer thickness increase.

In addition, the thermal stability of a relatively thick GeSn layer (500 nm) with a critical indirect-direct-bandgap-transition Sn composition of 8% grown on Ge/Si was studied. Given the ex-situ annealing studies on thinner GeSn with similar Sn composition, the thermal stability of the thicker GeSn in this thesis presents comparable thermal stability. High degree of strain relaxation (> 90%) with no Sn segregation on the surface was achieved by rapid annealing at 500 °C. This investigation provides an insight in the thermal stability of thick GeSn layers grown on Si under ex-situ thermal annealing, which can be useful for GeSn-based device fabrication.

Apart from bulk materials, III-V QDs present natural advantages on defect tolerance and carrier confinement, which are highly welcomed properties for Si-based optoelectronic devices. However, the epitaxial growth of uniform self-assembled QDs is very sensitive to various growth parameters including temperature, V/III ratio, growth rate, growth interruption time, etc. Achieving a repeatable and well-controlled QD growth technique is thus highly demanded. The main challenge facing the C-band

InAs/InP QD growth is the morphology control of QDs over Qdashes. A combination of growth parameter adjustment and In-flush technique with different capping layers and annealing temperatures enabled the realisation of narrow RT PL FWHMs for single-layer and multi-layer QD structures in the work in this thesis. The measured FWHM of the RT PL is among the best ones in the literature although the excitation powers vary from work to work. Small footprint optically pumped microdisk lasers with a low lasing threshold of 30 μW were demonstrated. Electrically pumped FP lasers were also fabricated recently but the output power was only 0.57 mW. Improvements of fabrication of the samples are in progress.

6.2 Future work

Since we have successfully achieved lower TD density for the doped LT nucleation layer Ge grown on Si, further TD reduction may be expected for alternative n-type dopants such as P, who has a smaller lattice constant than Ge and penta-valency. More efforts can also be put on co-doping method in the LT nucleation layer. Moreover, the effect of this optimised Ge buffer can be examined by the performance of the device grown on it. Therefore, it is necessary to develop III-V or Group-IV devices such as InAs/GaAs QD lasers, GeSn laser or Ge and GeSn detectors on it.

Second, the in-situ annealed GeSn buffer layer growth method can be combined with tensile strain and n-type doping in the GeSn active region to achieve more efficient light emission from GeSn. In addition, as the effects of in-situ annealing are significantly different from the ex-situ annealing, a combination of both may provide a build-up effect and thus allow higher thermal budget for device fabrication.

Lastly, more growth parameters can be further optimised for the InAs/InP QD growth, including the wetting layer for QDs, the first capping layer for the QDs during In-flush, growth interruptions and spacer layer growth temperature. Moreover, the epitaxial growth on Si substrates is required for the ultimate applications.

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