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Efficient Dual Output Regulating Rectifier and Adiabatic Charge Pump for Biomedical Applications Employing Wireless Power Transfer †

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Abstract: A power management unit (PMU) is an essential block for diversified multi-functional low-power Internet of Things (IoT) and biomedical electronics. This paper includes a theoretical analysis of a high current, single-stage ac-dc, reconfigurable, dual output, regulating rectifier consisting of pulse width modulation (PWM) and pulse frequency modulation (PFM). The regulating rectifier provides two independently regulated supply voltages of 1.8 V and 3.3 V from an input ac voltage. The PFM control feedback consists of feedback-driven regulation to adjust the driving frequency of the power transistors through adaptive buffers in the active rectifier. The PWM/PFM mode control provides a feedback loop to adjust the conduction duration accurately and minimize power losses. The design also includes an adiabatic charge pump (CP) to provide a higher voltage level. The adiabatic CP consists of latch-up and power-saving topologies to enhance its power efficiency. Simulation results show that the dual regulating rectifier has 94.3% voltage conversion efficiency with an ac input magnitude of 3.5 Vp. The power conversion efficiency of the regulated 3.3 V output voltage is 82.3%. The adiabatic CP has an overall voltage conversion efficiency (VCE) of 92.9% with a total on-chip capacitance of 60 pF. The circuit was designed using 180 nm CMOS technology.

Keywords: active rectifier; adiabatic charge pump; biomedical implant; dual output design; inductive wireless power transfer; pulse frequency modulation; pulse width modulation; wireless power transfer

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1. Introduction

Advances in multifunctional and highly complex implanted biomedical devices require multiple voltage supplies. Due to the ever-increasing functionalities, there is a demand for an efficient method to provide energy to implantable devices. Transcutaneous wire connections for charging can be replaced by wireless power transfer (WPT) providing multiple power ranges [1]. The WPT can employ inductive [2] and capacitive [3] links to replace or recharge implanted batteries. WPT systems can operate at biosafety-compliant levels of output power at frequencies from 6.78 to 13.56 MHz [4,5]. Misalignment and safety issues in WPT designs are discussed with a focus on design strategies in [4,5]. Different arrangements of power transmission arrays have been proposed for biomedical research [4], however, a highly efficient power management circuit should also be able to handle misalignment caused by movement.

Power management units (PMUs) to manage the variable coupling of WPT designs have been developed for various biomedical applications and low-power portable electronics devices [4–8]. PMUs ensure the safety, reliability, efficiency, and compliance of the

operation and power distribution in low-power electronic systems. PMUs can convert the coupled ac voltage harvested to multiple levels of regulated dc voltages required in a system. In PMUs, passive rectifiers are commonly used in many large-scale applications but are unsuitable for low-power applications as they have poor power conversion efficiency (PCE) and voltage conversion efficiency (VCE). Passive rectifiers have high inherent voltage drops and are unsuitable for systems operating at low voltage levels. Using active CMOS diodes with a feedback network improves the PCE and VCE, but switching issues need to be addressed to decrease reverse leakage current caused by slow switching at the MHz inductive coupling frequencies requiring accurate control. Figure 1 shows the power efficiency of a conventional two-stage dual output WPT system in Figure 1a and a single-stage dual output regulating rectifier design is shown in Figure 1b. A conventional PMU has an active rectifier followed by low dropout voltage regulators (LDOs) [9,10]. Despite the high efficiencies of active rectifiers, the need for a separate second stage of regulation degrades the overall system efficiency due to the power loss in the bypass capacitor, C_{pass}. To support this two-step conversion, two large supply decoupling capacitors are required before and after regulation to reduce voltage ripple and improve regulation feedback stability. Full on-chip integration of two large capacitors in an mm-sized implant is prohibitive not only because of the large silicon area required but also because of eddy currents induced by the RF field in large solid metal planes, which substantially reduce the wireless power transfer efficiency. For state-of-the-art biomedical devices, there is a need for low-voltage supplies for the sensing circuits and a high-voltage supply for neural stimulation. Some applications such as optogenetics, require low voltage high current delivery for optical stimulation used for motor neuron rehabilitation [10–12]. The dual supply requirements depend on the function of the biomedical implant. Typical LED drivers are heavily duty-cycled and rapidly switch between the active and sleep modes. The PMU must be able to generate different levels of voltage supplies from a single source using multiple LDOs [13] as in Figure 1a, or by using a dual output approach as in Figure 1b. The efficiency of linear regulator is shown in Figure 2 over a change in the ratio of the voltage input V_{in}/V_{out}. For biomedical applications, high efficiency is required to power dissipation as heat [14].

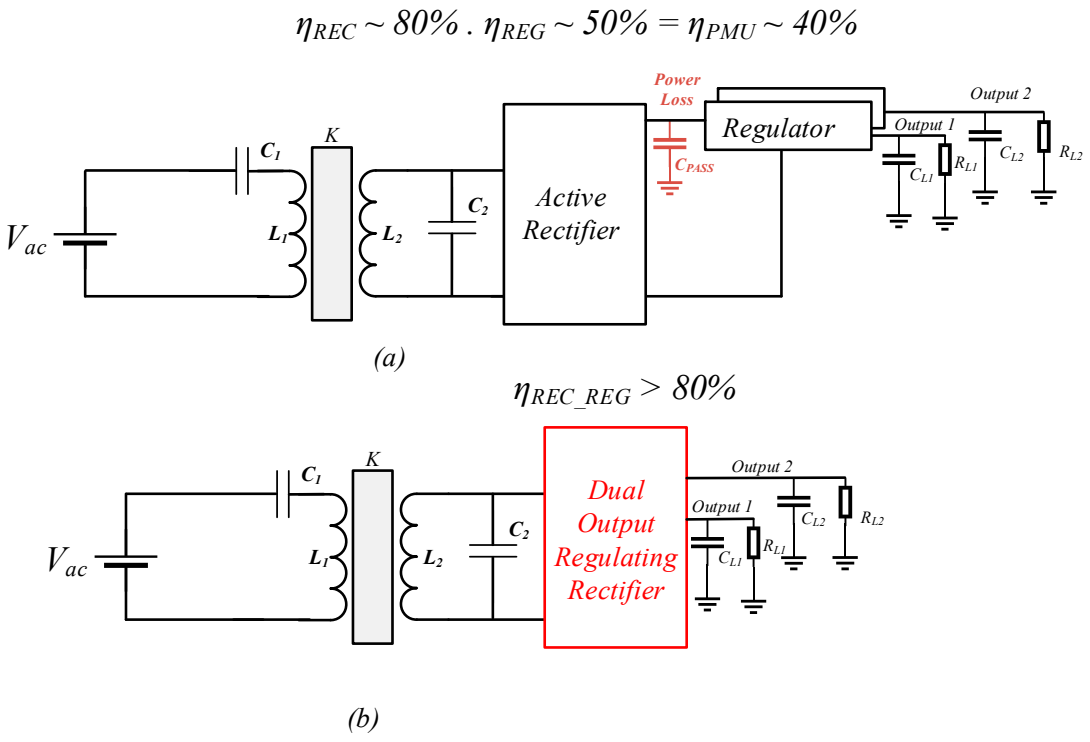

Figure 1. Block diagram of (**a**) conventional WPT system with C_{PASS} between two stages of regulation and rectification (**b**) single stage dual output regulating rectifier.

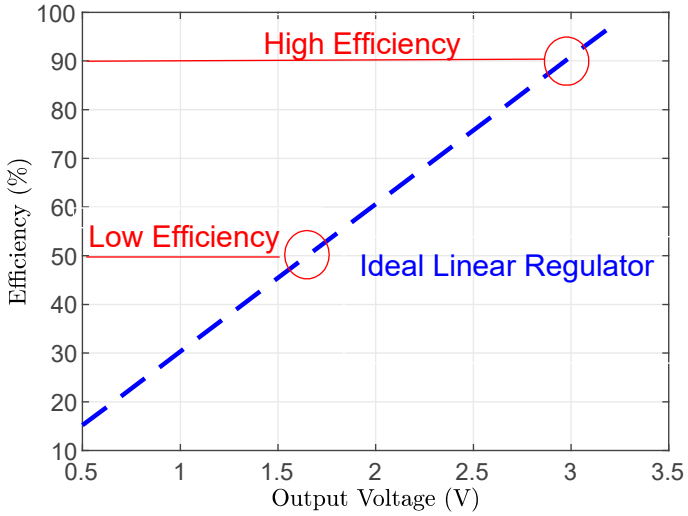

Figure 2. The LDO efficiency (V_{out}/V_{in}) of regulator changes over various output voltage.

This paper is an extension of [15] and focuses on the theory, analytical modeling, and architecture of a high current loads PMU using a dual output regulating rectifier with a feedback controller that has a stable feedback loop. It includes an analysis of the design of an adiabatic charge pump for a high voltage level supply of an implant. The design principles are illustrated in a general-purpose design for biomedical applications.

The manuscript is organized as follows. Section 2 describes the proposed system architecture including an efficient dual output regulating rectifier, and the design of an adiabatic charge pump and its layout is detailed. Section 3 includes results for each of the subblocks and further analysis with emphasis on optimization techniques. Section 4 discusses the overall performance of the system and comparison with the state-of-the-art. Concluding remarks are drawn in Section 5.

2. System Architecture and Working Principle

Figure 3 shows the overall system architecture of the WPT system in a multifunctional biomedical device. It consists of a class E amplifier with a self-tuning *RC* feedback network. The application-specific integrated circuit (ASIC) consists of a PMU that includes a dual output regulating rectifier with low voltage output *VL*, a regulated voltage output *VR*, and a high output voltage, *VH*, generated by an adiabatic charge pump. The adiabatic charge pump operates using a non-overlapping clock to control the clock signals. The system also consists of a class E oscillator and an additional communication and control block to optimize the performance and communicate with the external circuits but will not be considered in this paper.

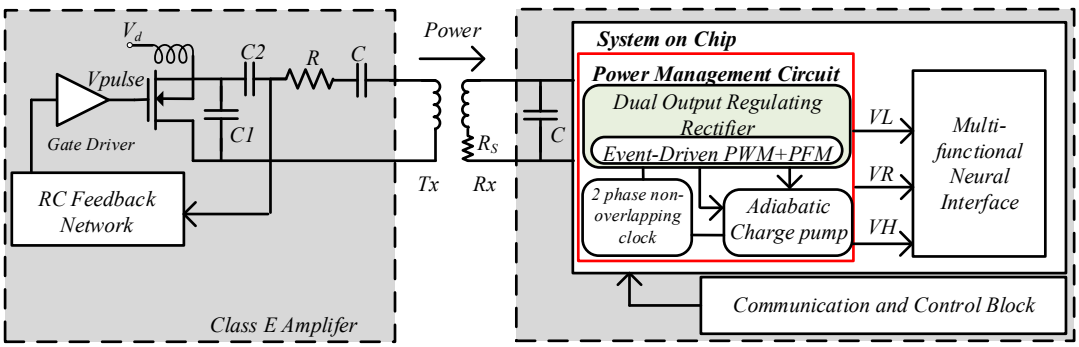

Figure 3. Proposed WPT system for a neural interface implantable device.

2.1. System Architecture

In a WPT system, when designing a PMU, it is crucial to maximize the magnitude of delivered power and overall power and voltage conversion efficiency. In this design, the voltage amplitude of V_{ac} across the RX coil from the class E oscillator will vary between 7 V and 9 V peak to peak as a result of variable *RX-TX* coupling due to body movement and mismatches. The power consumption at the power management input, P_{in}, is

$$P_{in} = \frac{V_{ac}^2}{2R_{ac}} \tag{1}$$

where R_{ac} is the input load resistance. The output dc power, P_{out}, from the two loads is

$$P_{out} = P_{out1} + P_{out2} = V_R^2/R_{L1} + V_L^2/R_{L2}. \tag{2}$$

Combining (1) and (2), the VCE of two outputs regulation and rectification is equivalent to $(V_R^2 + V_L^2)/V_{ac}^2$, the overall system's *PCE* is

$$PCE = \frac{P_{out}}{P_{in}} = \frac{V_R^2/R_{L1} + V_L^2/R_{L2}}{\frac{V_{ac}^2}{2R_{ac}}}. \tag{3}$$

In Equation (3) V_L and V_R are chosen to be 1.8 V and 3.3 V, respectively. R_{L1} and R_{L2} are the loads at the outputs of the regulating rectifier.

By maintaining a high VCE, the overall transferred PCE, $PCE_{overall}$, is

$$PCE_{overall} = \frac{P_{L1} + P_{L2}}{P_{in}} = 2R_{ac}\left(\frac{VCE_R^2}{R_{L1}} + \frac{VCE_L^2}{R_{L2}}\right). \tag{4}$$

In a conventional PMU achieving high PCE, VCE is limited as it consists of two steps, rectification and regulation and $PCE_{two\_stage} = PCE_{Rectifier} \cdot PCE_{Regulator}$. Due to the changes in coupling conditions between *TX* and *RX* coils during the patient's movement, regulation of the rectified voltage is required to provide stable dc voltages to the loads. The operating frequency is restricted to the industrial, scientific, and medical (ISM) bands of 6.75–13.56 MHz. These are the most used frequencies for implantable applications providing a good compromise between coil size, switching losses, and power attenuation through human tissue. With conventional WPT, two large supply decoupling capacitors are required before and after regulation to reduce voltage ripple and improve the regulation feedback stability. The decoupling capacitors will require a large silicon area and will cause eddy currents induced by the large metal planes degrading the overall efficiency. Using high-speed LDO regulators lowers the size of the decoupling capacitors but has large quiescent power consumption. Having multiple LDOs decreases the overall *PCE* and *VCE* of the system with high current loads.

2.2. Dual Output Regulating Rectifier Architecture

To address the disadvantages of the cascaded two-stage rectifier (Figure 1a), the design of the dual output regulating rectifier topology can improve the overall system efficiency and offer greater integration compactness. Figure 4 shows the dual output regulating rectifier using either pulse width modulation (PWM) or pulse frequency modulation (PFM). To optimize efficiency PFM is selected by the power management circuit when there is low power demand. The (variable) floating ac voltage (V_{ac+} and V_{ac-}) on the receiving coil Rx from the class E oscillator is applied to the regulating rectifier (Figure 2). The two regulating rectifier outputs: *OUTPUT 1* of *VL* = 1.8 V and *OUTPUT 2* of *VR* = 3.3 V are suitable for various applications. *OUTPUT 1* and *OUTPUT 2* each contain two multiplexers that are connected to sets of different numbers of pMOS transistors 2×, 4×, 6× in parallel selected by the power management circuit to decrease power losses and reverse current [16]. The choice of the number of pMOS power transistors provides a tradeoff between the

conduction and switching losses to optimize the PCE over a wide range of load values. The active rectifier controllers feature body-biased high-speed comparators [14], and PFM dynamic buffers as shown in Figure 5 that can support several operation modes to minimize power losses by adjusting the switching frequency. The regulating rectifier controllers feature adaptive body biasing (*ABB*) to the body of the power pMOS transistors, so they are always connected to the highest terminal between the input terminals (V_{ac+} and V_{ac-}), and the outputs terminals *OUTPUT1* and *OUTPUT2* (1.8 V or 3.3 V). The circuit of *ABB* is shown in Figure 6.

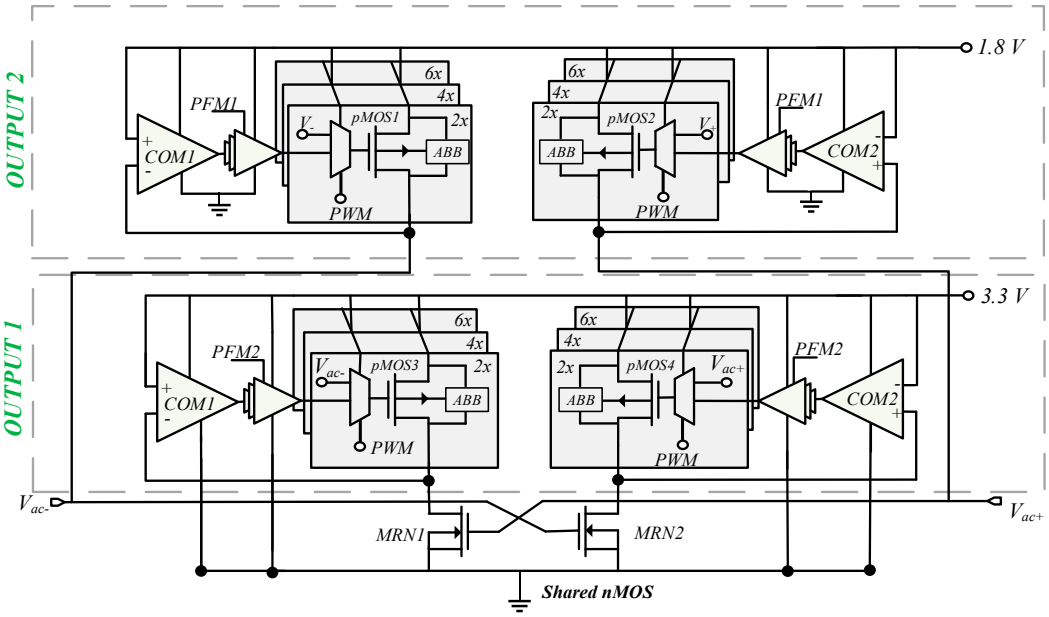

Figure 4. Proposed dual output regulating rectifier with PWM/PFM event-driven feedback control.

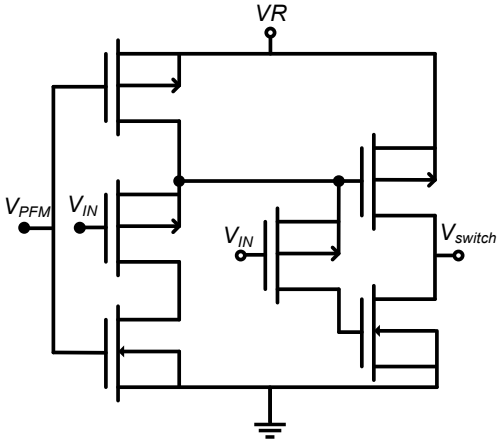

Figure 5. Adaptive PFM controlled buffer V_{PFM} from PFM controller, and V_{IN} from the high-speed comparator output, and V_{switch} connected as an input to the pMOS switches.

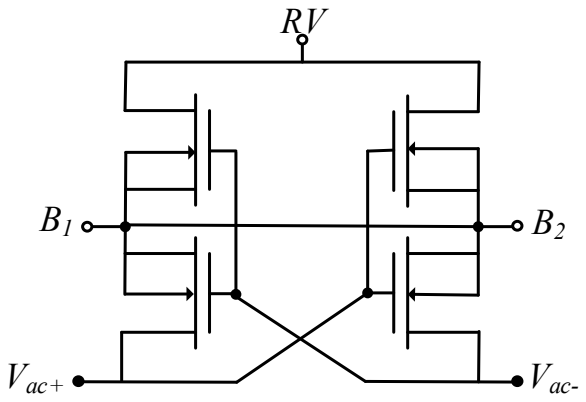

Figure 6. Adaptive body biasing (ABB) with B_1 and B_2 connected to the body of *pMOS1 and pMOS 2*, respectively.

Using the body terminal can help avoid the problem associated with the threshold voltage. Connecting the pMOS transistors to the coil terminals can cause a large voltage variation at high frequencies, resulting in latch-up and substrate leakage. Separate n-well voltages are controlled with auxiliary pMOS transistors that connect the n-well to the output voltage, *RV* or the coil terminal, V_{ac+} or V_{ac-} to the higher potential. Another advantage is the elimination of the body effect on the rectifying pMOS transistors and the reduction of the active rectifier dropout voltage and power dissipation. Implementing *ABB* can improve PCE by 4% at 1 kΩ load; at 300 Ω load PCE improvement is 1.5%.

The block diagram of the application of PWM and PFM to the regulating rectifier is shown in Figure 7. The outputs of the active rectifier controllers are fed to a PFM controller to trigger the regulation speed of the dynamic buffers. PFM only operates at low power when required for power-saving optimization and ensuring that the active switches in the rectifier are operating at their optimal frequency and duty cycle. The PWM controller consists of an error amplifier, a rail-to-rail static comparator, and an accurate ramp generator required for generating the PWM feedback loop. The switching configuration between PWM and PFM is shown in Table 1.

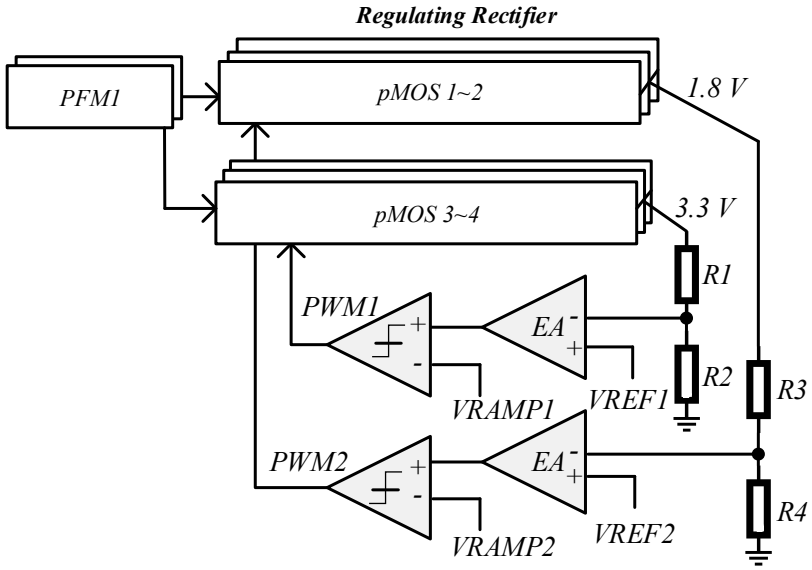

Figure 7. Block diagram of the dual output regulating rectifier. R_1, R_2 , R_3, and R_4 are high-value pseudo resistors. The design includes *PWM1,2* and *PFM1,2*.

Table 1. Operation modes of the dual output regulating rectifier.

PWM	PFM	Operation Mode
OFF	OFF	Diode connected
ON	OFF	Comparators connected
OFF	ON	Frequency decreased. Power saving mode
ON	ON	Frequency decreased

During startup, PWM and PFM are off making the diode connection. Only when PWM is switched on the comparators are connected. When PFM is on, the frequency is decreased for power-saving mode. This gives the system the ability to regulate and adapt to various input frequencies.

2.3. Feedback Control Analysis and Design Considerations

The width of the activation pulse is controlled by the PWM analog feedback loop. The PFM feedback loop is non-linear. The bandwidth limitation on the output dc voltage regulation of the PWM feedback loop must be minimal. The active feedback loop acts as a filter that can compensate for the ripple on the dc output using PWM. The PWM topology is utilized in biomedical applications with high current requirements and designed for R_L = 100 Ω–2 kΩ.

2.3.1. Pulse Width Modulation (PWM) Control

Pulse width modulation (PWM) can be used to regulate the output voltages of the rectifier by turning on and off the switching in the rectifier with a pulse to control the average output voltage. The PWM controllers sense the output voltages *RV* and *LV* and compare them to the reference voltages V_{REF1} and V_{REF2}. Timing of the pulse width uses an accurate voltage ramp generator shown in Figure 8. The delay from the start of the ramp to the point at which it exceeds the signal for comparison (the output of *EA*) defines the pulse width. An accurate ramp slope is necessary, as it is related to the feedback loop gain. A significant portion of the power consumption is in the ramp generator and having a low-power design is crucial. The current sources (I_s) are well matched to ensure a 50% duty ratio providing a ramp signal with a constant amplitude and repetition rate.

The PWM mode has an overall PCE, η_{PWM}, given by

$$\eta_{PWM} = \frac{P_{out}}{P_{in}} = \frac{V_{REC}^2 / R_{load}}{P_{cond} + P_{switch} + P_{static}} \quad (5)$$

where P_{cond} is the power from the source accounting for conduction losses, P_{switch} are the switching losses, and P_{static} the switching losses of the PWM subblock. The PWM controller conduction of two stages is 22 μW in this implementation. It can be further optimized by increasing the number of event-driven modules within the block.

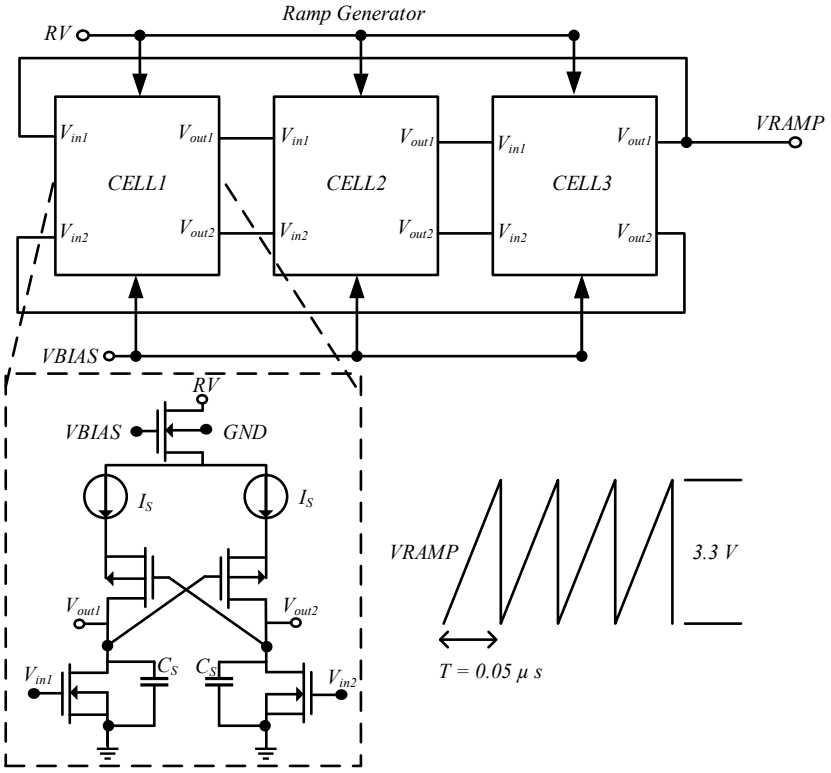

Figure 8. Accurate ramp generator circuit for *VRAMP*.

2.3.2. Pulse Frequency Modulation (PFM) Control

Pulse frequency modulation is used to regulate the output voltage of a rectifier by controlling the frequency of the pulses. The PFM control signals determine the frequency of the pulses in response to changes in the load or the input voltage, allowing the rectifier to maintain a relatively constant output voltage. PFM control is in discontinuous conduction mode and is preferable for light to moderate loads due to its low switching frequencies and reduced switching losses. Combining PFM and PWM control is highly preferable [17]. The feedback loop controls the frequency of the rectifier conduction. During each switching event, the rectifier conducts from t_1 to t_2 in the positive cycle and t_3 to t_4 in the negative cycle. The assumption is that the rectifier conducts for one complete cycle every T seconds. The charge supplied to the load Q_{out} in this period is

$$Q_{out} = \int_0^T I_L dt = \frac{V_{OUT}\ T}{R_L} \tag{6}$$

where I_L is the current in the load R_L and V_{OUT} is the voltage at the load. The input charge Q_{in} supplied by the input is

$$Q_{in} = \int_{t_1}^{t_2} \frac{V_0\ \sin(\omega_0 t) - V_{OUT}}{R_s} dt. \tag{7}$$

The efficiency of the η_{PFM} is

$$\eta_{PFM} = \frac{\frac{V^2{}_{OUT}\ nT_1}{R_L}}{P_{cond}(t_2 - t_1) + P_{switch}(t_2 - t_1) + P_{static}}. \tag{8}$$

There are n conducting cycles for every switching event. The switching period is nT_1 resulting in constant switching frequency and efficiency at various n periods, but at a cost of voltage ripple. The integration can be computed numerically [18]. For switching loss mitigation, the PFM is preferably used in light load conditions.

In this design, there are two frequency controllers, PFM controller 1 and PFM controller 2 for voltage outputs *LV* and *RV* of the regulating rectifier block. They provide a feedback loop that controls the frequency at which the rectifier conducts. The timing diagrams with the block diagram of the PFM control are shown in Figure 9. Under light loads, the pulse frequency decreases to narrow the pulse widths, limiting the PWM mode and reducing the overall switching power losses. Under heavy load conditions, the pulse frequency increases to eliminate reverse currents from the load to the coil. The PFM design is shown in Figure 9a.

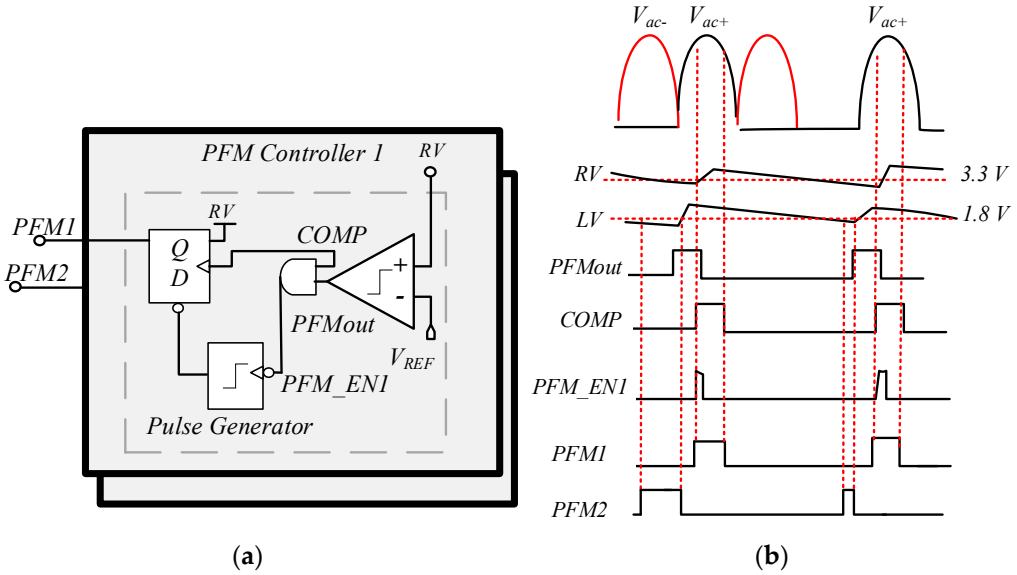

Figure 9. (**a**) Architecture of the PFM controller and (**b**) time domain response.

The signal time domain waveforms for a critically narrow pulse width are shown in Figure 9b. When *RV* increases, the PFM is enabled, *PFM_EN*, creating a square waveform for *PFM1*; however, when *LV* decreases *PFM2* is enabled with *PFM_EN2*. This ensures that the output loads *RV* and *LV* are regulated.

2.4. Charge Pump Design and Analysis

In some biomedical applications, a charge pump (CP) circuit is required to efficiently convert a low voltage to a higher voltage. Stimulators in biomedical applications are heavily duty-cycled requiring quick transitions between active and sleep mode. A CP should operate efficiently at both high and low output loads to ensure that the sleep mode is power efficient. The current demand for implantable stimulators is a few mA; many designs require off-chip capacitors and large-size power transistors to reduce their on-resistance to minimize the conduction power loss. On-chip pump capacitors are possible by using a suitably high clock frequency.

2.4.1. Charge Pump Principals

There are several CP topologies: (1) linear CPs which are based on Dickson CPs [19], (2) nonlinear CPs based on the Fibonacci CPs [20], and (3) exponential CPs [21]. A linear CP is shown in Figure 10 with n stages and n pump capacitors for an input/output conversion ratio of n.

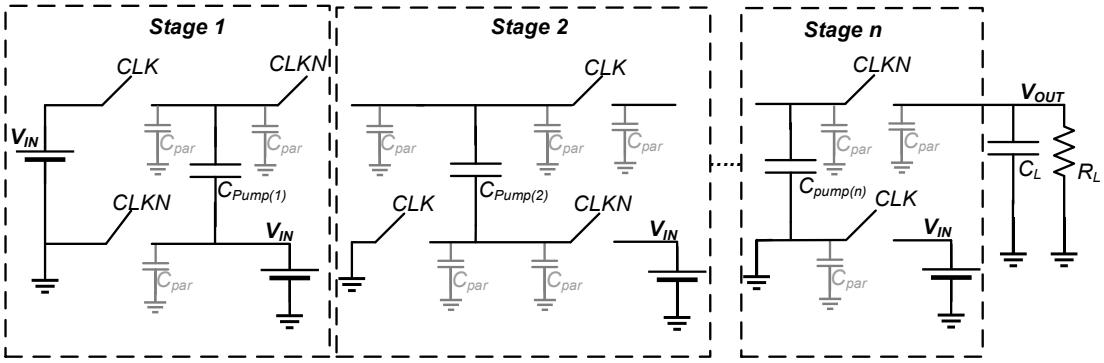

Figure 10. Linear charge pump with n stages.

In a conventional CP design, the charge is stepped up from the supply, V_{IN}, to the output node, V_{OUT}, stage by stage. The voltage step ΔV at each of the pumping nodes is

$$\Delta V = V_{Clock}\frac{C_{pump}}{C_{pump}+C_{parasitic}} - \frac{I_{OUT}}{f\left(C_{pump}+C_{parasitic}\right)} \tag{9}$$

where V_{Clock} is the voltage amplitude of the clock signals (CLK and $CLKN$) used, C_{pump} is the pumping capacitance, and $C_{parasitic}$ is the parasitic capacitance at each pumping stage, I_{OUT} is the current output, and f is the clock frequency. Assuming the clock voltage, $V_{Clock} = V_{IN}$, the voltage step ΔV is

$$\Delta V \approx V_{clock} = V_{IN}. \tag{10}$$

In a four-stage CP circuit that comprises diode-connected MOSFETs to transfer the charge from one stage to the next, the output voltage V_{OUT} is

$$V_{OUT} = \sum_{i=0}^{4}(V_{IN} - V_{t(M_i)}) \tag{11}$$

where $V_{t(M_i)}$ is the forward voltage drop across the diode-connected MOS. In the charge sharing Dickson design [22], the topology has a reliable control and a clocking scheme that is feasible for integrated circuits. However, the transistors are diode-connected resulting in a forward voltage drop that is equivalent to the CMOS threshold voltage. The threshold voltage increases due to the body effectively when the voltage is stepped up at each stage. The CP efficiency can be significantly degraded by the body effect as the number of pump stages increases. A four-phase clock generator has been proposed but it requires a complex generator that consumes extra power [22]. The output voltage V_{OUT} with a two-phase clock using n stages is:

$$V_{OUT} = V_{IN} + n\left(V_{IN}\frac{C_{pump}}{C_{pump}+C_{parasitic}} - \frac{I_{out}}{f\left(C_{pump}\right)} - R_{LOAD}I_{OUT}\right) \tag{12}$$

where R_{LOAD} is the output load resistance. If $C_{pump} >> C_{parasitic}$ and $V_{CLK} \gg \frac{I_{OUT}}{f\left(C_{pump}+C_{parasitic}\right)}$ then $V_{CLK} \sim V_{IN}$. The voltage loss, V_{loss}, is

$$V_{loss} = \frac{I_{OUT}}{f\left(C_{pump}\right)}. \tag{13}$$

At a small V_{OUT}, R_{LOAD} is not taken into consideration. V_{OUT} of the switch-capacitor charge pump (SC-CP) determines the power and voltage conversion efficiency. Generally,

the larger the value of the pump capacitors used, the larger the V_{OUT} and parasitics. The output power, P_{OUT}, of the SC-CP is

$$P_{OUT} = V_{OUT} \; I_{OUT} = \frac{V_{OUT}^2}{R_{LOAD}}. \tag{14}$$

The theoretical maximum power efficiency η_{CP} of the CP is

$$\eta_{CP} = \frac{V_{OUT}}{M \; V_{IN}} \tag{15}$$

where M (>1) is the voltage conversion ratio of the CP. The efficiency is inversely proportional to V_{in}. Gate-oxide reliability problems can arise due to the high-voltage overstress that occurs on the gate oxides [23,24]. The voltage overstresses on the gate oxide accumulates over time ultimately causing oxide breakdown which is more harmful to the gate oxide than the short transient stresses. To ensure high efficiency in the CP, good gate-oxide reliability, and minimizing the voltage drop in the CP switches is necessary. In [24], applying a latch-based CP topology can provide charge transfer equal to the switching clock amplitude. In [25], thfve number of stages is reduced by using a current consumption minimization strategy. In [26], the respective body terminals of the switches are dynamically body biased to two pairs of transistors to ensure the substrate and n-well are always connected to the optimum voltage terminal during operation.

A SC-CP converter performance in steady-state is evaluated by calculating the output impedance [27]. The evaluation of the resistive impedance as a function of frequency relies on two limitations: the resistive leakage paths and the charge transfer among (ideal) capacitors. The formulation developed to permit the optimization of the capacitor size to meet a constraint such as the total capacitance or the total energy storage limit, can also help in optimizing the switch sizes with switching power. Additional losses are due to the short-circuit current, parasitic capacitance, and gate-drive losses, which can be taken into consideration in further analysis. There are two extreme limits affecting a low output impedance:

(1) Slow switching limits (SSL) when all the switches and other conductive interconnects are assumed to be ideal, and the currents flowing between the input and output source and the comparators are ideal pulses, the SSL impedance is inversely proportional to the switching frequency, and the capacitors provide charge transfers without loss.
(2) Fast switching limits (FSL) when the resistance of the switches, capacitors and interconnects dominate. Capacitors act as voltage sources. In such a system, the current flow occurs in a frequency-independent piecewise constant pattern.

2.4.2. Adiabatic Charge Pump

Inherent potential reverse charge sharing losses can be reduced by using a charge recycling technique to reduce the bottom capacitance plate parasitic losses. The reliability issue due to gate oxide stress is addressed by providing a non-overlapping clock and ensuring the gate and source voltages do not exceed the input voltage. The design has a high-efficiency pumping operation and minimizes the voltage drop while charging. A charge-sharing topology was proposed in [28] for a linear charge pump in which a two-step waveform is applied on the gates of the transistors to reduce current peaking and improve the PCE. As the output current requirement increases the PCE decreases significantly and addressing the current peaking issue can improve the PCE.

A stage in the CP design is shown in Figure 11a and the timing signals are shown in Figure 11b. There are three identical stages. It modifies the latch CP design to decrease the overall power consumption by implementing virtual ground and bulk biasing. This adiabatic technique reduces energy dissipation by decreasing the voltage swings and current peaks which halve the power dissipation improving the PCE of the charge pump. This topology minimizes the voltage drop across the current source by slowly ramping up the

supply voltage. Recycling the charge dissipated helps energy reduction by implementing a virtual ground-bound charge in a capacitor, and then reusing the same charge by an internal feed of the virtual input. The use of virtual ground-bound charge can pump up the capacitors' input with the virtual input provided. The virtual ground nodes boost the potential of source terminals of n-channel transistors and reduce sub-threshold leakage exponentially due to the reduced body effect. It helps to obtain a high PCE as the sub-threshold leakage charge can be collected and recycled. The virtual ground capacitor has less leakage than a transistor channel. The bulk biasing circuit for each CP stage is required to ensure that the pMOS bulk is connected to the highest potential and the nMOS bulk is connected to the lowest potential. This reduces the threshold voltage at a forward bias and increases the threshold voltage at a reverse bias to ensure that the transistors operate within their limits. The bulking capacitors are minimum size to avoid an increase in parasitic capacitance. The clock-generating circuit for *CLK* and *CLKN* is as in [15].

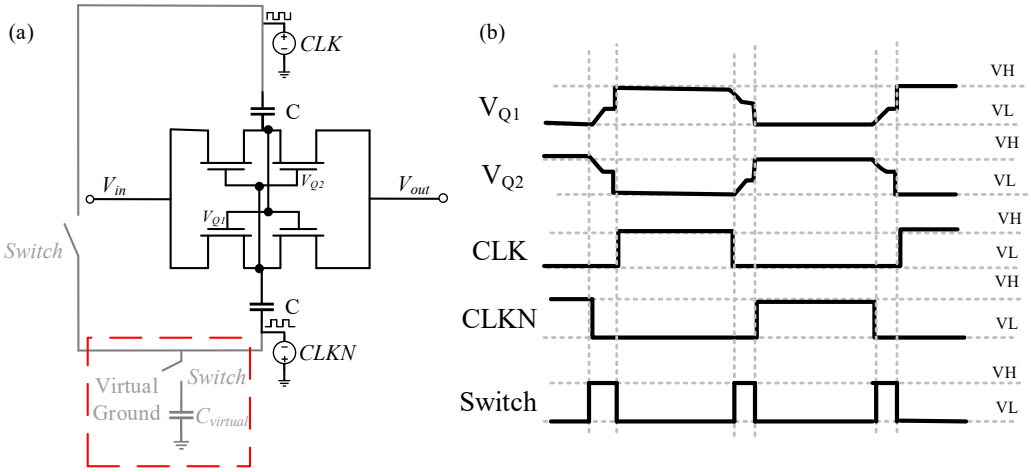

Figure 11. (**a**) The adiabatic schematic (**b**) timing signals of the adiabatic charge pump.

As shown in Figure 12, all nMOS transistors are in a single P-well within a deep N-well. The N-well is large enough to accommodate all the pMOS transistors in the same well. This causes the bulks of the pMOS and nMOS transistors to be connected by a distributed parasitic diode. The bulk bias circuit of each stage of the charge pump can provide dynamic body biasing.

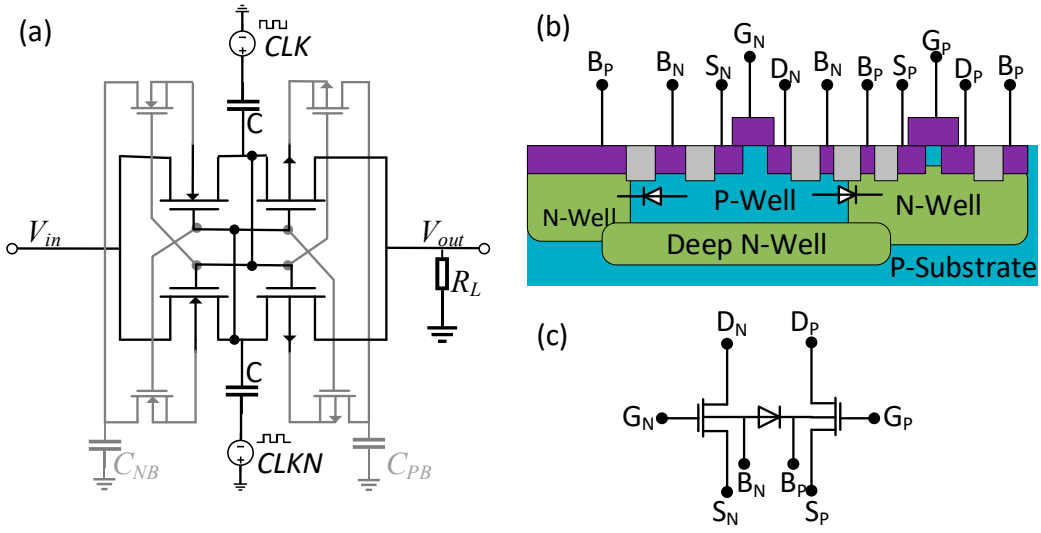

Figure 12. (**a**) Dynamic bulk biasing (in grey) with the charge pump design (**b**) physical implementation to the latch-up (**c**) parasitic diode between the bulk of pMOS and nMOS transistors.

The technique for saving energy during the charging of capacitors C in Figure 11 uses some voltage steps when charge Q is transferred through the virtual capacitor. When the capacitor is charging, the energy delivered, E_{source}, by the voltage source is

$$E_{source} = Q \times V_{in}. \tag{16}$$

During the discharge of the upper and lower capacitors, C, they are connected in parallel to a smaller virtual capacitor to be reused. This helps to decrease power dissipation. In several steps, the energy transferred E_T is given by

$$E_T = \frac{1}{2} C\left(\frac{V_f}{2} - V_i\right)^2 + \frac{1}{2} C\left(V_f - \left(\frac{V_f}{2} - V_i\right)\right)^2 \tag{17}$$

where V_i and V_f are the initial and final capacitor voltage levels. With a combination of power reduction with several-step charging, charge sharing can provide a 50% reduction in energy compared to single-step charging charge pump. The power efficiency η_{PCE} of the CP is

$$\eta_{PCE} = \frac{I_L \,.\, V_{out}}{I_P \,.\, V_{IN}} = \frac{\frac{V_{out}}{V_{in}}}{N + 1 + \alpha \frac{N^2}{N+1+\frac{V_{out}}{V_{in}}}} \tag{18}$$

where $\alpha = \frac{C_{parasitic}}{C_p}$ and C_p is the bottom plate parasitic capacitance. The overall efficiency is highly dependent on the gain factor $\frac{V_{out}}{V_{in}}$ and α.

3. Simulated Results

In this section schematic simulation results of each of the sub-blocks in the PMU with efficiency analysis are detailed to confirm the overall system performance. The PMU subblocks are simulated with Cadence Virtuoso in 180 nm CMOS technology.

3.1. Dual Output Regulating Rectifier

Simulations were performed at various frequencies of 6.78 MHz to 13.56 MHz. The outputs the dual output regulating rectifier for *OUTPUT 1* = 1.8 V and *OUTPUT 2* = 3.3 V with loads of 330 Ω and 1 kΩ, respectively, were recorded

$$VCE = \frac{V_{dc}}{\max(|V_{in\_ac}|)} \times 100\%. \tag{19}$$

The VCE is stable for both outputs. At 13.56 MHz, the regulating rectifier peak value VCE is 94.3% when V_{in_ac} is 3.5 V. The design supports a wide strategy to monitor and adaptively regulate the output voltage levels. The overall PCE, η_{PCE}, of the dual output regulating rectifier is

$$\eta_{PCE} = \frac{P_{out1} + P_{out2}}{P_{IN}} = \frac{P_{out1} + P_{out2}}{V_{AC,rms} \times I_{AC,rms}} \tag{20}$$

where P_{out1}, P_{out2}, and P_{IN} are the output power 1, output power2 and the input power, respectively. The simulated PCE has an average peak of 82.3% at an output power of 40.5 mW. Figure 13 shows η_{PCE} over the ISM frequency band and demonstrates stable voltage outputs.

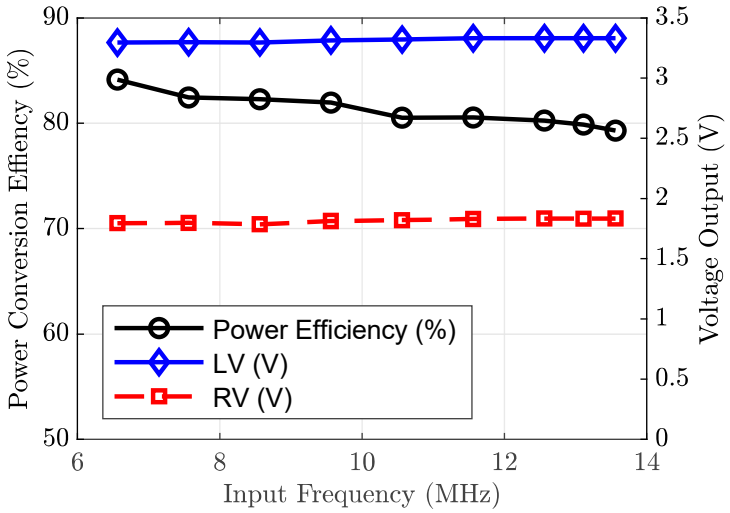

Figure 13. Simulated power conversion efficiency η_{PCE} and voltage outputs at input frequencies within the ISM band range.

3.2. Three-Stage Adiabatic Charge Pump

Figure 14 compares the output voltage of a conventional CP shown in Figure 10 with the adiabatic latch CP's different output currents demonstrating the increased output voltage of the adiabatic CP. The maximum power efficiency is 82.9% at an output current of 102 µA. The output is limited to 12 V to ensure that the transistors in the deep n-well are not damaged when the output current is decreased.

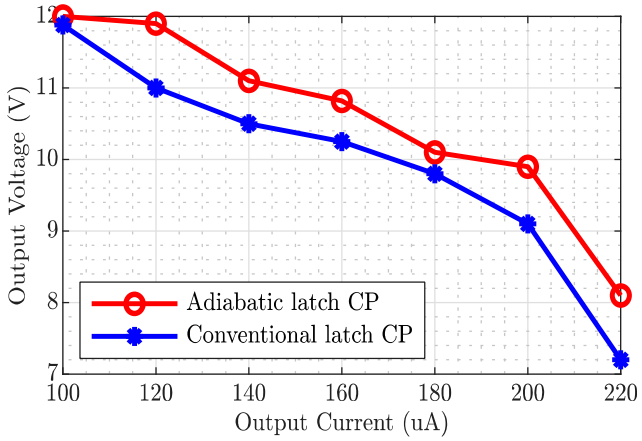

Figure 14. Comparison of the output voltage of the conventional and adiabatic charge pumps for 100 to 220 µA output current. In each, the total capacitance used is 60 pF.

3.3. Overall System Performance and Analysis

The overall PMU performance is shown in Figure 15. The overall PCE of the regulating rectifier and adiabatic charge pump over various power outputs is > 60% using three output voltages of 1.8 V, 3.3 V, and 12 V. The efficiency peaks at around 40.5 mW; total power output of the dual output regulating rectifier and adiabatic charge pump.

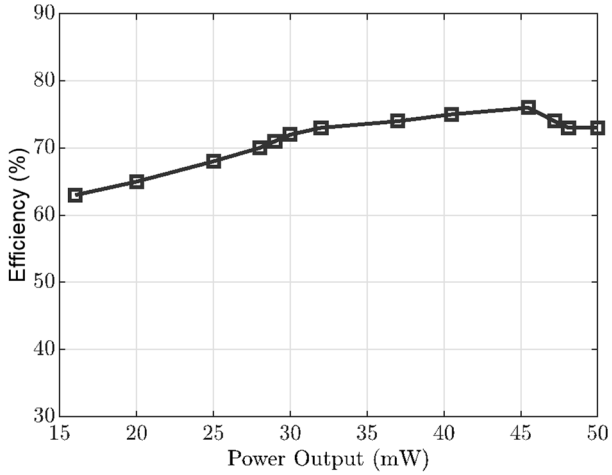

Figure 15. Overall system efficiency of dual output regulating rectifier and charge pump at different output powers.

4. Discussion

The dual output capability of the system in this work has both active rectification and voltage regulation. The PWM and PFM support the simultaneous generation of two independent regulated supply voltages for different functioning blocks from a single input ac voltage V_{ac}. Table 2 compares the performance of the dual output regulating rectifier with state-of-the-art designs. This work has high PCE and VCE compared to previous works. The design works at a higher frequency level and provides higher output voltages. The dual output regulating rectifier topology has the highest VCE compared to designs of other dual output regulating rectifiers. The design operates with a variation of resistive loads, $R_{L1,2}$ of 330 Ω to 1 kΩ compared to state-of-the-art designs.

Table 2. Comparison of dual output regulating rectifier designs.

	[29]	[30]	[31]	[32]	**This Work**
Process (nm)	180	180	180	180	180
Freq. (MHz)	13.56	0.0125	1	1–10	13.56
V_{in_ac} (V)	1.35~1.8, 2.15~2.8	1.6~2	NA	1.5~2.5	1.5–3.5
Regulation Topology	Delay-based Rectifier	SSDO Tri-mode	Voltage power Reg.	Regulating Rectifier	Regulating Rectifier
V_{dc} (V)	3.12	3.6	1	1.5–2.5	1.8–3.3
$R_{L1,2}$ (kΩ)	0.5	0.2,1	8	0.1	0.33–1
$P_{out, Max}$ (mW)	10	114	4.7	65	40.5
VCE (%)	82.2	NA	92	75.8	94.3
PCE Peak (%)	79	91.7	75.3	90.75	82.3

The adiabatic charge pump performance is compared to previously proposed charge pump designs in Table 3. It has much higher overall efficiency compared to other designs with maximum power of 40.5 mW, eliminating the reverse current paths from the output to the input direction to avoid voltage loss.

Table 3. Comparison of charge pump designs.

	[33]	[34]	[35]	[36]	[37]	[38]	[22]	This Work
Process (nm)	130	65	65	65	130	180	130	180
Topology	Linear	Linear	Boot-Strap	Dickson	Bootstrap	Bootstrap	Adiabatic	Adiabatic
No. of Stages	6	3	10	4	3	3	7	3
Clock Freq (MHz)	0.040	15.2	10	1.8	0.8	86.1	0.36	10
Total Cap. (pF)	46.08	22.5	1001	160	150	400	100	60
Load current (µA)	12	1.74	0.76	10	5	500	0.1	100
Max power (µW)	15	1.5	6.6	4.7	7	3675	0.035	1200
PCE (%)	58	38.8	33	66	58	69	59–62	82.9

5. Conclusions

A high-efficiency battery-less integrated PMU that consists of a dual output regulating rectifier and an adiabatic charge pump with low power consumption has been designed. The theoretical analysis and analytical modeling of the power transfer system for biomedical applications have been presented. The circuit design, equations, and design steps are highly flexible and well-suited for other IoT applications. The regulating rectifier provides dual output voltages of 1.8 V and 3.3 V used in many applications. The peak efficiency of the system can reach 82.3% when the power output is 40.5 mW.

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