Low-cost high gain MoS$_2$ FETs from amorphous low mobility film precursors

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ABSTRACT: With the aggressive invasion of Thin Film Transistors (TFTs) in the rapidly altering/disposable portable electronics, displays, smartphones and wearables market, cost reduction has evolved into a challenge as much as electrical properties' improvement. Therefore, it is not surprising that processes requiring expensive equipment and energy-intensive processes are abandoned in favor of Room Temperature (RT) approaches, liquid phase deposition and colloids. Despite being cheaper, the latter suffer from controllability, performance and large contact resistance issues, deteriorating the quality of the final product. To meet the trends while

not compromising the performance, we fabricate a MoS$_2$-based ionic liquid gated TFT with ON-current of 1.5×10^4 A for holes and a field effect mobility of 64.3 cm^{2}V^{-1}s^{-1} at RT in a hybrid liquid-solid state 3D topology utilizing low energy expenditure impurity tolerant processes. The device addresses the weakness of unattainability of P-type conduction in MoS$_2$, thereby extending its pertinency to PN diodes and complementary integration logic. In addition, photo-enabled switching and memory functionality is demonstrated and detailed material and electrical properties are investigated. The herein presented advanced architecture is, to our knowledge, the first low-cost high gain MoS$_2$ metal-oxide-semiconductor field-effect transistor (MOSFET) based on amorphous low mobility film precursors that enables high-performance multifunctional stackable MOSFETs on any kind of processing-sensitive, plastic and/or flexible substrate.

1. Introduction

Transition Metal Dichalcogenide (TMD) semiconductors offer unique advantages when incorporated into field effect transistors (FETs) in their atomically thin form. Their high transparency, high mobility values and mechanical flexibility make them ideal candidates for use in high performance transparent and flexible electronics, provided they reside in the form of single or few layers [1, 2]. The latter is crucial to promote electrostatic gate control of the channel [3] and to eliminate short channel effects [4]. However, crystalline monolayer TMDs are challenging and expensive to achieve and/or involve small-scale poor-yield processes [5], like mechanical exfoliation, hindering mass production. On the contrary, amorphous bulk TMDs are directly accessible from vapors [6] utilizing large scale, low cost and low energy consumption deposition techniques like hot wire chemical vapor deposition (HW-CVD) at RT.

Amongst semiconducting TMDs, molybdenum disulfide (MoS_2) is one of the most popular due to its natural abundance and excellent environmental stability [7]. Hence, its potential in numerous electronic and optoelectronic device applications, including flexible FETs [8], photovoltaic cells [7], photodetectors [9], sensors [10], logic circuits [11], and memory cells [11], has been extensively investigated over the last years. However, MoS_2 FETs still suffer from large contact resistance due to Schottky barriers formed at the metal/MoS_2 interface as well as due to interlayer resistance [3] and, even in their crystalline form, experience extrinsic mobility issues [12], such as charged impurity scattering, detrimental for applications. In order to alleviate contact resistance issues, low work function metals and N-type charge transfer dopants have been investigated by several groups, but the contact resistance did not exhibit momentous reductions at RT (being reduced by a factor of ~3 in the first case (i.e. from 3.3 kΩ·µm to 1.1 kΩ·µm) and by a factor of ~2 (i.e. from 56.61 kΩ·µm to 26.65 kΩ·µm) in the second) and only moderate channel mobilities (of the order of 24.7 $cm^2V^{-1}s^{-1}$) were achieved with these methods [13, 14]. Considerable work has also been done in other directions, such as dielectric engineering, utilizing high-k materials to electrostatically reduce impurity scattering in MoS_2 devices [15, 16].

In this work we demonstrate an alternative path to competitive flexible MoS_2 devices, namely, shaping and using on-site high-performance hybrid (liquid/solid state) MoS_2 channels directly inside amorphous precursors of relative impurity. To achieve this, a processing protocol involving low thermal budget annealing and ionic liquid doping is developed and applied. The active channel is shaped while being engraved in a multifunctional precursor matrix consisting of amorphous MoS_2 including MoO_x and non-bound sulfur species as well as an ionic liquid filler. The latter serves simultaneously as gating medium, ionic dopant and passivation layer for the

channel. This way, an air stable self-encapsulating high mobility P-type channel is being formed, making this approach effective facile and scalable.

With this technique, we achieve a low-lying contact resistance (R_c) of 2.6 kΩ·μm, which competes with the R_c values obtained on monolayer MoS_2 with engineered contacts [17]. A high ON-current of 1.5×10^4 A (normalized ON-current 1.25×10^{10} A/m) for holes is achieved at room temperature in air for a 5 μm channel length liquid-gated FET at 2 V drain-to-source voltage (V_{DS}) and no back-gate overdrive. The low voltage field-effect mobility (μ_{FE}), determined to be 1.93×10^{-7} $cm^2V^{-1}s^{-1}$ in the annealed back-gated MoS_2 devices, is being boosted more than eight orders of magnitude to values as high as 64.3 $cm^2V^{-1}s^{-1}$ for the liquid-gated topology, competing with the mobilities of high quality polysilicon TFTs [18, 19], that of the most competitive OFETs [20, 21, 22, 23], dielectrically screened monolayer MoS_2 [24] and graphene/MoS_2 heterointerface FETs [25], thereby paving a new way for fabricating high performance low cost flexible FETs. Electrical, spectroscopic and structural characterization as well as theoretical modelling using the finite element method are performed in order to gain further insight into the nature of MoS_2 physical and structural changes upon the utilized low thermal budget annealing as well as into the ionic liquid/MoS_2 hybrid on-site channel formation and operation mechanisms.

2. Results and Discussion

SPECTROSCOPIC AND STRUCTURAL CHARACTERIZATION

MoS$_2$ films intended for FET channels are grown via RT HW-CVD [26]. In their unprocessed, as grown form they are a low conductivity low mobility 46 nm-thick porous medium, as deduced from electrical measurements, spectroscopic ellipsometry (SE) and Scanning Electron Microscopy (SEM) (see corresponding subfigures of Figure 1 and ELECTRICAL CHARACTERIZATION section). The long range amorphicity of the films is confirmed via X-ray diffraction (XRD) and Raman spectroscopy (Figure 1), as well as from UV-vis absorbance (see Figure S1 in Supporting Information). The latter indicates absence of the excitonic A and B bands at 670 and 610 nm, which constitute the typical fingerprint of ordered 2H-MoS$_2$ structures [27], showing only transitions from the valence to the conduction band around 400 nm that, additionally, appear broad due to extended structural disorder [28]. From SE measurements' analysis the as-grown material bandgap is estimated to be 1.27 eV with no characteristic peaks or features in their spectral refractive indexes (Figure 1a), suggesting a bulk-like, amorphous material with indirect gap.
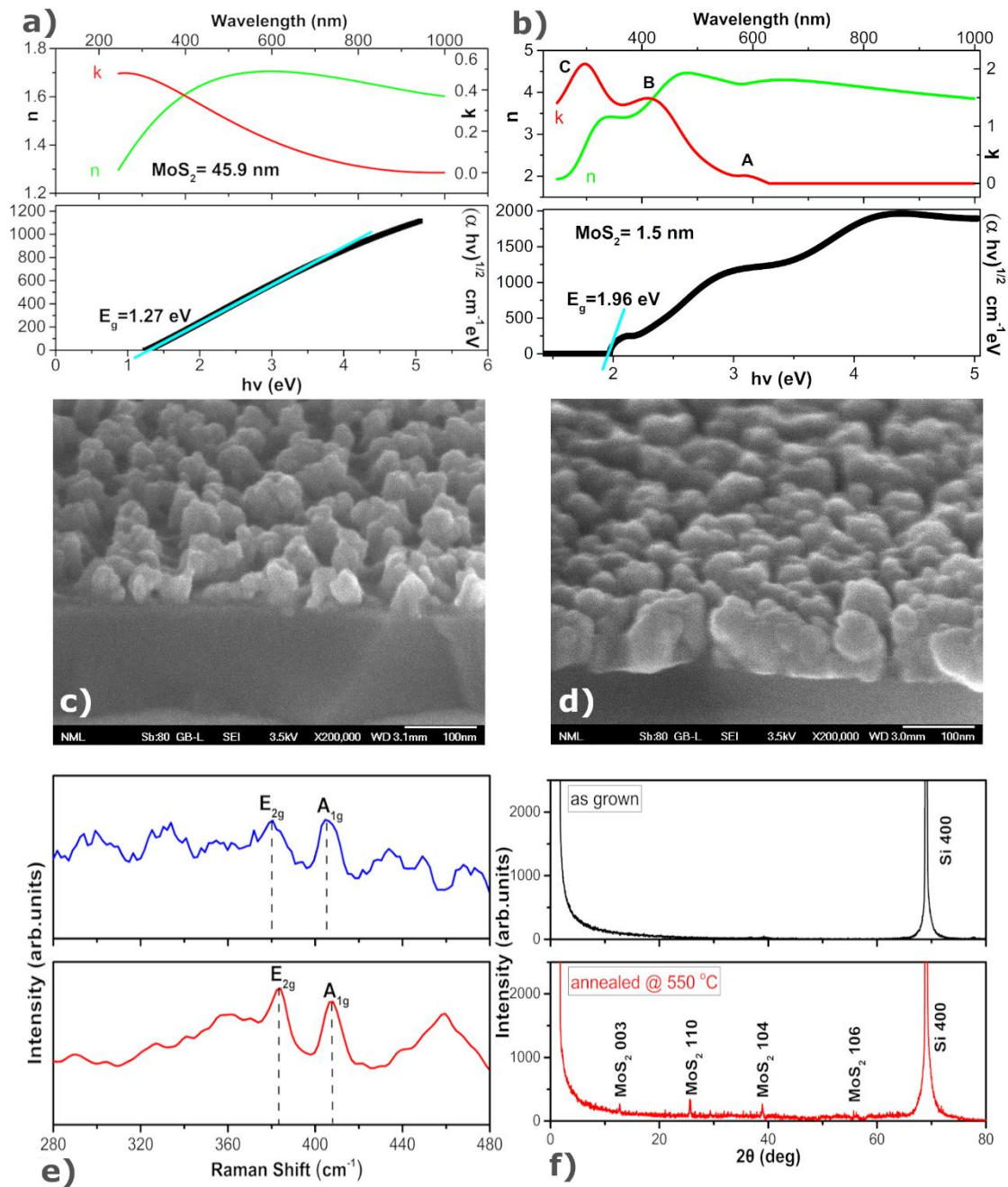
Figure 1. a) top: Experimentally determined MoS_2 complex refractive index (n, k) as derived from spectroscopic ellipsometry data analysis. bottom: extracted Tauc plot along with the corresponding MoS_2 bandgap (E_g) for the as-grown film and b) same data for films annealed at 550ºC. c) FE-SEM image of as-grown and d) FE-SEM image of annealed MoS_2 film, highlighting material migration along the growth axis (z-axis) upon thermal treatment. e) typical

Raman spectra of the as grown (blue) and annealed (red) MoS$_2$ thin films demonstrating the MoS$_2$-characteristic E$_{2g}$ and A$_{1g}$ peaks at 383,8 cm^{-1} and 408 cm^{-1}. The peaks become more intense and narrower upon annealing (at 550°C, under N$_2$, for 5min), highlighting an overall transition from amorphous to a crystal-like structure. f) XRD spectra of as grown (black) and annealed (red) MoS$_2$ films highlighting a transition from amorphous to multi crystalline material upon annealing, in accordance to Raman spectra.

However, after a mild annealing treatment at 550°C (5 min, N$_2$) the complex refractive index of amorphous MoS$_2$ (Figure 1a) is transformed to the information-rich case of Figure 1b, the result of which is consistent with published results for crystalline MoS$_2$ [29]. The three peaks in the spectral indexes of Figure 1b correspond to the A, B, and C excitons of the dielectric function, with the A and B peaks related to the transition from the spin-orbit split valence bands to the lowest conduction band at the K and K' points and the C peak associated with the transition from the valence band to the conduction band along the $\Lambda \rightarrow \Gamma$ path of the Brillouin zone [29, 30]. The ellipsometrically-determined bandgap is also increased after annealing to 1.96 eV, a value consistent with the direct bandgap dominant in mono- or oligo-layer MoS$_2$ and MoS$_2$ nanosheets [31, 32, 33] and concerns the bottom layers of the structure, remaining covered by the amorphous MoS$_2$ matrix as confirmed via the XRD and SEM images of Figure 1. The latter indicate a more coherent structure at the bottom of the film which evolves into a highly porous formation of increasing pore size towards the film top.

The surface chemical composition of the films was analyzed using X-ray photoelectron spectroscopy (XPS). The survey spectra (see Figure S2 in Supporting Information) show the expected Mo and S core and Auger lines for MoS$_2$, along with signals from C and O and smaller signals from S, F and Na. Analysis of the Mo 3d (Figure 2(a)) and S 2p (Figure 2(b)) core level

spectra reveal the presence of MoS_2 as well as significant amounts of additional sulfur species (S-H/N). The Mo $3d_{5/2}$ binding energy (BE) is found to be 229.7 ± 0.1 eV and the Mo $3d_{3/2}$ BE is 232.9 ± 0.1 eV, resulting in a spin-orbit-split (SOS) of 3.2 eV, all consistent with values previously reported in the literature for MoS_2 [34, 35, 36]. The Mo 3d core level is very close in BE to the S 2s line [34] and two chemically shifted components are observed at 225.9 ± 0.1 eV (MoS_2) and 227.9 ± 0.1 eV (S-H/N), with the higher BE component dominating. This is also reflected in the main S 2p core line showing a main component at 163.7 ± 0.1 eV from S-H/N environments and a smaller feature at lower BE (162.6 ± 0.2 eV) associated with MoS_2 [34].

In the Au-free spectra of Figure 2a, 2b the contribution of annealing can be isolated. Spectra suggest a shift to lower BE for both Mo 3d (Figure 2a) and S2p (Figure 2b) spectral components from MoS_2 upon annealing, indicating a rigid shift of the Fermi level, thereby suggesting the thermally-induced P-type doping of the MoS_2 matrix [37].

Minute amounts of Mo oxides are also observed in both the Mo 3d and O 1s spectra (Figures 2(a) and 2(c), respectively). The O 1s spectra may suggest a slight increase in the level of oxidation for the annealed sample with Au electrodes, in possible accordance with the observation reported by Salazar et al. that Au causes the reduction of precursor MoO_x species used in MoS_2 growth, leading to the appearance of Mo in several different oxidation states and influencing the sulfidation and growth of layered MoS_2 structures [38].

MoS_2 strongly interacts with Au itself, inducing N-doping to the portion of MoS_2 that is in close contact with the metal while remote portions remain undoped [39]. The phenomenon is more pronounced in the case of annealed samples and appears as a shift of the Au4f doublet to higher BE from the energy window commonly reported for pure gold consequent to contact with

MoS₂ and a further 0.3 eV shift to higher BE upon annealing of the Au-MoS₂ system. Possible

formation of Au–S bonding could also contribute to this shift to higher BE [40] with both

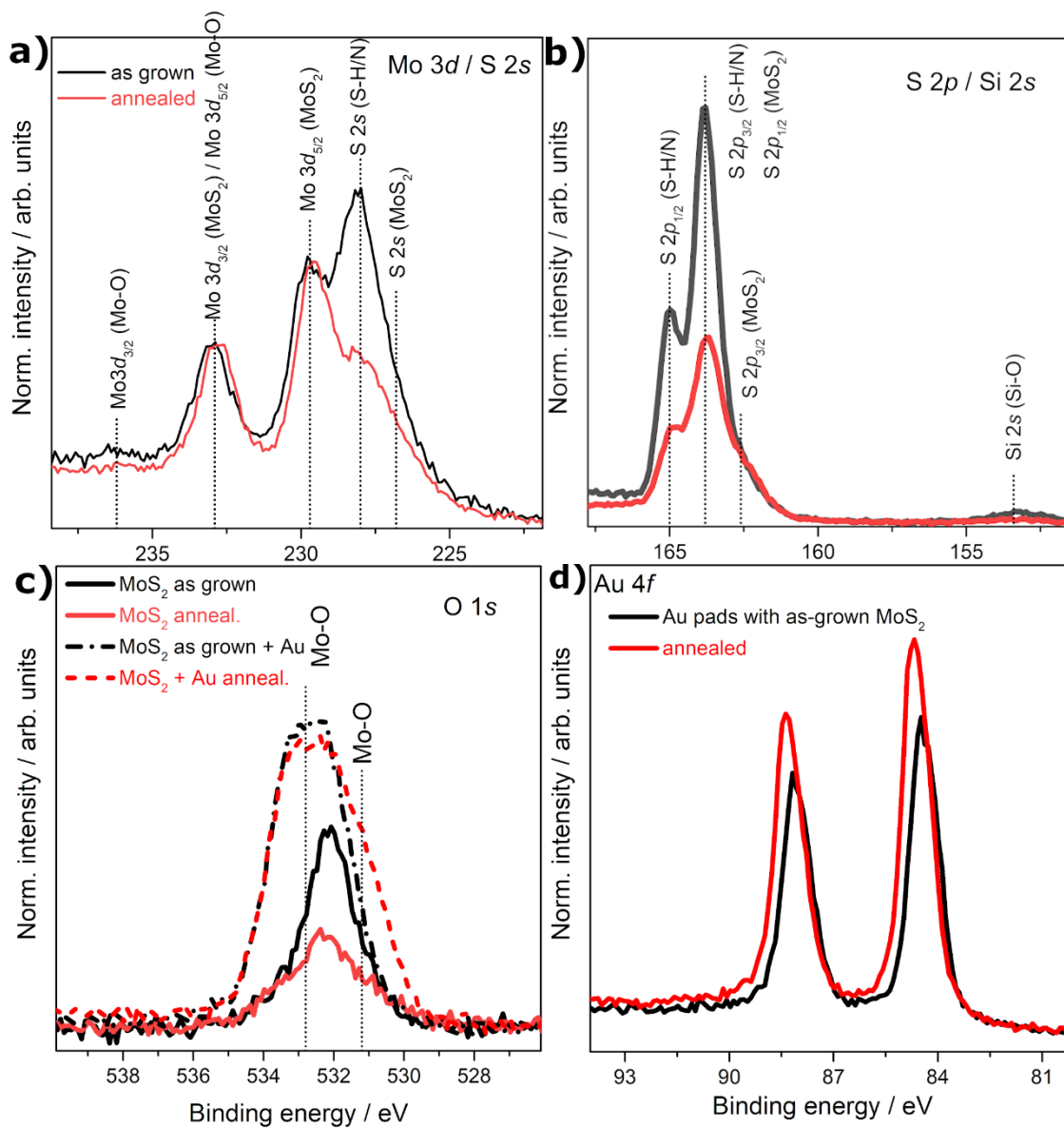mechanisms acting to enhance electrical conduction between MoS₂-bridged Au contacts.

Figure 2. a) Mo 3*d* and S 2*s*, b) S 2*p* and Si 2*s*, c) O 1*s* and d) Au 4*f* XPS core level spectra

collected for as grown MoS₂ and the film after annealing at 550ºC as well as for films deposited

on Au-equipped chips. S 2s and S 2p contributions to signal are being highlighted to enable better visualization of energy shifts between sample signals.

For as grown samples a small Si 2s signal from the Si substrate is visible (Figure 2(b)), that is in agreement with the porous nature of the films observed in SEM (see corresponding subfigures of Figure 1). This peak is significantly weakened upon annealing, due to material migration and structural rearrangement of the films. This becomes clearer with the aid of the SEM topographies of Figure 1, where annealing is shown to induce material migration along the growth axis leading to the formation of a robust oligo-layer bottom followed by a porous surface away from the SiO_2/MoS_2 interface.

ELECTRICAL CHARACTERIZATION

Comparison of in-plane and vertical (across growth axis) I-V characteristics of as grown films (Figure 3) indicate a highly anisotropic material in electrical terms, with the vertical axis exhibiting more than seven orders of magnitude higher conductivity. This is not surprising, since the films are effectively an MoS_2/air composite on plane (see SEM topographies of Figure 1). As expected in such cases, conduction between source and drain occurs via tunneling, the most-common conduction mechanism through insulators under adequately high fields [41]. Utilizing the Transfer Length Method (TLM) [42] on Figure 3 data the contact resistance of the as-grown MoS_2 film is estimated to be Rc= 200.86 GΩ·μm. The value owes to the presence of high degrees of porosity, apparent in both planar and cross-sectional FE SEM images of as-grown films (see corresponding subfigure of Figure 1), that increase overall resistivity values [43]. Naturally, such a structure cannot serve as-is as a FET channel, with the resulting devices

exhibiting I_{SD} independent of the applied V_{SG} in both top and back gate configurations up to the

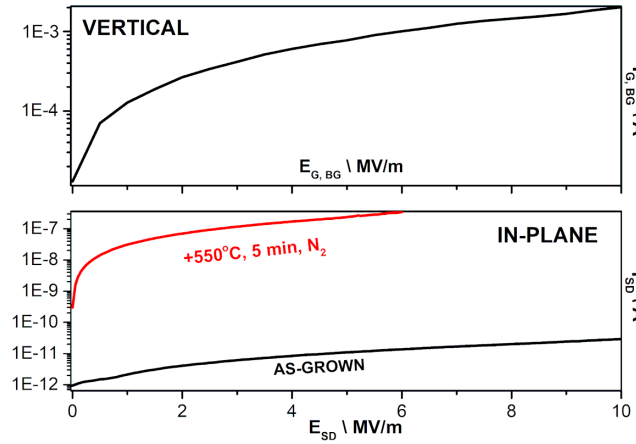top oxide (Al_2O_3) and bottom oxide (SiO_2) breakdown voltages.

Figure 3. Vertical (along the growth axis, obtained through point contact) (top) and planar,

between 5μm-spaced parallel overlapping Au on Ti contacts of 60 nm thickness and 100μm

overlap (bottom) I-V characteristics of HW-CVD MoS_2 films.

The comparative advantage of these films lies in their low cost, straight forward fabrication

simplicity, and compatibility with standard fab-line processes and temperature-sensitive

substrates. They are, therefore, utilized in this work as an amorphous, albeit stoichiometric,

precursor material pool, where the actual channel is post-schematized on site in a lithography-

free manner.

For this purpose, the reduction of contact resistance and refinement (but not elimination) of

porosity are desirable. To that end film deposition is followed by a 5 min post growth annealing

at 500ºC under a N_2 environment with the film left to reach RT without active cooling. This mild

thermal treatment does not remove porosity and has the extra merit of inducing electrically-

beneficial structural rearrangement of the MoS_2 matrix along with non-substitutional doping, in

the close vicinity of the Au electrodes (see Figures 1, 2 and corresponding analysis) resulting in the enhancement of planar conductivity by approximately five orders of magnitude (Figure 3, bottom graph). Further annealing and/or other higher thermal budget treatments would disrupt this scheme, having detrimental impact on planar conductivity.

In the case of 5 min annealed films TLM provides a value of Rc=14.14 MΩ·μm, four orders of magnitude lower than the initial Rc value. Planar mobility is also dramatically improved and, as a result, an active functional channel in the SiO_2/MoS_2 interface is now obtained with gate control under global back gate configuration in the limit of long overlapping S, D electrodes with 1 mm overlap (W) and decreased 1 μm spacing (L) (see Figure 4). An inappreciable leakage current of the order of pA is observed through the $Au/SiO_2/Si/Au$ back-gate stack at the biasing conditions used to obtain transfer characteristics.

The I-Vs acquired in Figure 4 permit the extraction of characteristic MOSFET parameters like mobility in the linear regime, $\mu_{MoS2, linear}= 1.93\times10^{-7}$ $cm^2/(Vs)$. The value is still restrictively low for high performance FET operation with the device exhibiting a transconductance of 3.4 μS. The manifested threshold voltage is extremely high (-68 V), while the expected saturation regime V_{SD} voltages reside far above + 68 V. In addition, the device displays very high off current of the order of 52 nA, which cannot be lowered via the application of back gate voltage.
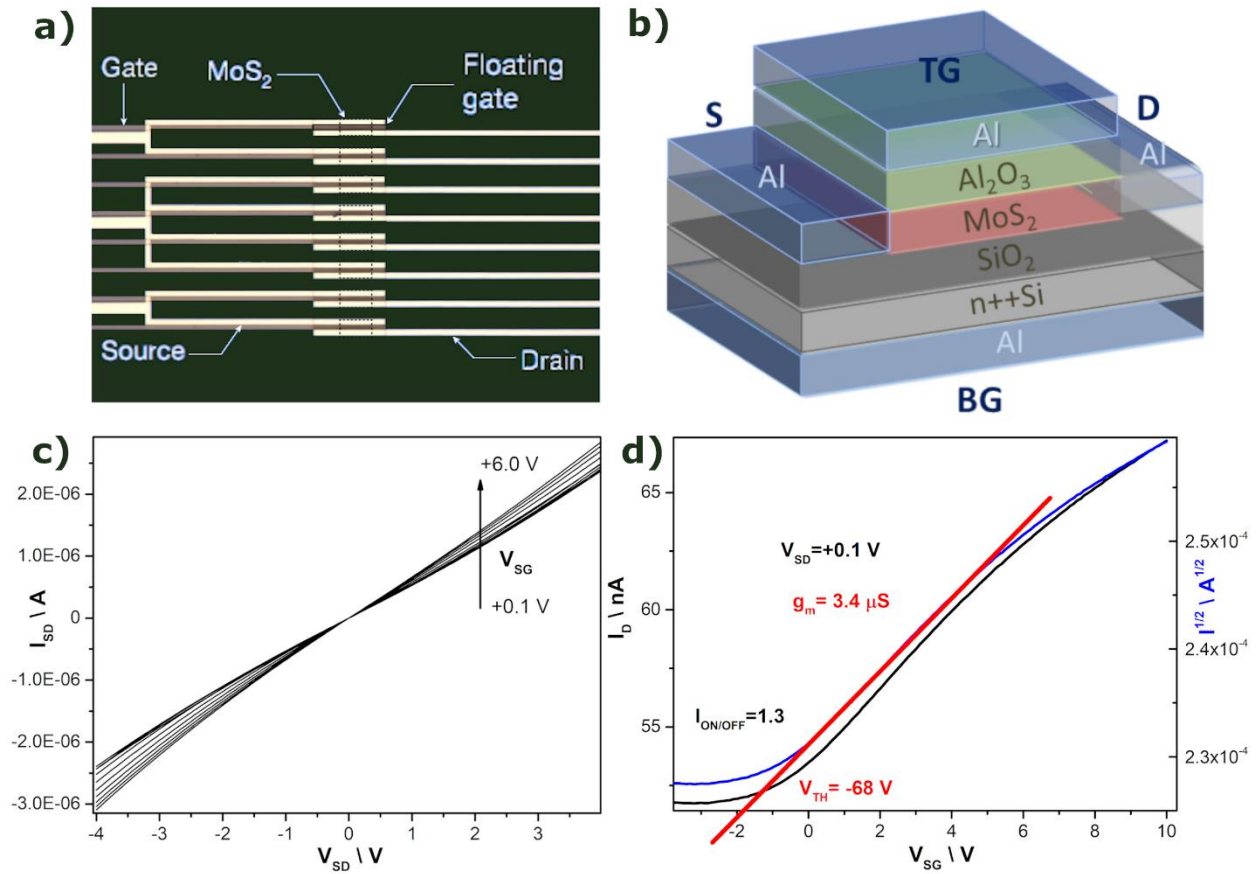
Figure 4. Contacts (a), active area stack schematics including top gate electrode (TG), source (S), drain (D) and global back gate electrode (BG) (b), and corresponding output (c) and transfer (d) characteristics of annealed MoS$_2$ films between 5 μm-spaced parallel overlapping contacts.

From split C-V measurements (see Figure S3 in Supporting Information) [44, 45], considering a 46 nm-thick MoS$_2$ film covered with a 30 nm Al$_2$O$_3$ (ε=9.8) gate oxide, the dielectric constant of MoS$_2$ is determined to be ε_r=28, in accordance with the value predicted for crystalline multilayer MoS$_2$ [46]. The result is consistent with the detected crystallization trend upon annealing at 550°C (Figures 1b, 1e, 1f) most pronouncedly in the Au contacts and channel vicinity, in accordance with the SE results (Figure 1b).

LOCAL CRYSTALLIZATION AND ON-SITE LITHO-LESS CHANNEL FORMATION

Besides the mean crystallization status probed via spectroscopic characterization, local crystallization information is also crucial for the investigation of inhomogeneous/nanopatterned samples and can typically be obtained via cross-sectional transmission electron microscopy (TEM) and selected area electron diffraction (SAED). However, determining nm-layer crystallization through TEM is challenging, and possibly misleading, since e-beam irradiation is a common source of recrystallization and information disruption in ultrathin or nanocrystalline films [47].

Therefore, a non-invasive indirect approach is followed to investigate the development of randomly oriented nm to μm crystallization domains in the MoS_2 film, especially in the near electrode vicinity, which is critical for electrical performance. The detailed conditions leading to the speculated local charge doping in the channel area are also of particular interest and should be determined. For this purpose, the thermally treated MoS_2 film is simulated and quantitatively visualized using the COMSOL Multiphysics 5.1 cross-platform finite element analysis solver and physics simulation software. Heat transfer across the substrate-electrode-MoS_2 stack is modelled for thermal annealing at $550^{\circ}C$ utilizing a hot plate bottom heater configuration and accounting for conduction, convection, and radiation. The model solves the differential form of Fourier's law in the topology domains with the system residing at ambient temperature. The MoS_2 layer is incorporated as a porous medium and the problem is solved using cylindrical symmetry for computational economy purposes. The results are presented in Figure 5 in surface (Figure 5a) and isosurface (Figure 5b) representations along with real chip FE-SEM images of the MoS_2 and MoS_2 on Au film before (Figure 5c) and after (Figure 5d) annealing to demonstrate the relevance of results.
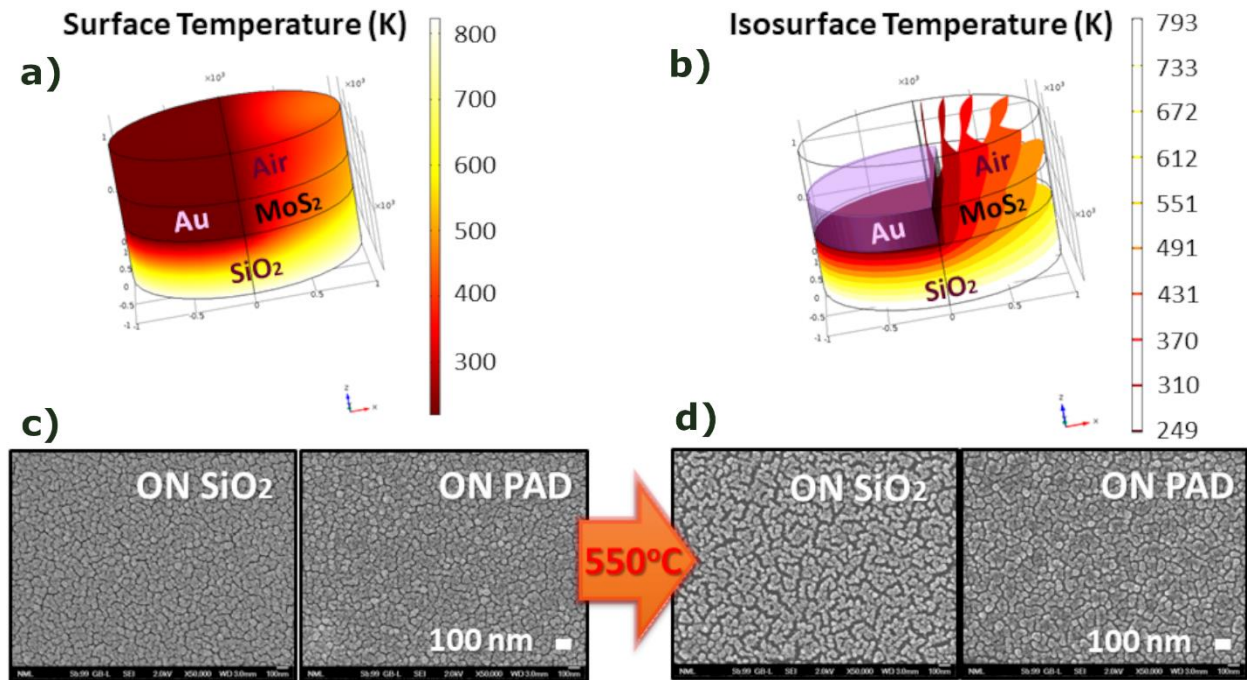
Figure 5. a), b) Stationary solutions of the heat transfer problem across the substrate-electrode-MoS$_2$-air stack upon heating the base at 550°C and introducing the structure in RT conditions. The thermal conductivity of SiO$_2$ is taken to be 1.3 W/mK, while the cross-plane thermal conductivity of the naturally occurring MoS$_2$ is calculated to be 3.5 W/mK at room temperature. Au electrodes have been assigned a thermal conductivity of 310 W/mK at 20°C. c) FE-SEM images before annealing and d) after annealing on MoS$_2$ grown on substrate and on Au pad highlighting Au impact on thermal status.

Figure 5 demonstrates that the utilized thermal treatment has differential impact on the various regions of the MoS$_2$ film, developing with the creation of discrete "cooler" zones in the near electrode vicinity and "hotter" zones towards the channel's center with effective local temperature at any point of the MoS$_2$ matrix resulting from the energy balance between local atom heating and heat dissipation into the electrodes [48]. This eventually leads to heat accumulation in the regions between electrodes (i.e., across the channel) favoring local

crystallization of the source-drain channel region. Additional heat may be developed at the centers of the interelectrode regions through thermal runaway, a positive temperature feedback effect of a system with higher heat generation than effective cooling [49], not considered in the current model, since crystallization is an exothermal process. It has been previously reported [50] that low-temperature (below 453 K) thermal treatments result in 1T crystal phase structures in MoS_2, while high-temperature ones (above 483 K) result in 2H MoS_2 structures along with crystal quality improvement and reduced defect sites. Existence of the 1T phase in the near electrode vicinity could further improve charge transfer ability [50] adding to the development of N-type regions in the previously P-type MoS_2 channel as explained above.

Moreover, the in-plane thermal conductivity of MoS_2 has been reported to take values between 13-45 W/mK [49], i.e., more than three times that of the out-of-plane value, meaning that heat flow through crystallized paths is favored, eventually leading to self-sustained directional thermal flow within the MoS_2 bulk (not included in the current model) during heating.

The herein documented N-type doping of the near contact vicinity results in the formation of a P-N junction in the previously P-type MoS_2 channel. The phenomenon is validated electrically via planar C-V characteristics and can be found in Figure S4 of Supporting Information along with the corresponding quantitative and qualitative characteristics of the junction.

FROM GATES TO LIQUID GATES AND GATE MATRICES

In order to attain high mobility FET channels, a biphasic liquid-gated field-effect transistor is realized as a means to improve mobility while steering clear of high-cost, high-energy growth and processing steps. To achieve such a scheme, the annealed MoS_2 matrix is used as a

topological ionic attractor through which positive mobile ions from the liquid phase are introduced to the channel zone and become available for FET function.

For this purpose, a μm-diameter droplet of copper phthalocyanine [52] / butanol (CuPc/bu) ionic liquid (details can be found in the Supporting Information) is placed onto an MoS_2 FET device of global backgate topology and exposed channel matrix (Figure 6a). The ionic liquid droplet acts as both a top gate and a top dielectric [53, 54] through the formation of an electric double layer as schematically depicted in Figure 6a.
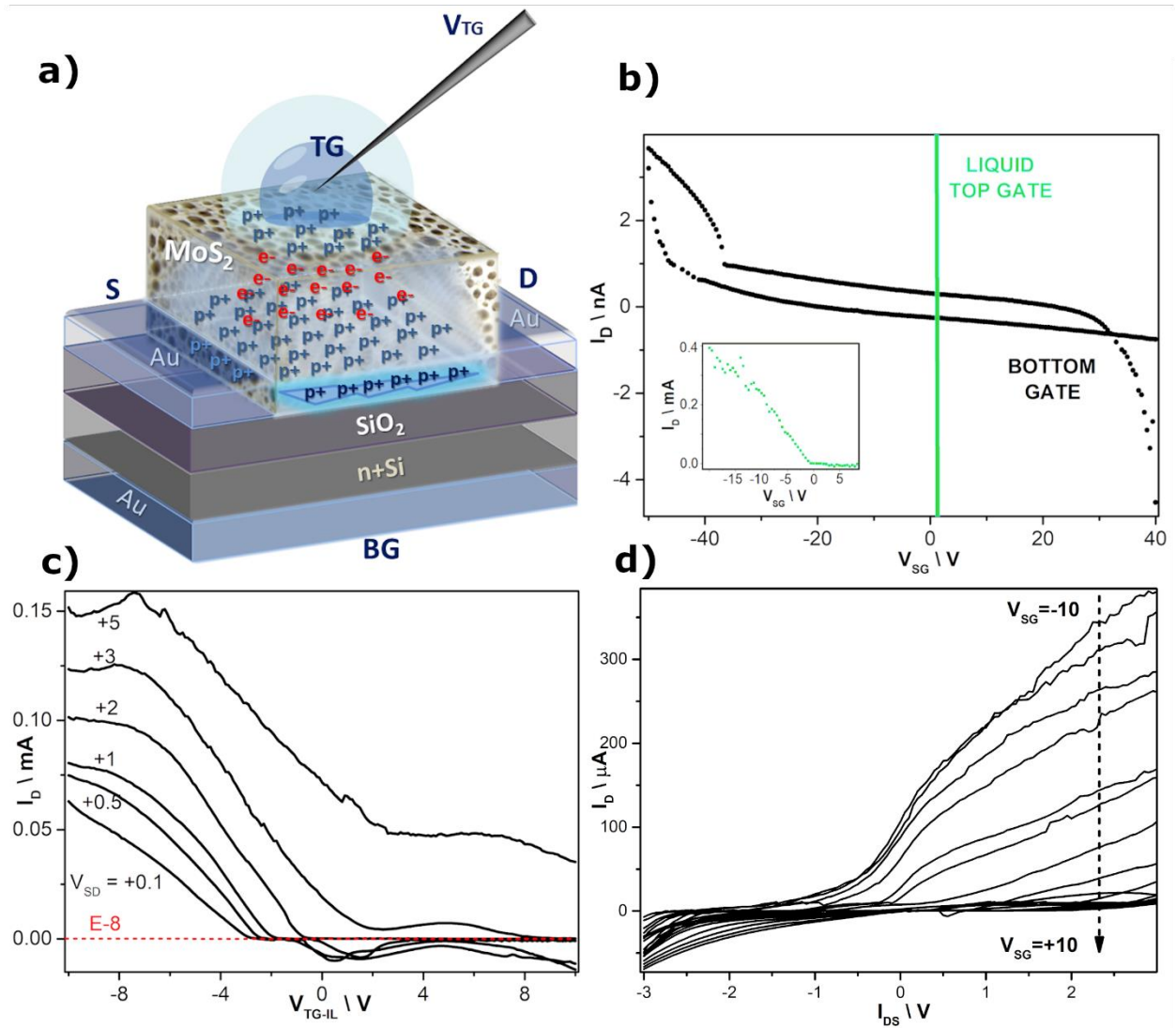
Figure 6. a) Schematic of the formation of an electric double layer b) DC characterization of a hysteresis loop for amorphous HW-grown MoS_2 transistors showing clear evidence of electron trapping and de-trapping during a full BG sweep (black curve). Transfer characteristics of the same device in CuPc/bu IL-top gated configuration in P-type operation (cyan curve). c) Transfer characteristics of the liquid-gated amorphous MoS_2 transistor for V_d varying from linear operation regime (V_d= 100 mV) to saturation. d) Respective Output characteristics.

While the ionic conductivity of pure water or n-butanol is low (ca. 50 μS cm^{-1} [55] and 0.07 μS cm^{-1} [56], respectively, at 25°C), the situation of the same liquids in a doped porous matrix can turn out to be quite different owing to the electric double layer (EDL) charge. An ultra-thin 1-2 nm EDL is created at the doped MoS_2-liquid interface [57] that serves as a high-capacitance dielectric material [58] ideal for field-effect devices. EDLs formed at solid–electrolyte interfaces are able to induce extremely large electric fields, thereby resulting in a high charge carrier accumulation in the solid, much more effectively than solid dielectric materials [58]. Moreover, under the conditions of large internal surface area of the porous matrix and small pore size, the volume-averaged total ionic concentration of the liquid in the matrix may be further increased [55], producing the characteristics of Figures 6c, 6d.

In order to protect the CuPc/bu droplet from evaporation in ambient conditions, an orthogonal solvent solution with both high boiling point and high adhesion to the substrate, namely 6% polymethyl methacrylate (PMMA) in propylene glycol methyl ether acetate (PGMEA), is deposited as a liquid capping layer on top. An electrochemically inert platinum-coated tip is then immersed into the droplet through the capping layer to externally address the liquid electrode.

Applying a negative bias to the top liquid gate electrode results in the migration of positive ions towards the immersed Pt-coated needle, whilst negative ions are accumulated near the EDL to counterbalance the created field. This induces an accumulation of holes in the vicinity of the doped MoS_2 channel, creating an abundancy of positive mobile ions at the interface between the MoS_2 and the ionic liquid, thereby forming an increased mobility P-type channel. The transfer curve of the liquid-gated MoS_2 transistors is shown in Figure 6c.

An I_{on}/I_{off} ratio of $\approx 10^4$ is obtained, whilst retaining, however, a high off-state current of $\approx 10^{-8}$ A, due to poor gate control of the MoS_2 matrix. Compared to the precursor MoS_2 devices of Figure 4 the addition of the ionic liquid gate radically improves the device performance; the conductance increases by a factor of 10^3 or 10^4. Mobility also increases by more than eight orders of magnitude to 64.3 cm^2/(Vs).

The dramatic improvement in conduction induced by the mere presence of the IL (even without gate voltage application) suggests that it screens and lowers the Schottky barrier at the metal-semiconductor interfaces, which constitutes a major conduction bottleneck [59] in the fabricated devices. The improvement in mobility indicates that charged impurities are also screened by the IL, reducing carrier scattering while also providing mobile charge carriers. By using a highly porous large effective surface area MoS_2 matrix, ions can accumulate in all three dimensions of the MoS_2 channel, enabling higher doping levels than what could be obtained in bulk or two-dimensional materials.

From the output characteristics of Figure 6d it is calculated that $I_{SATURATION} = 4\times10^{-4}$ A for V_{GS}=-9 V. From a $I_{SD}^{1/2}$ Vs V_{SG} plot the V_{TH} is estimated to be -2.49 V, transconductance g_m=2.4 mS, and linear mobility is found to be $\mu_{MoS2,linear}$= 64.3 cm^2/(Vs). Utilizing the TLM a value of

2.6 kΩ·μm is retrieved for the contact resistance, a record low competing with CR values obtained for 2–3-layer crystalline MoS_2 with phase engineered contacts [17]. The total resistance of the fabricated Au-hybrid-Au channel configuration falls in the range of 12.7 kΩ·μm, thus contact resistance accounts for 20% of the total resistance.

As can be observed from the transfer characteristics of Figure 6c the threshold voltage is shifted to more positive values with increasing V_D in a monotonic manner, a fact presumably originating from the progressively increasing availability of mobile dopants with increasing top gate field. Dopant concentration naturally affects both oxide voltage drop and depletion layer voltage drop [60, 61], thus increasing overall V_{TH}. Mobility, however, is not significantly affected (see Figure 6c) since the main limiting factor determining its value is scattering, mainly ionized impurity scattering, scattering with MoS_2 lattice phonons, and surface roughness scattering in the channel region, which is a MoS_2 quality-related phenomenon for sufficient concentrations of mobile ions in the ionic liquid (IL).

Owing to the fact that CuPc is an intensive UV-Vis light absorber [52], the CuPc-containing IL top gated configuration can naturally realize photoswitching (Figure 7a) as well as non-volatile memory functions (Figure 7b) in a single cell.
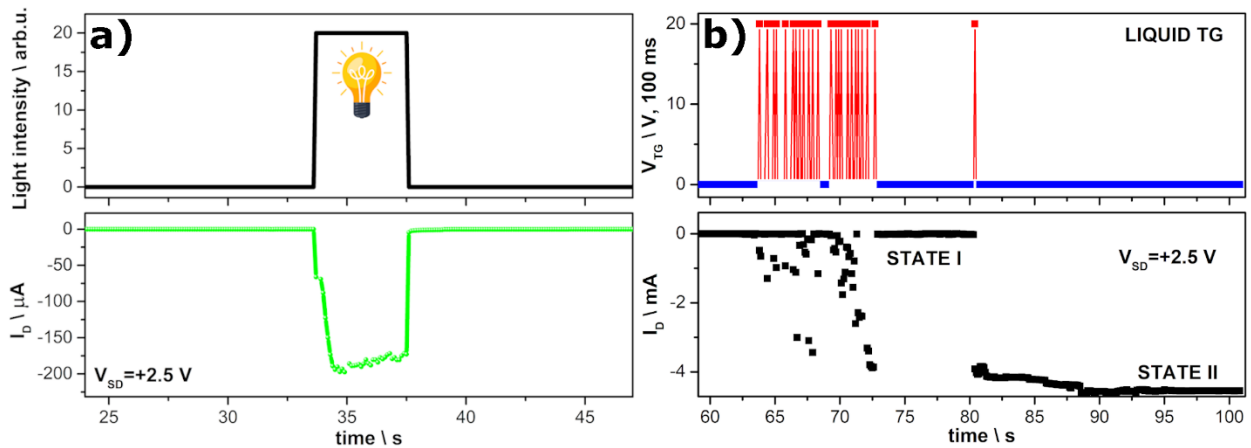
Figure 7. Transient I_{SD} response of CuPc/bu IL-gated MoS_2 FETs in ambient conditions. The pulsed signals were applied to the liquid top gate and the response of the drain current (I_D) to these pulses was measured at a constant source-drain bias (V_{SD}=+2.5 V). a) I_{SD} upon application of a 4 s white light pulse from a xenon lamp, demonstrating real time photoresponse. b) I_{SD} response of the same cell upon a 20 V/100 ms pulse train "training", highlighting non-volatile memory functionality, thus, the "learning" ability of the device.

The response demonstrated in Figure 7b can be considered analogous to experience-based learning in synapses, rendering such devices a promising candidate for future MoS_2 transistor components that could electrically mimic the release and absorption of neurotransmitter ions in biological systems.

3. Conclusions

To summarize, we report the fabrication of ionic-liquid-gated MoS_2-based field-effect transistors with dramatically higher mobilities than their respective back-gated counterparts and on par with some of the most competitive MoS_2 topologies. The observed mobility enhancement is attributed to the presence of the ionic liquid, functioning simultaneously as ionic dopant and ultrathin gating medium, effectively reducing the Schottky barrier at the MoS_2/metal S, D contacts by more than four orders of magnitude. The hybrid liquid-solid state device exhibits P-type conductance, high ON-current of $1.5x10^4$ A for holes and a competitive field effect mobility of 64.3 $cm^2V^{-1}s^{-1}$ at RT. The device addresses the unattainability of P-type conduction in MoS_2, thereby extending its pertinency to PN diodes and complementary integration logic. In addition, photo-enabled switching and memory functionality is demonstrated while the devices are fabricated utilizing CMOS-compatible low energy expenditure, low thermal budget processes.

Remarkably, the high mobility counteracts the presence of non-ideal channel and channel-dielectric-metal interfaces which are of high porosity, structural disorder, charged impurities, and interface roughness. The herein fabricated and evaluated advanced architecture is, to our knowledge, the first low-cost high gain MoS_2 MOSFET based on amorphous low mobility film precursors that enables high-performance multifunctional stackable MOSFETs on any kind of processing-sensitive, plastic and/or flexible substrate.

4. Experimental Section

Fabrication of the BG and DG MoS_2 FETs

We fabricated and tested MoS_2 transistors utilizing a 46 nm thick amorphous MoS_2 film with high porosity as the channel matrix residing between 5 μm spaced source and drain Au/Ti electrodes patterned via conventional optical lithography and lift-off. Highly doped (0.01-0.02 Ω·cm) N-type Si with an 80 nm-thick SiO_2 layer was used as substrate with an Al global backgate contact, formulating a three terminal MOSFET device. Where needed, an Al top gate electrode was manufactured via e-beam lithography and lift-off. Source-Drain electrodes are lithographed prior to MoS_2 deposition and the electronically active region is defined according to the electrode configuration.

MoS_2 film deposition was performed via RT HW CVD by heating a molybdenum wire at 450°C, at chamber pressure of 1.3 Torr and room sample holder temperature, utilizing H_2 flow and H_2S injection. Deposition proceeds via the reaction of the native MoO_x formed on the surface of the Mo filament with H_2S, according to:

$2MoO_3 + 4H_2S \rightarrow 2MoS_2 + 4H_2O + O_2$ [6]

Characterization

All electric measurements were performed at room temperature in a shielded probe station using a HP4041B HP picoammeter of ±0.001 pA (1fA) resolution, a HP4284A precision high-speed LCR meter with test range from 20 Hz to 1 MHz and 0.05% basic accuracy, a Keithley 4200 semiconductor parameter analyzer for DC and pulse device characterization, real-time plotting, and analysis with high precision and sub-femtoamp resolution and an HP 8110A 150 MHz pulse voltage generator through Pt-Ir probes connected via low-noise coaxial cables. UV-vis absorption spectra were obtained on a Perkin-Elmer UV-vis Lambda 40 spectrophotometer. FTIR transmittance spectra were recorded on a Bruker, Tensor 27 spectrometer using 1000 scans at 4 cm^{-1} spectral resolution. SEM images in top view and cross section were obtained using a JEOL field emission scanning electron microscope. Spectroscopic ellipsometry measurements were performed on a M2000-F J.A. WOOLLAM Spectroscopic Ellipsometer system operating across a 250nm-900nm wavelength window at 75° angle of incidence equipped with a L2194-01 Xenon Lamp, utilizing the Woollam Software for data acquisition, data analysis and modeling. All fittings were performed under the assumption of isotropic and non-depolarizing media. X-ray diffraction characterization was performed with a D500 Siemens diffractometer using Cu Kα radiation and a secondary graphite monochromator. X-ray microanalysis (EDAX) was performed with a FEI Inspect instrument equipped with Genesis Spectrum v.4.52 software. Micro-Raman was performed by excitation with a 514.4 nm diode laser line with a spot size of 0.7 micron and density of 0.07 mW/μm^2 on the sample's surface using a x100 objective.

ASSOCIATED CONTENT

Supporting Information. Supplementary figures and details concerning Structural and Spectroscopic and Characterization as well as Electrical Characterization and Ionic liquid gating medium and fabrication details are provided as mentioned in text. The following files are available free of charge. (pdf)

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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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SYNOPSIS