COTS Components Radiation Test Activity and Results at MSSL part 2

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Abstract—**following the paper [1] presenting the full radiation test result of ADC128S102 and DAC121S101 in NSREC2016 conference, this paper continues to report the test results of another three popular commercial off the shelf (COTS) devices AD8065, DG612 and EL7457 under the same EUCLID mission program at MSSL. The tests cover both total ionization dose (TID) and single event effect (SEE). The paper aims to share the test results with the community and provides valuable data for any relevant research.**

Index Terms—**COTS, SEE, TID, IC, MSSL, AD8065, DG612, EL7457**

I. Introduction

MSSL has a long established history in making scientific instrument with major space agency in the world like ESA, NASA. Programs like Hindo instrument on Solar-B, PEACE instrument on Cluster are extremely successful with more than 10 years continuous service in orbit.

EUCLID is one of the latest ESA flagship program for mapping the dark universe. The Visible (VIS) instrument has equipped 36 CCDs driven by 12 chains of readout and power electronics. The design is highly modulated. This results in large quantity of fewer variants of EEE components. This in principle should help the procurement to lower the unit price. However the initial exchange of quotes with the supplier indicates the unit cost of the rad-hard ICs are still outstanding. Besides, some unique IC with excellent performance lacks the rad-hard version. This drives MSSL design team into the route of up-screening the COTS parts.

Following the report of ADC128S102 and DAC121S101 on NSREC2016 receiving widely popularity, this paper will present the full radiation test results of another three devices: AD8065[2], DG612[3] and EL7457[4].

AD8065 is a dual channel JFET input op-amp from Analogue Device. DG612 is a four channel analogue switch from Vishay. EL7457 is a level shift clock driver from Intersil. They play a key role in a CCD readout circuit design. In the up-screening program, we performed gamma dose test to access the total dose effect and threshold. Due to the funding limit and low risk of SEE to these analogue devices, only SEL test was performed on DG612 and EL7457.

In the prior project for instrument UVIS as part of the NOMAD suite, flying on the ESA's ExoMars TGO spacecraft, AD8065 and DG612 are also used in the CCD readout circuit design. A similar up-screening program had been run on these two parts. But only TID was examined in that program. The results of both passed the 30krad test threshold, which enhances the confidence in pursuing the same route for EUCLID program.

EL7457 has been investigated for radiation performance at MSSL for Gaia mission. The prior results [5] show the TID tolerance could be as high as 50krad. SEL LET threshold is above 80 MeV.cm^2.mg^{-1}. The result reported in this paper shows a degradation of TID but similar good performance on SEL.

II. Test Setup

A. Test Facilities and Plan

The test facilities and plan for the three devices here are almost identical to the ones for the two devices reported in NSREC2016 [1]. Therefore, the detail is not repeated here. Just for quick reference, Table I shows the step, total dose and timing for the TID test. The exact dose rate varies a little from the plan in real test. Table II lists the source of heavy ions. To test beyond the 60 MeV.cm^2.mg^{-1}, the EUT can be tilted with respect to the beam axis. The test will stop when beam fluence reaches of 1E10^7 ions/cm^2.

TABLE I
Irradiation Evaluation Test Steps [6]

STEPS	1	2	3	4	5	6	7
PROCESS	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad
Dose[krad(Si)]	2.5	2.5	5	10	10	-	-
Cumulative Dose [krad(Si)]	2.5	5	10	20	30	-	-
Dose Rate [rad(Si)/h]	360	360	360	360	360	-	-
Exposure Time (h)	6.9	6.9	13.9	27.8	27.8	24	168
Temperature (°C)	25	25	25	25	25	25	85

TABLE II
Ion Beam Setting at RADEF [7]

Ion	LET^{SRIM} at surface [MeV.cm^2.mg^{-1}]	Range^{SRIM} [μm]	Beam energy [MeV]
$^{20}Ne^{+6}$	3.63	146	186
$^{40}Ar^{+12}$	10.2	118	372
$^{56}Fe^{15+}$	18.5	97	523
$^{82}Kr^{22+}$	32.1	94	768
$^{131}Xe^{35+}$	60.0	89	1217

The data is quoted from the RADEF test report.

The research was carried out at the Mullard Space Science Laboratory, University College London, as part of the EUCLID VIS flight instrument development project.

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III. TEST RESULTS

A. AD8065

The AD8065 from ADI in Figure 1 is a single channel voltage feedback amplifiers with FET input. The device is developed in ADI's proprietary XFCB (eXtra Fast Complementary Bipolar) process. The particular part number under test is AD8065AR in an 8-ld SOIC package.

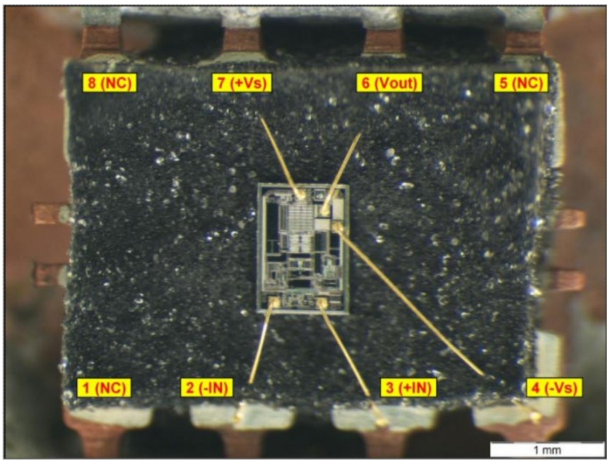


Figure 1 AD8065 full die view

1) TID

Setup

The electrical parameters and bias condition for the test is listed in Table III.

TABLE III

ELECTRICAL MEASUREMENTS TEST CONDITION AND LIMITS

N°	SYMBOL	TEST	CONDITIONS (T_{AMB} = 22±3°C)	LIMITS		UNIT
				MIN.	MAX.	
1	VIO1	Input Offset Voltage	VCM=0V	--	1.5	mV
2	IIB	Input Bias Current	--	--	6	pA
3	IIO	Input Offset Current	--	--	10	pA
4	AVOL	Open-Loop Gain	VO=±3V, RL=1kΩ	100	--	dB
5	CMRR	Common-mode Rejection Ratio	VCM=-1V to +1V	-85	--	dB
6	±VOUT	Output Voltage Swing	RL=1 kΩ	-4.88	--	V
7				+4.90	--	V
8	ICC	Quiescent Current	--	--	7.2	mA
9	PSRR	Power Supply Rejection Ratio	--	-85	--	dB
10	tr	Output Rise Time	VO=4V (step) RL=No load, G=1.	--	--	s
11	tf	Output Fall Time	VO=4V (step) RL=No load, G=1.	--	--	s
12	VIO2	Input Offset Voltage	VCM=0V, VS=±12V, RL=1kΩ	--	1.5	mV

1. VS=±5V, RT=1kΩ, unless otherwise noted in table III.

The bias circuit is kept very simple and shown in Figure 2.

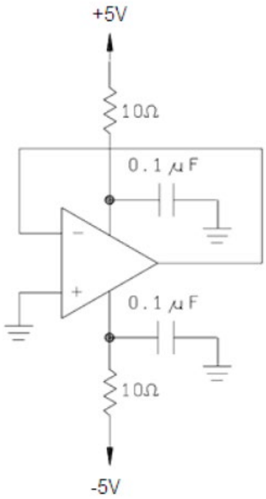


Figure 2 AD8065 TID test bias circuit

Result

The summary of results are presented in Table IV.

TABLE IV

SUMMARY OF TOTAL IONIZED DOSE TEST OF AD8065 IN 2015

	0 krad	2.5 krad	5 krad	10 krad	20 krad	30 krad	ANN24h	ANN168h
$V_{IO}1$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IB}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IO}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
AVOL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
CMRR	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$\pm V_{OUT}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{CC}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
PSRR	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_r	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_f	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$V_{IO}2$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
INPUT VOLTAGE NOISE	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Comparing to the test result from UVIS program [8] presented in Table V, the performance is very consistent.

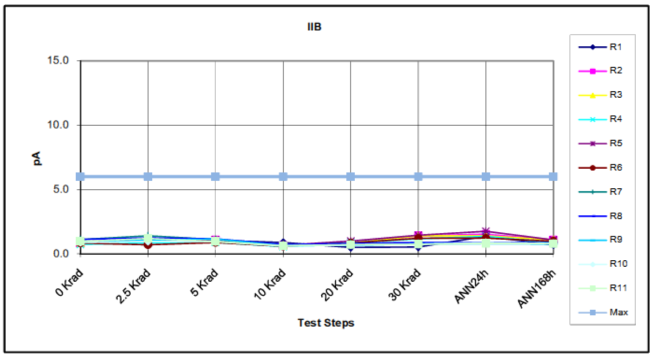
TABLE V

SUMMARY OF TOTAL IONIZED DOSE TEST OF AD8065 IN 2014

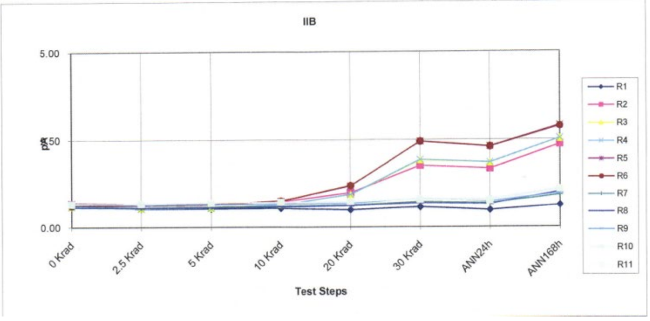
	0KRAD	2.5KRAD	5KRAD	10KRAD	20KRAD	30KRAD	ANN24h	ANN168h
$V_{IO}1$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IB}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IO}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
A_{VOL}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
CMRR	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$\pm V_{OUT}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{CC}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
PSRR	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_r	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_f	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$V_{IO}2$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

The detail measurement data shows the device's parameter is well within the specification with large margin.

One of the key parameters for the CCD readout circuit application is IIB. Figure 3 shows this parameter is sensitive to the gamma dose, but for the test up to 30krad, it is well within the specification.



(a)



(b)

Figure 3 (a) is from test under EULICD program, (b) is from test under UVIS program. Note the y-axis scale is different so that the curve looks very different.

Summary

The value of all the electric parameters under monitor remains unchanged or very little move only, when the sample is subject to radiation at 198.43rad(Si)/h up to total dose of 30krad. The device shows superb immunity to radiation damage. Based on the current result, it is confident to state the device has a good potential to survive even higher dose.

B. DG612

DG612 in Figure 4 is a high-speed, low-glitch quad channel analog switch from Vishay Siliconix. The device is built on the Vishay's D/CMOS process, which combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup. The part number under test is DG612DY in SOIC-16 package.

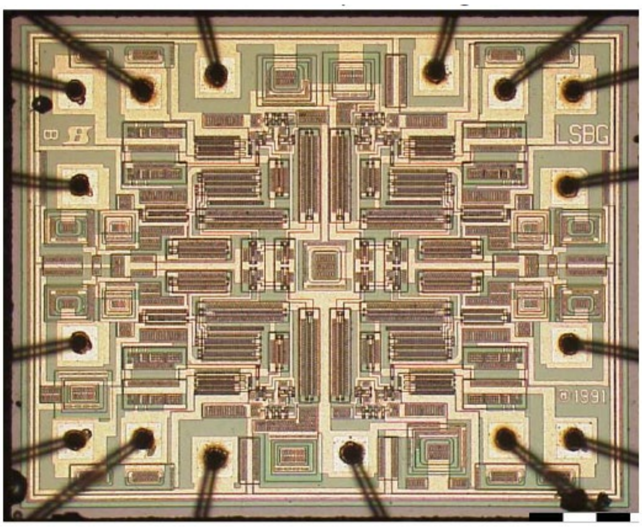


Figure 4 DG612 full die view

1) TID

Setup

The electrical parameters and bias condition for the test is listed in Table VI.

TABLE VI

ELECTRICAL MEASUREMENTS TEST CONDITION AND LIMITS

N°	SYMBOL	TEST	CONDITIONS (T_{AMB} = 22±3°C)	LIMITS		UNIT
				MIN.	MAX.	
1	RDS(ON)	Drain-to-source ON resistance.	IS=-1mA, VD=0V	--	45	Ω
2	IS(OFF)	Source Off Leakage	VS=0V, VD=10V	-0.25	0.25	nA
3	ID(OFF)	Drain Off Leakage Current	VS=10V, VD=0V	-0.25	0.25	nA
4	ID(ON)	Switch On Leakage Current	VS=VD=0V	-0.4	0.4	nA
5	IIN	Input Current	--	-1	1	µA
6	I+	Positive supply current	VIN=0V or 5V	--	1	µA
7	I-	Negative supply current	VIN=0V or 5V	-1	--	µA
8	tON	Turn-On Time	RL=300Ω, CL=75pF, VS=±2V. Note 2	--	35	ns
9	tOFF	Turn-Off Time	RL=300Ω, CL=75pF, VS=±2V. Note 2	--	25	ns
10	Q	Charge injection	CL=1nF, VS=0V. Note 3	--	--	pC
11	XTALK	Crosstalk	RIN=10Ω, RL=50Ω, f=5MHz. Note 3	--	--	dB

1. V+=15 V; V-= -3 V; VL=5 V; VIN=4 V, 1 V, unless otherwise noted in in Table IV.

The bias circuit shown in Figure 5 is also kept simple and close to the real application.

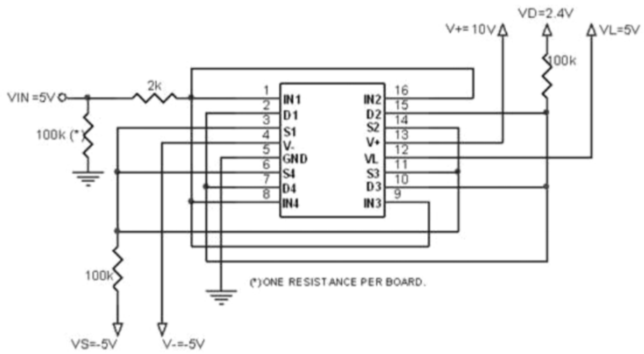


Figure 5 DG612 TID test bias circuit

Results

The summary of the result is listed in Table VII.

TABLE VII

SUMMARY OF TOTAL IONIZED DOSE TEST OF DG612 IN 2015

	0 krad	10 krad	15 krad	20 krad	22.5 krad	25 krad	35 krad	ANN24h	ANN168h
$R_{DS(ON)}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$I_{S(OFF)}$	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
$I_{D(OFF)}$	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
$I_{D(ON)}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IN}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{+}	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
I_{-}	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
t_{ON}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_{OFF}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
Q	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
X_{TALK}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Comparing to the result from UVIS program [9] in Table VIII, the performance is stable.

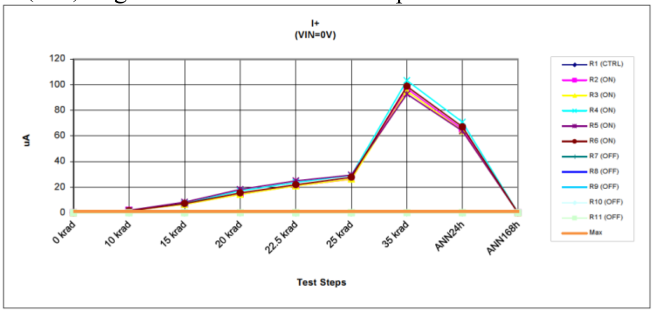
TABLE VIII

SUMMARY OF TOTAL IONIZED DOSE TEST OF DG612 IN 2014

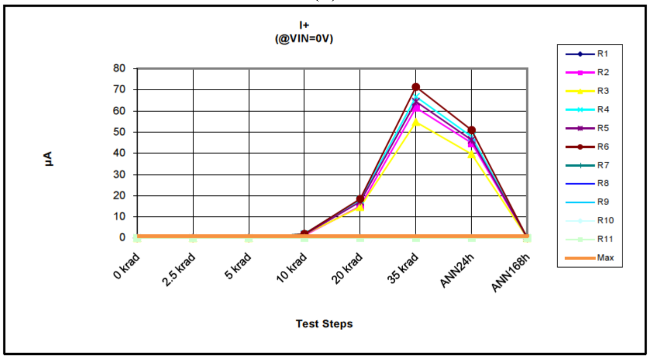
	0 KRAD	2.5 KRAD	5 KRAD	10 KRAD	20 KRAD	35 KRAD	ANN24h	ANN168h
$R_{DS(ON)}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$I_{S(OFF)}$	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	PASS
$I_{D(OFF)}$	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	PASS
$I_{D(ON)}$	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IN}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_+	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
I_-	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1	PASS
t_{ON}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_{OFF}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
Q	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
X_{TALK}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Note 1: parameter out of limits.

The parameter sensitive to the radiation is I_+, I_-, IS(OFF) and ID(OFF). Figure 6 shows the result of parameter I_+.



(a)



(b)

Figure 6 (a) is from test under EULICD program, (b) is from test test under UVIS program. The dose test stepping is arranged differently in the two tests, so the table and graph looks slightly different. But from both tests, the parameter was found to be out of limit at 10krad check point.

Note the parameter I_+ and I_- are within the limit when they are tested at condition VIN=5V but out of limit at condition VIN=0V.

Summary:

In the test from this report, the sample is exposed to a real dose rate at 213.77rad(Si)/h. Test stops at 35krad. It is found four electric parameters under monitoring are sensitive to the radiation. They are: I+, I-, IS(OFF) and ID(OFF). The two supply currents (I+, I-) start to be out of limit (±1μA at room temperature) between 0 and 10krad. The maximum current recorded is ~100μA at 35krad. It looks like the current will increase exponentially with the accumulated dose. The device remains functioning despite the increasing supply current. So it is considered acceptable. The leakage currents (IS(OFF),ID(OFF)) start to increase out of spec between 10 and 15krad. The max is recorded at 29.5mA at 35krad. This is higher than the possible switch on IS and ID, as limited by the resistor in series in the test circuit. This suggests that there is parasitic short-path created by the accumulated dose. All the four parameters recover to initial value after 168h annealing. For unbiased samples, none of the four parameters have changed.

2) SEE

Setup

Bias circuit in Figure 7 is a copy of real application.

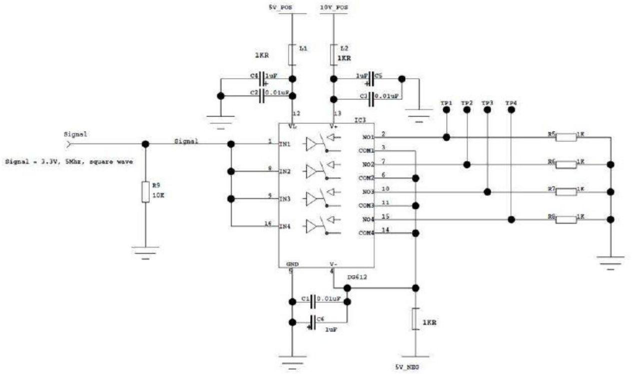


Figure 7 DG612 SEL test bias circuit.
Test configuration is DUT_VL = +5V, DUT_V+ = +10V, DUT_V- = -5V, INPUTS = Square wave ±3.3V at 5MHz.

Results

The summary of the result is listed in Table IX.

TABLE IX

SUMMARY OF SEL TEST OF DG612 IN 2015

Facility	medium	run_number	Facility_run_number	board_id	temperature	dut_partnumber	test_mode	Ion	LET	roll	tilt	Eff. LET	run_duration	entered_fluence	SEL
RADEF	vacuum	1	70	1	room	1,2	SEL	Xe	60	0	0	60.0	685	1.00E+07	0
RADEF	vacuum	2	71	1	room	3,4	SEL	Xe	60	0	0	60.0	264	1.00E+07	0
RADEF	vacuum	3	72	1	room	1,2	SEL	Xe	60	0	53	99.7	436	1.00E+07	0
RADEF	vacuum	4	73	1	room	3,4	SEL	Xe	60	0	53	99.7	544	1.00E+07	0
RADEF	vacuum	5	74	1	room	1,2	SEL	Xe	60	0	60	120.0	543	5.91E+06	0
RADEF	vacuum	6	75	1	room	1,2	SEL	Xe	60	0	60	120.0	586	5.72E+06	0
RADEF	vacuum	7	76	1	room	3,4	SEL	Xe	60	0	60	120.0	1450	1.00E+07	0

Summary

Four samples are tested with two samples at a time. The SEL detection threshold is set at 100mA for VL, 100mA for V+ and -100mA for V-. The test starts with Xenon without tilt (LET = 60 $MeV.cm^2.mg^{-1}$), no SEL event was detected upto beam fluences of $1E10^7$ ions/cm^2. Then test continues with higher LET by tilting the Xenon source. At effective LET of 100 and 120 $MeV.cm^2.mg^{-1}$, still no SEL event was captured.

We can conclude the device is latchup free up 120MeV. This may be directly resulted from the design of an epitaxial layer.

C. EL7457

EL7457 in Figure 7 is a high-speed, non-inverting, quad CMOS driver, manufactured by Intersil. It is likely to be built on SOI technology as most INTERSIL devices are using this process. This device has been tested for TID and SEL in a radiation study for GAIA project in 2007[10].

Its rad-hard version is ISL7457SRH. ESA has carried out independent SEE test on it in 2014[11].

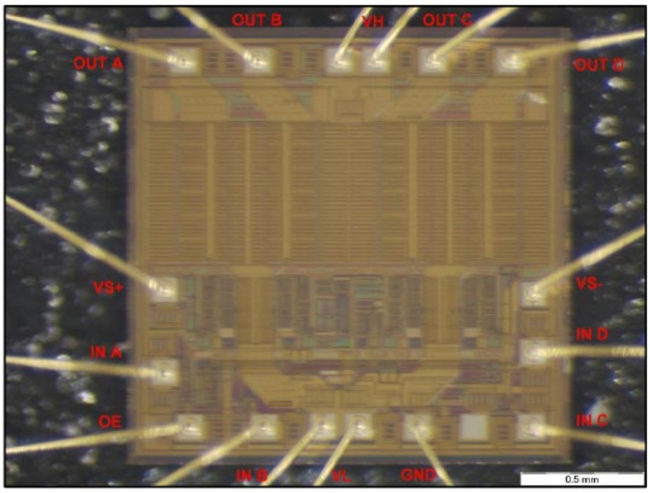


Figure 7 EL7457 full die view

1) *TID*

Setup

The electrical parameters and bias condition for the test is listed in Table X.

TABLE X

ELECTRICAL MEASUREMENTS TEST CONDITION AND LIMITS

N°	SYMBOL	TEST	CONDITIONS (T_{AMB}=22±3°C)	LIMITS MIN.	LIMITS MAX.	UNIT
1	I_{IH}	Logic "1" Input Current (Vs = ±5V)	VIH = 5V		10	pA
2		Logic "1" Input Current (Vs = +1510V)	VIH = 5V	-	10	pA
3	I_L	Logic "0" Input Current (Vs = ±5V)	VIL = OV	-	10	pA
4		Logic "0" Input Current (Vs = +1510V)	VIL= OV	-	10	pA
5	R_{OH}	ON Resistance VH to OUTx (Vs = ±5V)	Iour = -100mA	-	6	Ω
6		ON Resistance VH to OUTx (Vs = +15/0V)	Iour = -100mA	-	5	Ω
7	R_{OL}	ON Resistance VL to OUTx (Vs = ±5V)	Iour = +100mA	-	6	Ω
8		ON Resistance VL to OUTx (Vs = +15/0V)	Iour = +100mA	-	5	Ω
9	I_{LEAK}	Output Leakage Current (Vs = ±5V)	VH = VS+, VL = VS-	-	10	pA
10		Output Leakage Current (Vs = +15/0V)	VH = Vs+, VL = Vs_	-	10	pA
11	I_s	Power Supply Current (Vs = ±5V)	Inputs = Vs+	-	1.5	mA
12		Power Supply Current (Vs = +15/0V)	Inputs = Vs+	-	2	mA
13	T_r	Rise time (Vs = ±5V)	INx = OV to 4.5V step, CL = 1nF	-	40	ns
14		Rise time (Vs = +15/0V)	INx = OV to 5V step, CL = 1nF	-	20	ns
15	T_f	Fall time (Vs = ±5V)	INx = 4.5V to OV step, CL = 1nF	-	30	ns
16		Fall time (Vs = +15/0V)	INx = 5V to OV step, CL = 1nF	-	20	ns
17	T_{D+}	Turn-on delay time (Vs = ±5V)	INx = OV to 4.5V step, CL = 1nF	-	30	ns
18		Turn-on delay time (Vs = +15/0V)	INx = OV to 5V step, CL = 1nF	-	20	ns
19	T_{D-}	Turn-off delay time (Vs = ±5V)	INx = 4.5V to OV step, CL = 1nF	-	40	ns
20		Turn-off delay time (Vs = +15/0V)	INx = 5V to OV step, CL = 1nF	-	20	ns
21	T_{ENABLE}	Enable delay time (Vs = ±5V)	INx = OV to 4.5V step, RL = 1k0	-	35	ns
22		Enable delay time (Vs = +15/0V)	INx = OV to 5V step, RL = 1k0	-	25	Ns
21	$T_{DISABLE}$	Disable delay time (Vs = ±5V)	INx = OV to 4.5V step, RL = 1k0	-	35	ns
22		Disable delay time (Vs = +15/0V)	INx = OV to 5V step, RL = 1k0	-	25	Ns

Results

The summary of the result is listed in Table XI

TABLE XI

SUMMARY OF TOTAL IONIZED DOSE TEST OF EL7457

			0 krad	2.5 krad	5 krad	10 krad	20 krad	30 krad	Ann24h	Ann168h
– INPUT SECTION –										
I_{IH}	±5V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{IL}	±5V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
– OUTPUT SECTION –										
I_{LEAK}	±5V	ON	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
R_{OH}	±5V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 1	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
R_{OL}	±5V	ON	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2
– POWER SUPPLY SECTION –										
I_{S+}	±5V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_{S-}	±5V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I_S	15V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
– SWITCHING CHARACTERISTICS SECTION –										
t_R	±5V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_F	±5V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_{D+}	±5V	ON	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
t_{D-}	±5V	ON	PASS	PASS	PASS	PASS	PASS	NOTE 2	PASS	PASS
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 2	NOTE 2	NOTE 2
		OFF	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 3	NOTE 3
t_{ENABLE}	±5V	ON	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	15V	ON	PASS	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
$t_{DISABLE}$	±5V	ON	PASS	PASS	PASS	NOTE 2	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1
	15V	ON	PASS	PASS	PASS	NOTE 1	NOTE 2	NOTE 2	NOTE 2	NOTE 2
		OFF	PASS	PASS	PASS	PASS	NOTE 1	NOTE 1	NOTE 1	NOTE 1

NOTE 1: Parameter out of limits

NOTE 2: Loss of functionality of the device.

NOTE 3: The results obtained for the Turn-off delay time (VS = +15/0V) parameter, exceeded lightly the maximum limit shown in the test plan from 0krad step. As it is explained in the test plan, these limits have been taken from the 5962-08230 specification only as reference due to the fact that no limits were specified in the MFR data sheet (only are specified the typical values). For this reason, the maximum limit of the 20ns is not considered as pass/fails criteria in the initial electrical measurement and control sample.

Figure 8 presents a typical parameter value change vs accumulated dose. Most of the parameters affected by the dose only show very minor excess of limit. The worst failure is observed that some samples have lost functionality at 10krad checking point. The loss of functionality means when the input signal switches between high and low level, the output signal stays constant. No obvious excessive supply current is observed. But we notice the output pin diode threshold had dropped to 0.35V.

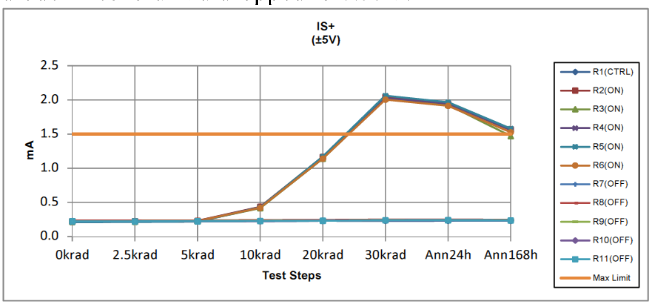


Figure 8 I_{S+} parameter change with accumulated dose.

Summary

The real dose rate at test is 203.39rad (Si)/h and up to cumulative dose of 30krad. The result shows EL7457 is very sensitive to the radiation damage. Most parameters are strongly affected by gamma dose. Between 5krad and 10krad, some biased samples lost the functionality or completely failed. It is said the EL7457 was very poor and very non homogenous in radiation and the ISL7457 (their rad-hard equivalent version) had much better performance by partly re-design (e.g. improve the step coverage) and WLAT (Wafer Lot Acceptance Test) screening. However we note even the official datasheet for ISL7457 only claims 10krad minimum TID at dose rate of 50-300rad/s. This indicates the device design/manufacturing process is intrinsically sensitive to radiation damage. The lot under test only survived up to 5krad compared to the previous report of 50krad [5].

2) *SEE*

Setup

The bias circuit in Figure 9 is used for the SEL test.

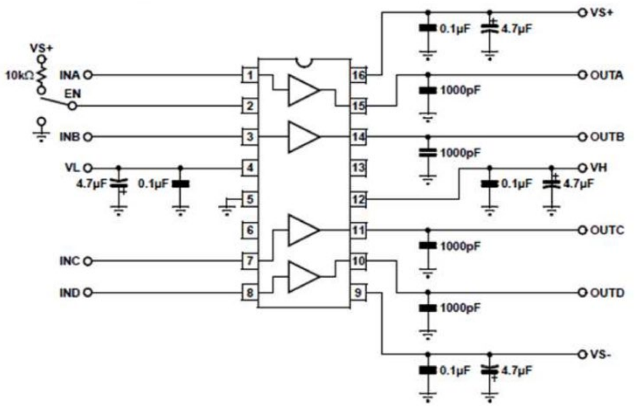


Figure 9 EL7457 SEL test bias circuit.
Test configuration is DUT_V+ = +10V, DUT_V- = 0V, INPUTS = Square wave ±3.3V at 2MHz.

Result

The summary of the result is listed in Table XII.

TABLE XII
SUMMARY OF SEL TEST OF EL7457

run_folder	Facility	medium	run_number	Facility_run_number	test_mode	board_id	dut_part_id	temperature	Ion	LET	roll	tilt	Effective LET	run_duration	entered_fluence	SEL
RUN003	RADEF	vacuum	3	48	SEL	kit 2	1, 2	room	Xe	60	0	55	104.61	728	1.00E+07	0
RUN004	RADEF	vacuum	4	49	SEL	kit 2	3, 4	room	Xe	60	0	55	104.61	767	1.00E+07	0
RUN005	RADEF	vacuum	5	50	SEL	kit 2	1, 2	room	Xe	60	0	58	113.22	785	1.00E+07	0
RUN006	RADEF	vacuum	6	51	SEL	kit 2	3, 4	room	Xe	60	0	58	113.22	782	1.00E+07	0
RUN007	RADEF	vacuum	7	52	SEL	kit 2	1, 2	room	Xe	60	0	60	120.00	841	1.00E+07	0
RUN008	RADEF	vacuum	8	53	SEL	kit 2	3, 4	room	Xe	60	0	60	120.00	844	1.00E+07	0

Summary

Same procedure and setup are followed as DG612. Only the thresholds are adjusted to 100mA for Vs+ and -100mA for Vs-. EL7457 proves to be latchup free up to 120 MeV.cm^2.mg^{-1}. Another study in [5] with test up to 80MeV also finds no incidence of latchup.
SET is not tested. But ESA study on ISL7457ASRH [11] records cases at LET as low as 45.4MeV.cm^2.mg^{-1}.

IV. SUMMARY

AD8065 shows great immunity to Gamma ray up to the total dose of 30krad TID.
DG612 shows some sensitivity on some parameters but all tends to recover after annealing.
EL7457 is very sensitive to the radiation. Some samples failed between 5krad and 10krad permanently.
Both DG612 and EL7457 prove to be SEL free up to 120 MeV.cm^2.mg^{-1} for beam fluences up to 1E10^7 ions/cm^2.

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[3] DG612 datasheet, from VISHAY, http://www.vishay.com/analog-switches/list/product-70057/ .
[4] EL7457 datasheet, from INTERSIL. http://www.intersil.com/en/products/amplifiers-and-buffers/all-amplifiers/powerfet-ccd-drivers/EL7457.html
[5] GAIA-PEM Industrialisation Study COTS Device Radiation Test Report, 24 March 2006.
[6] RadLab at ALTER TECHNOLOGY(Spain), webpage: http://www.altertechnology.com/atn/en/radiation/total-ionizing-dose-tests-924.htm.
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[9] Total Dose Radiation Test Report for DG612, ATN-RR-309, 28 Oct 2014
[10] Radiation Testing to Determine the TID Susceptibility and SEL LET Thresholds of COTS Devices, 13 Different Types, for the GAIA Project, ESA/ESTEC D/TEC-QCA, Jan 24th 2007.
[11] SEE test of the Intersil Quad CMOS Driver ISL7457SRHF, RADEF November 2014, ESA report ESA-TECQEC-LAB-TR-0758.