Modelling, Analysis and Design of Optimised Electronic Circuits for Visible Light Communication Systems

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A thesis submitted for the degree of Doctor of Philosophy

of

University College London

Information & Communication Systems Research Group

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November, 2021

Declaration

I, Amany Kassem, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the work.

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Abstract

This thesis explores new circuit design techniques and topologies to extend the bandwidth of visible light communication (VLC) transmitters and receivers, by ameliorating the bandwidth-limiting effects of commonly used optoelectronic devices. The thesis contains detailed literature review of transmitter and receiver designs, which inspired two directions of work. The first proposes new designs of optically lossless light emitting diode (LED) bandwidth extension technique that utilises a negative capacitance circuit to offset the diode's bandwidth-limiting capacitance. The negative capacitance circuit was studied and verified through newly developed mathematical analysis, modelling and experimental demonstration. The bandwidth advantage of the proposed technique was demonstrated through measurements in conjunction with several colour LEDs, demonstrating up to 500% bandwidth extension with no loss of optical power. The second direction of work enhances the bandwidth of VLC receivers through new designs of ultra-low input impedance transimpedance amplifiers (TIAs), designed to be insensitive to the high photodiode capacitances (C_{pd}) of large area detectors. Moreover, the thesis proposes a new circuit, which modifies the traditional regulated cascode (RGC) circuit to enhance its bandwidth and gain. The modified RGC amplifier efficiently treats significant RGC inherent bandwidth limitations and is shown, through mathematical analysis, modelling and experimental measurements to extend the bandwidth further by up to 200%. The bandwidth advantage of such receivers was demonstrated in measurements, using several large area photodiodes of area up to 600 mm^2, resulting in a substantial bandwidth improvement of up to 1000%, relative to a standard 50 Ω termination. An inherent limitation of large area photodiodes, associated with internal resistive elements, was identified and ameliorated, through the design of negative resistance circuits. Altogether, this research resulted in a set of design methods and practical circuits, which will hopefully contribute to wider adoption of VLC systems and may be applied in areas beyond VLC.

Impact Statement

This thesis contributes to the study, design, and practical implementations of new electronic circuit design techniques to enhance the bandwidth of optoelectronic devices in visible light communication systems (VLC). This theme is particularly relevant given the unprecedented demand on the limited radio frequency (RF) spectrum, which has motivated researchers to explore alternative technologies to support data communication. VLC established itself as one of the most promising candidate technologies to alleviate the looming RF spectral crisis. As an indoor access network, one of the main driving forces for VLC is the significant advances in solid-state lighting, which enabled power-efficient and extended life-span lighting infrastructure using light-emitting diodes (LEDs). Moreover, the ubiquity of LEDs offers an attractive economic advantage since VLC technology leverages on the existing lighting infrastructure to serve the dual functionality of illumination and data communication. In addition to offering other advantages such as the huge unregulated $\sim$400 THz bandwidth free of licensing costs.

The analysis, techniques and topologies introduced in this thesis are shown to improve the utility of the VLC technology significantly through performance optimisation of the highly bandwidth-limited optoelectronic devices, including high power LEDs and large area photodiodes, which are typically employed in VLC systems. The bandwidth optimisation techniques proposed in this thesis tackle the bandwidth limitation associated with the optoelectronic devices in a rather atypical approach by adopting new and existing electronic circuits that boosts performance. Such techniques are envisaged to impact the innovation in VLC systems and motivate new research to construct simple and cost-effective systems using optimised circuits for indoor communications in office and home environments. Furthermore,

the reported circuit techniques dealt with the bandwidth challenges encountered at both the transmitter and the receiver side, which paved the way for the efficient utilisation of commercially available high power LED lighting to provide room illumination alongside data communication. This is in addition to the use of commercially available exceptionally large area photodiodes with significantly better light-harvesting capabilities, therefore, allowing for communication at practical data rates and transmission distances.

Most of the research and experimental work presented in the thesis have been peer-reviewed and reported in four top conference papers and one journal paper in the field of circuits and systems design. The successful implementation of the proposed circuit techniques would hopefully contribute to the wide adoption of VLC systems and may be applied in areas beyond VLC, especially in high-speed optical fibre communications, where the adoption of the proposed circuit techniques could potentially allow for higher achievable data rates. Furthermore, the techniques developed in this thesis may impact other areas of electronic sensing applications and sensor networks, from pollution monitoring and ultrasound sensing to tomography for industrial and medical applications and other systems where performance is limited by high and undesirable capacitances of sensors and sources.

Acknowledgements

First and foremost, I would like to express my deep heartfelt appreciation to my principal supervisor Professor Izzat Darwazeh who has patiently guided me throughout my PhD and my MSc before that. Izzat has been incredibly generous with his time and efforts. He motivated my sense of curiosity and wonder, which deepened my enthusiasm and passion for circuit design and influenced how I view and approach my work. Thank you for believing in me and for continuously challenging my knowledge of the subject, which have significantly improved the quality of the work in this thesis. Your contribution to my personal and professional growth has been immeasurable. You have been a mentor and, above all, a friend, and for that, I am eternally grateful.

The research presented in this thesis was carried out in the Laboratories of the Electronic and Electrical Engineering department at University College London, where I was lucky to have been surrounded and supported by a bunch of fantastic people to whom I am deeply indebted and so appreciative. I first offer my gratitude to Dr Paul Anthony Haigh, who was a postdoctoral fellow at UCL for part of my PhD. I really appreciate the guidance he has given me, especially with setting up my first VLC experiments. Thank you, sincerely. I am also so grateful for Dr Temitope Odedeyi for all the technical discussions and the good lab company he provided during lockdown times. Dr Waseem Ozan, for providing the best company during lunch and for all the coffees throughout the years. Thank you both for your valuable friendships. To my dearest friend, Xinyue Liu, who joined UCL halfway through my PhD and my life has not been the same ever since. She brought so much fun to my life and has provided a much needed refuge that has sustained me during

the past years. Thank you for your friendship. Last but not least, I must thank Scott Martin for fabricating all the PCBs used in this research, often at a very short notice. Thank you for your patience. I would also like to thank Gerald McBrearty and Andrew Moss for maintaining a well-organised lab environment and for their help providing much of the equipment used in the experiments in this work.

I would like to express my immense gratitude to my parents, who not only generously funded my PhD but relentlessly pushed me to be my best self. As always, this PhD would not have been possible without their support. To my mother, thank you for going above and beyond what is possible to support me and for setting a wonderful example of what it means to be a strong loving woman. I look up to you in so many ways. To my father, my greatest supporter, no words can ever do you justice or express the love and admiration I have for you. I hope I always make you both proud. To my twin brother Hossam, who was in London for a good part of my PhD, I am beyond blessed to have you by my side. Thank you very much for always believing in me. I hope we both continue to shine together.

Last but not least, to my partner, Mostafa, your support means the world to me. Thank you for loving me and being by my side. I would also like to thank my best friends; Menna and Zeina, whom I consider to be my chosen family. Thank you very much for being such good listeners and reliable friends. I am forever grateful to have you both. I would also like to thank my dear friends, Sarah and Nour, with whom I have shared a lot of happy memories and whose friendships made London feel like home.

Finally, I would like to acknowledge funding, for 18 months of this PhD work, by UCL and by the Engineering and Physical Sciences Research Council (EPSRC) Multifunctional Polymer Light-Emitting Diodes with Visible Light Communications (MARVEL) grant.

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List of Abbreviations & Symbols

β Transistor current gain

ζ Damping factor

ω_n Natural frequency

ε_o Relative permittivity of vacuum

ε_r Dielectric constant of a material

A_T Transimpedance gain

A_v Amplifier voltage gain

C_μ Base collector capacitance

C_π Base emitter capacitance

C_c Compensating capacitor

C_{gd} Gate drain capacitance

C_{gs} Gate source capacitance

C_j Junction capacitance of the LED

C_{pd} Photodiode junction capacitance

L_b Base contact inductance

L_c Collector contact inductance

L_e Emitter contact inductance

Q Quality factor of the complex pole

R_F Feedback resistor

R_{com} Compensating resistor

R_e Emitter contact resistance

R_{in} Input resistance

R_{stb} Stabilising resistor

f_T Transit frequency

g_m Transconductance

r_π Base emitter junction dynamic resistance

r_{bb} Intrinsic base spreading resistance

r_d Dynamic resistance of the LED

r_e Transistor dynamic resistance

AGC Automatic Gain Control

ANN Artificial Neural Network

BJT Bipolar Junction Transistor

BLW Baseline Wander

CAP Carrier-less Amplitude and Phase

CB Common Base

CC Common Collector

CD Common Drain

CE Common Emitter

CG Common Gate

CML Current Mode Logic

CMOS Complementary Metal Oxide Semiconductor

CS Common Source

DMT Discrete Multitone

EM Electromagnetic

ESD Electrostatic Discharge Circuit

FET Field Effect Transistor

HBT Heterojunction Bipolar Transistor

IEEE Institute of Electrical and Electronic Engineering

INIC Current Inversion Negative Impedance Converter

IoT Internet of Things

LED Light Emitting Diode

NIC Negative Impedance Converter

NII Negative Impedance Inverter

NMOS N-channel Metal Oxide Semiconductor

OCS Open Circuit Stable

OFDM Orthogonal Frequency Division Multiplexing

OOK On Off Keying

Op-amp Operational amplifier

OWC Optical Wireless Communication

PCB Printed Circuit Board

PMOS P-channel Metal Oxide Semiconductor

RF Radio Frequency

RGC Regulated Cascode

SCS Short Circuit Stable

SFB Shunt Feedback

SiGe Silicon Germanium

SMD Surface Mount Devices

SNR Signal to Noise Ratio

TIA Transimpedance Amplifier

VLC Visible Light Communication

VLCC Visible Light Communication Consortium

VLSI Very Large Scale Integration

VNA Vector Network Analyser

VNIC Voltage Inversion Negative Impedance Converter

WDM Wavelength Division Multiplexing

XCP Cross Coupled transistor Pair

Chapter 1

Introduction

Communication specialist companies such as Cisco forecast the number of connected devices to be more than three times the global population by 2023 [1]. The proliferation of mobile devices, all of which demand faster connection speeds, is fuelled by various data-hungry applications such as virtual reality, multimedia streaming and gaming services, resulting in severe spectral congestion, causing a capacity crunch; the main cause is the inability of radio frequency (RF) to meet demand due to spectrum shortage. Therefore, complementary wireless communication systems are being continuously proposed, and one of the most promising candidates is visible light communication (VLC). VLC uses light in the spectral range 380-740 nm ($\sim$800-400 THz) to transmit and receive data, mainly via light emitting diodes (LEDs) and photodiodes, respectively.

The first demonstration of VLC using a single white LED was in Japan in 2000 [2]; since then interest in VLC rapidly grew with abundance of practical demonstrations adopting different technologies to enable multi-Gbps VLC systems. Alas, practical VLC is still in its infancy, due to the bandwidth limitation imposed by the optoelectronic devices, namely, LEDs and photodiodes, hence, restricting the achievable transmission speeds. Moreover, severe limitations are imposed by the highly attenuating free-space channel, which limits the received optical signal power. To combat such limitations, researchers focused on the efficient utilisation of the limited bandwidth offered by the optoelectronic devices by (i) Adopting advanced modulation formats, such as orthogonal frequency division

multiplexing (OFDM) and carrier-less amplitude and phase (CAP), to maximise the number of transmitted bits per symbol [3–8], (ii) Using efficient equalisation techniques at the transmitter and receiver [9, 10] (iii) Exploiting the colour dimension to enable wavelength division multiplexing (WDM), as such provide additional spectrum [11, 12]. Others resorted to improving the available bandwidth by employing higher bandwidth devices such μLEDs and lasers. Only a few researchers have exploited bandwidth enhancement circuits techniques to circumvent the bandwidth limitation imposed by LEDs or photodiodes.

This work is motivated by the importance of dealing with the bottleneck imposed by the optoelectronic devices, which has been identified as a perpetual challenge in achieving high data rates in VLC in [13], and most recently elegantly summarised in [14], where the importance of optimised device selection was highlighted. As such this thesis focuses on exploring existing and new electronic circuit techniques that improve the utility of the highly bandwidth-limited optoelectronic devices in VLC systems, extending the bandwidth of VLC transmitters and receivers. At the transmitter, the main challenge is improving data transmission speeds, considering the low modulation bandwidth of commercially available LEDs, typically limited to a few MHz. The LED bandwidth is determined by the carrier lifetime and the RC time constant associated with its dynamic resistance (r_d) and junction capacitance (C_j). A commonly used circuit technique to overcome the bandwidth limitations of LEDs is analogue passive RC-based equalisers, as reported in [15–20]. This type of equaliser applies a passive high pass filter with the inverse response of the LED frequency response, hence, extending its bandwidth. Nevertheless, such bandwidth extension is often at the expense of substantial loss in the LED optical signal power. While such equalisers have effectively demonstrated high data rates in VLC links by extending the transmitter bandwidth, their benefits will always be limited as they incur a significant loss in optical power. Hence, limiting the LED output light intensity and possibly the overall system capacity due to the reduction in signal to noise ratio (SNR) at the receiver.

In contrast, the work in this thesis proposes an optically lossless LED circuit-

based bandwidth extension technique. The technique is based on the use of active circuits to generate negative capacitance in parallel to the LED junction capacitance to neutralise its bandwidth-limiting effect on the determination of the VLC transmitter bandwidth. The elegance of such a technique is that it does not result in any resistive loading to the LED; hence, the resultant bandwidth enhancement does not compromise its optical power. Moreover, it allows for bespoke, yet easily adjustable, LED driver circuit design based on the distinct characteristics of each LED, while also combining with other existing techniques to further the bandwidth enhancement. The generation of negative capacitance via active circuits can be achieved either by using networks known as negative impedance converters (NICs) or by using amplifiers that utilise the Miller effect. The operation, advantages and disadvantages of each of the negative capacitance circuits are to be discussed in Chapter 2.

At the receiver, the challenge is to capture sufficient light to ensure correct detection of the transmitted information. This is a difficult challenge due to two reasons; firstly, the highly attenuating nature of the free-space channel, whose loss is proportional to the square of the transmission distance. Second, most photodiodes operating in the visible range are made of doped silicon, which has poor responsivity in the visible light frequency range, especially at blue wavelength, commonly used in VLC. To boost the received optical power and maximise the associated photocurrent, especially for applications that demand large transmission distances, ideally, the receiver should have a large-area photodiode to maximise light capture. Alternatively, systems may employ high gain transimpedance amplifiers (TIAs)[1] to convert the low amplitude photocurrent from the photodiode into an amplified voltage. Ideally, systems would combine large photoactive area detectors and high gain TIAs. Unfortunately, large-area photodiodes have highly limited bandwidth, particularly when followed by either 50 Ω or high input impedance TIAs; such limitation arises from their substantially high junction capacitance (C_{pd}), which is proportional to the active area. In the vast majority of VLC reports, such bandwidth limitation is avoided by employing small area photodiodes, which are simply

[1]Throughout this thesis, the term TIA, which is the most commonly used, is adopted for optical frond-ends with current input and voltage output

incapable of collecting sufficient optical power to allow practical distances.

Using a low input impedance TIA configuration is advantageous in tolerating high photodiode capacitances [21]. This is because the dominant time constant, which determines the receiver bandwidth, is a product of photodiode capacitance and the TIA input resistance. Hence, a TIA with low input resistance reduces the time constant and significantly increases the bandwidth. Circuits with ultra-low input resistance, such as the regulated cascode (RGC) [22–24] were found to be highly attractive for use in VLC systems. The work in this thesis proposes the use of the low input impedance RGC TIA to improve the utility of unconventionally large-area photodiodes, in the range of 100 mm^2 to 600 mm^2, which have associated junction capacitances in the range of 100's of picofarads to a few nanofarads. The use of such large-area photodiode is not common in VLC systems, which often employ photodiodes of few mm^2. This is often done to avoid the bandwidth limitation associated with such large-area photodiodes, yet it removes the increased signal power advantages achieved with such photodiodes and, in turn, often limit the transmission distances.

Employing such a large-area photodiode can be highly beneficial in boosting the received signal power. Such an increase in the received signal power may allow for transmission at longer distances, making the application of VLC more practicable. Nevertheless, it imposes a complex design challenge on the successive transimpedance amplifier. This work endorses the use of low input impedance TIAs for their advantages in tolerating such high photodiode capacitance and, therefore, provides a remarkable improvement in bandwidth compared to a traditional 50 Ω TIAs. The work explores existing and new low input impedance TIA configurations based on critical analysis of their performance with high photodiode capacitances to achieve high gain and wide-band performance.

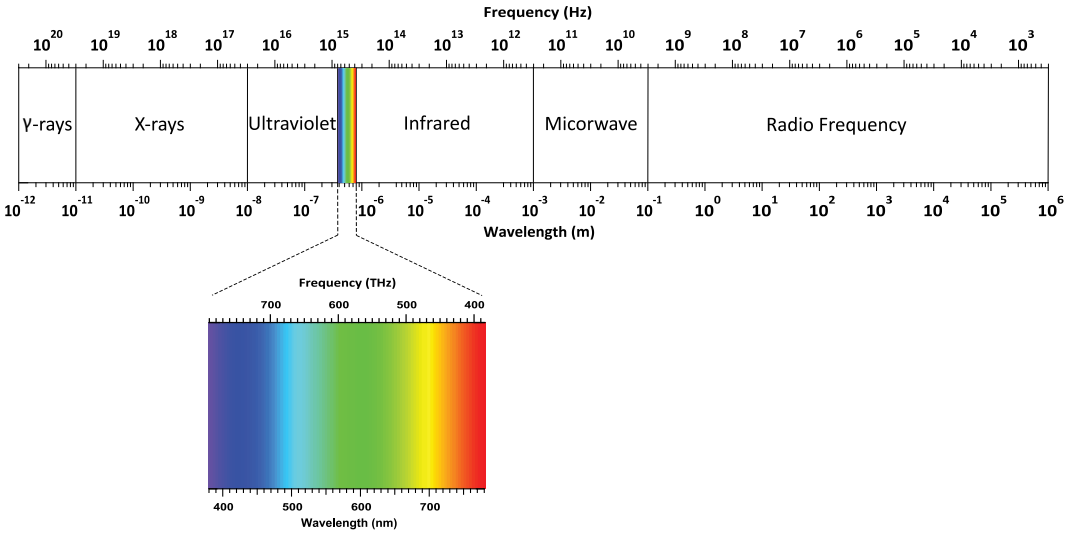


Figure 1.1: EM spectrum

1.1 VLC Preliminaries & Challenges

Figure 1.1 shows the electromagnetic (EM) spectrum specifying the wavelength band of different waves, where it extends from low RF to highest frequency gamma rays with the shortest wavelength. The RF is predominately the most used portion of the EM spectrum to facilitate communication. On the other hand, advancements in user electronics and mobile communication have led to an unprecedented proliferation of mobile devices, demanding higher data rates and better signal quality. The result is a severely congested RF spectrum. Therefore, systems that complement wireless links have been proposed, and one of the most promising is VLC, which is gaining high research momentum. VLC offers ∼400 THz of new, unlicensed bandwidth, as opposed to the 300 GHz of heavily regulated RF spectrum. This spectrum directly translates into a new capacity for access networks, alleviating the looming capacity crunch.

Moreover, the ubiquity of LEDs renders an economic advantage, as existing lighting infrastructure is utilised, and installation of LEDs is cheap: LEDs serve the dual functionality of illumination and communication, through intensity modulation of an LED using a data source. The modulated light from the LED propagates over free-space and is recovered using direct detection via a photodetector. The first VLC report using white LEDs emerged in Japan [2]. Following this, the concept of VLC

started to grow rapidly, and the visible light communication consortium (VLCC) was established in Japan in 2003. This was followed by the standardisation of VLC by the institute of electrical and electronic engineering (IEEE) in 2012, and ever since, the interest in VLC has rapidly grown with an abundance of practical demonstrations adopting different technologies to enable high data rate transmission. The following sections briefly discuss some of the transmitters and receivers employed in VLC, highlighting their advantages and drawback and some of the technologies that allowed for improved utility of such devices in the application of high-speed data transmission. Noting that the following discussion of the bandwidth limitation of the optoelectronic devices and techniques to tackle such limitation is only relevant within applications requiring high-speed data transmission, yet such theme may not concern other visible light applications such as indoor positioning.

VLC Transmitter Light Source

The majority of light sources utilised in VLC systems are white light LEDs, which are classified into two types: Phosphors-coated LEDs (PC-LEDs) and tri-chromatic red, green and blue LEDs (RGB-LED). The first type achieves white light using a single blue LED coated with a complementary colour converting material such as a yellow phosphor. The second method is by combining the emission of multiple colour LEDs to form white light. However, the former approach limits the bandwidth of the LED to a few MHz due to the slow response of the phosphorous colour converting material [13, 25]. It is possible to enhance the modulation bandwidth of PC-LEDs by employing blue filtering at the receiver to undo the effect of the slow yellow component and extract the fast blue response. Hence, extending the LED bandwidth up to 30 MHz, but at the expense of considerable loss in the received signal power [25–27].

To overcome the LED bandwidth limitation, advanced modulation techniques have been extensively adopted. The most popular advanced modulation formats used in VLC are OFDM and CAP. A comparative study highlighting the merits and drawbacks of the two modulation schemes is available [28]. In addition, a review in [7], surveys the milestone of the application of CAP modulation in VLC

has undergone, including multi-band CAP and its transition to non-orthogonal sub-bands and to the most recent developments. The adoption of advanced modulation formats such as CAP, has substantially improved the utility of highly bandwidth-limited devices. For example, work in [8] utilises a large off-the-shelf LED panel with dimensions of 60×60 cm^2 at distances up to 2 metres, achieving a data rate of 40 Mbps due to the use of multi-band CAP modulation.

While the generation of white light using PC-LEDs offers advantages in terms of reduced cost and complexity compared to RGB-LEDs. RGB-LEDs, however, offer the distinct possibility of modulating each colour independently and hence supporting parallel transmission using WDM. Moreover, the bandwidth of individual components is not limited by the colour converting material as in PC-LEDs. However, one of the main challenges with WDM is the cross-talk between the different colour components, where the energy from each wavelength overlaps, causing difficulties in separating individual wavelengths at the receiver. Such limitation often requires the implementation of independent dichroic filters, photodiodes and receiver circuits for each wavelength used, which leads to increased system complexity as reported in [11]. Other reports propose to reduce the complexity of WDM systems by utilising different colour LEDs, yet only one photodiode receiver [12]. The technique capitalises on the natural diversity offered by photodiodes based on the wavelength-dependent responsivities, which allows for the separation of the different LED wavelengths based on their different SNR ratios.

The bandwidth of a single-colour LED is fundamentally limited by its carrier lifetime and the RC time constant associated with the product of its dynamic resistance and junction capacitance. One popular variety of LEDs that treats the bandwidth limitations encountered in conventional single-colour LEDs is μLEDs. Compared to conventional broad area single-colour LEDs, μLEDs can be driven at significantly higher current densities, reducing their carrier lifetime, allowing for higher bandwidth. Moreover, since capacitances scale with the device area, the modulation bandwidth of μLEDs is not limited by its RC time constant. However, despite their significantly high modulation bandwidth, implementing μLEDs of-

ten requires aggregating a large number of μLEDs into an array. This is because the optical power given by a single μLED is quite low, due to its ultra-small area emitting area. For example, work in [3], utilises a single 50-μm diameter LED of 60 MHz 3dB- bandwidth and a commercial high-speed silicon photodiode (ultra-small area 0.12 mm^2), in addition to employing OFDM, bit and power loading to achieve a communication speed of 3 Gbps at a 5 cm link distance. Whereas, work in [29] aggregates a 3x3 40-μm LED array of 245 MHz 6dB- bandwidth and, also employing OFDM, to achieve communication speed of 4.81 Gbps at a 30 cm link distance. One reason for the increase in the communication distance is the increase in the transmitter optical power from 4.5 mW to 18 mW, from the single to the 3x3 40-μLED case, respectively.

Organic LEDs (OLEDs) are another light source used in VLC, which has garnered a lot of research interest, mainly due to their widespread use in display technologies and their simple and cost-effective manufacturing ability [30]. Nevertheless, such devices have significantly low charge mobility, typically three orders of magnitude lower than inorganic LEDs, limiting their modulation bandwidths in the range of 10's to 100's of kHz only. Despite their severe bandwidth limitation, such devices are still suitable for a wide range of prospective applications, such as the implementation of the internet of things (IoT), which only require data rates of a few Mbps. In [31], a new class of OLEDs are integrated into a real-time VLC setup employing a commercially available silicon photodiode of area 13 mm^2, achieving an error-free above 1 Mbps, without the use of any computationally complex equalisers, yet at a distance of only 5 cm.

Laser diodes light sources are often employed in VLC systems, with demonstrated Gbps transmission rates. However, despite having significantly higher modulation bandwidth than LEDs, their quality for indoor illumination remains debatable, due to the highly directional nature of their emission. Nevertheless, studies in [32] showed that the use of diffused laser light sources could provide a homogeneous illumination as with conventional LED light luminaries.

All of the sources used require drive circuits, which match the characteristics

of the device, a challenge often overlooked by designers, which will be addressed in this thesis.

VLC Receiver Light Detectors

The receiver detectors used in VLC systems are predominately either silicon-based positive-intrinsic-negative (PIN) photodiodes or avalanche photodiodes (APD). Other photodetector varieties, such as the single-photon avalanche (SPAD) photodiode, have also established themselves as one of the promising receiver technologies because of their potential for improved sensitivity. However, the dead time, finite output pulse width, and photon detection efficiency of existing SPAD still limit their bandwidth [33]. Other viable photodetectors like solar cells [34], and imaging sensors (camera sensors) [10] have also been reported. Moreover, advances in photodetectors using polymer-based materials have given rise to organic photodiode (OPD), which can be cheaply and easily fabricated and has the advantage of responsivity higher than silicon in the visible range [35]. Yet, such devices are limited by their significantly low bandwidth ($<$1 MHz) [36].

The available SNR at the receiver determines the quality of the received signal, and for a given bandwidth, the SNR is determined by the transmitted power, channel loss and the receiver responsivity and noise, which are sometimes expressed as figures of sensitivity. As in all communication systems, a compromise is required between power, bandwidth and signal quality. For example, a VLC transmitter employing traditional large-area LED can maximise the transmitted optical power, yet would have limited bandwidth. On the other hand, employing μLEDs would result in higher bandwidth, yet with reduced transmitted optical power. VLC receivers power-bandwidth compromise is no different from that of transmitters, since employing larger area photodiodes has the advantage of increasing the light collection; as such, improving the SNR, yet again limits the available bandwidth because of associated high capacitances. Another way of improving the SNR when using small area photodiodes is to use concentrators, which typically consists of a set of lenses at the transmitter and the receiver, but other implementations are also possible such as the use of luminescent concentrators [37]. The advantage of using optical con-

centrators is increasing the effective receiver area and hence, increasing the signal power without compromising bandwidth. However, such an advantage is typically at the expense of reducing the receiver field of view [13].

In the vast majority of VLC reports employing either PIN or APD receivers, the photodiode areas are small. Such systems have demonstrated high data rates primarily by employing advanced modulation formats, often at the expense of reducing the link distance to impractical distance, increasing the transmitted power, or using a focusing lens at the transmitter or the receiver. While such approaches are valid, nevertheless, on many occasions employing photodiodes with larger areas, optimised TIA design to alleviate the photodiode bandwidth limitation would have significantly improved the system capacity and may have allowed for longer transmission distances. For example, in [38], a multi-CAP VLC system is demonstrated using a bandwidth-limited OLED transmitter and a receiver consisting of a focal lens, commercially available silicon PIN photodiode of 0.8 mm^2 and a transimpedance amplifier at a distance of only 5 cm. The system aimed to show the advantage of using multi-CAP over CAP modulation, which resulted in 10% improvement in achievable data rates. A system reported in [39] is based on a single PC-LED and a receiver that consists of an optical focal lens, commercially available silicon PIN photodiode (3 mm^2) and op-amp based TIA. This system employs a combination of blue filtering, analogue passive and active post equalisation to achieve a data rate of 340 Mbps over a 43 cm link distance. In [40] a combination of pre-emphasis and active post equalisation was used to support transmission speed of 550 Mbps over 60 cm between a PC-LED and a commercially available silicon PIN photodiode (of 7 mm^2 area) and TIA. In [41], An OFDM based VLC system utilising three colour LEDs and a high-speed PIN photodiode (< 1 mm^2) achieves a 10 Gbps data rate at 50 cm aggregate distance for the three LEDs. Whereas, work in [42] reports a study on the energy efficiency between a special discrete multitone (DMT) modulation and DC-biased optical-OFDM (DCO-OFDM), the study is based on a link employing blue LED and a PIN photodiodes at 60 cm. Another report of organic-based VLC system using OLEDs and OPDs followed by commer-

cially available 50 Ω TIA is reported in [36], the link exploits artificial neural network (ANN) equalisation at the receiver to achieve a transmission rate of 350 kbps at only 5 cm.

More practical transmission distances were reported in [8], which is a system using a multi-band CAP modulation, a large off-the-shelf LED panel with dimensions of 60×60 cm^2 and a receiver consisting of a 150 mm^2 and high gain TIA, achieving a data rate of 40 Mbps at distances up to 2 metres. Work in [43] reports a VLC system using PC-LED and a receiver consisting of a PIN photodiode of area 1 mm^2 followed by a TIA at a distance of 1 metre. The work studies the effect of employing blue filtering to enhance the data transmission rate of white PC-LEDs. A common practice observed from reviewing different VLC reports is bypassing the use of a TIA at the receiver and directly capturing the signal by a high-speed oscilloscope as in [41], which is not a practical system implementation. Others resorted to the use of op-amps configured as TIAs to provide amplification at the receiver as in [39, 44], which often limits the receiver's bandwidth performance as imposed by the gain-bandwidth product of the op-amp and the photodiode capacitance [45].

Altogether, it can be concluded that there has been extensive work on modulation schemes, equalisers, spatial and wavelength multiplexing to make efficient use of the limited available bandwidth of VLC's optoelectronic devices. In addition, there have been investigations of using higher bandwidth devices such as using lasers or other custom devices such as μLEDs, which offer bandwidths significantly higher than commercially available traditional LEDs. In addition to other organic-based devices such as OLEDs and OPDs, which despite their bandwidth limitation provide other advantages in terms of cost and ease of manufacturing. Despite such appreciable efforts to improve the transmission rates in the VLC system, limited work went into the optimisation of circuits to enhance the utility of existing bandwidth-limited devices. A recent study in [14] highlighted the performance merits obtained when optimising the device selection in VLC system and the associated trade-off between the power-bandwidth performance based on device characteristics such as active area. The study showed the advantage of mutually optimising the

modulation scheme and device selection; for a link using μLEDs and commercially available photodiode, a 20 dB SNR margin or 3 times improvement in data rate can be achieved.

The work of this thesis deals with the optimisation of VLC transmitters and receivers for high-speed data transmission, considering much of others work highlighted in this section. The structure of this thesis and its contributions are presented in the following two sections.

1.2 Thesis Structure

This thesis is in eight chapters and one appendix. In addition to this chapter, Chapters 2 and 5 are literature reviews of the relevant circuit techniques used in this thesis and described in the four work chapters: 3, 4, 6 and 7. A brief summary of each chapter is in the listing below.

- Chapter 1 is an introductory chapter that gives a general introduction to the subject of visible light communication, and it highlights some of the downsides with the currently reported VLC systems from which the motivation of the work in this thesis was drawn. The chapter also describes the research and sets an outline for the thesis. Finally, it lists the outcome of this research in terms of key contributions to knowledge and publications.

- Chapter 2 introduces the concept of negative impedance and reviews the key circuit techniques used for the generation of negative impedance, in particular negative capacitance, including their wide-ranging applications. Furthermore, it classifies the key negative impedance circuit techniques as circuit configurations based on negative impedance converters and others that exploit the Miller effect. Numerous reports of circuit realisations of each technique were summarised and critically assessed. The studies of this chapter inspired the research into new negative capacitance-LED bandwidth extension technique of Chapter 3 and also the new photodiode bandwidth extension Linvill based circuit of Chapter 7, proposed to generate negative resistance for the neutralisation of the photodiode series resistance.

- Chapter 3, presents newly developed studies on the performance of a negative capacitance circuit reported in [46]. The chapter includes full mathematical derivations of this circuit impedance characteristics based on a simplified hybrid-π model of the bipolar devices used. The chapter also included a performance assessment of the negative capacitance circuit based on simulations of the derived equivalent circuit model. The performance analysis concluded the necessary design optimisations to obtain a stable wide-band negative

capacitance. As a proof of concept, a verification of the utility of the negative capacitance circuit was presented through measurements of the circuit constructed on a printed circuit board (PCB) using discrete components.

- Chapter 4, discusses a new LED bandwidth extension technique based on the utilisation of the negative capacitance circuit of Chapter 3. The chapter commences with a brief review of LED modelling and parameter extraction, from which the key LED bandwidth-limiting factors are identified. Then, it proceeds with an overview of the commonly used circuit techniques to extend the LED bandwidth in VLC. The chapter then describes the design philosophy of the LED bandwidth extension technique proposed, based on mathematical analysis of the impedance characteristics of the LED itself and when compensated by the negative capacitance circuit. The chapter also includes detailed simulation studies of the compensated LED impedance and pole-zero behaviour. Finally, as a proof of concept, the negative capacitance circuit is applied to extend the bandwidth of several commercially available LEDs of different colours and manufacturers within an experimental VLC test setup.

- Chapter 5, contains a comprehensive review of different transimpedance amplifier configurations. First, the chapter highlights the design challenges imposed by the large photodiode capacitance in achieving wide-band transimpedance amplifiers. Then it presents a timeline like progression of the design of transimpedance amplifiers with high sensitivity to large photodiode capacitances, including those reported for VLC systems. Based on inference from the literature review, the apparent suitability of using low input impedance TIAs as VLC front-ends was established. Hence, attention was given to discussing the operation, advantages and disadvantages of the low input impedance configurations, particularly the common base/common gate stage and the regulated cascode stage, together with modifications of each of the stages.

- Chapter 6, presents studies on the performance of the regulated cascode tran-

simpedance amplifier with ultra-high photodiode capacitances. The chapter also includes mathematical derivations, circuit analysis, and simulation studies of the regulated cascode transimpedance amplifier based on a simplified equivalent circuit model of the TIA to identify its main bandwidth-limiting factors. The conducted analysis concludes the design optimisations necessary to achieve optimal bandwidth performance. Furthermore, it identified an internal Miller capacitance as a key bandwidth-limiting factor. Hence, a design modification of the conventional RGC TIA was proposed. An independent analysis based on the mathematical derivation and circuit analysis of the equivalent circuit of the modified TIA is conducted. One section was dedicated to presenting a comparative assessment of the modified regulated cascode versus the conventional design. As a proof of concept, a verification of the bandwidth advantage of the modified RGC was demonstrated through measurements of the scattering parameters of the two TIAs constructed on a PCB using discrete components.

- Chapter 7, describes the application of the low input impedance regulated cascode TIA of Chapter 6 to enhance the bandwidth of several commercially available large-area photodiodes. The chapter includes a section describing the measurements methodology and the VLC link constructed to evaluate the bandwidth advantage of the RGC TIA, when compared to a standard resistive 50 Ω termination. This chapter also describes the modelling procedure of large-area photodiodes based on measurements of their scattering parameters, from which the impedance responses of the photodiodes were obtained. The impedance response was then used to extract the parameter values of the photodiode passive equivalent circuit model at different reverse bias conditions. The photodiode modelling identified the photodiode series resistance as an additional bandwidth-limiting factor. Finally, the chapter describes a proposal of a new photodiode bandwidth extension circuit technique based on using the Linvill negative impedance converter circuit to generate negative resistance in series with the photodiode series resistance; to remove its bandwidth-limiting

effect. The proposed technique is shown to provide substantial bandwidth enhancement through simulation studies of the negative resistance circuit with the RGC/modified RGC TIA and the full photodiode model.

- The final chapter, concludes the thesis and presents an outline for future work.

1.3 Key Contributions & Publications

Motivated by the limited work on optimised VLC circuits, the research work of this thesis has resulted in a number of original theoretical and design contributions towards improving the practicability of VLC systems. The advantages of the reported circuit techniques are substantiated by theoretical analysis and mathematical modelling of new electronic circuits and optoelectronic devices, in addition to simulations studies and results conducted using Advanced Design System (ADS) software. Simulation studies were then verified and supported by experimental results. A summary of the main contributions is as follows:

- Designed and optimised a negative capacitance circuit capable of generating a wide range of negative capacitances at an extensive frequency range based on circuit reported in [46]. The negative capacitance circuit was designed to comply with capacitances encountered in the LEDs used in VLC. Simulations and measurements of the circuit demonstrated its versatility for applications beyond VLC. The analytical basis of this circuit was derived and verified through simulations and measurements of the circuit constructed on a printed circuit board using discrete components, which was presented in Chapter 3.

- Proposed a new optically lossless LED bandwidth extension circuit technique. The technique uses a negative capacitance circuit in parallel with the LED junction capacitance, offsetting its bandwidth-limiting effect and extending the LED bandwidth. This is the world's first proposal to exploit such circuits in the bandwidth extension of LEDs. The design principles and necessary optimisations based on derivations of the impedance characteristics of the LED equivalent passive circuit model and the negative capacitance circuit are described in Chapter 4.

- Applied and experimentally validated the negative capacitance circuits and their use to enhance the bandwidth of several commercially available LEDs of different colours and manufacturers. The bandwidth advantage of the negative capacitance circuit was demonstrated by constructing a VLC link employing the raw LED versus the compensated LED. Measurement of the electro-optical response of the LED demonstrated bandwidth enhancements of up to 500% depending on the LED colour, without incurring any loss in optical power.

- Identified an internal Miller capacitance of the regulated cascode as bandwidth-limiting through detailed mathematical derivations and circuit analysis based on the simplified equivalent circuit model of the TIA.

- Developed a new transimpedance topology, based on modifications of the existing regulated cascode configuration. The new modification neutralised an inherent bandwidth-limiting Miller capacitance in the conventional design by introducing an additional cascode stage, which significantly improved bandwidth and stability. The advantages of the new transimpedance amplifier was verified through mathematical analysis, simulations and measurements of the circuits of the two TIAs constructed on PCBs as described in Chapter 6.

- Designed, constructed and verified the application of the low input impedance regulated cascode TIA to enhance the bandwidth of several commercially available large-area photodiodes of different areas and manufacturers, which is described in Chapter 7. The bandwidth advantage of the RGC TIA was demonstrated by constructing a VLC link employing the large-area photodiode followed by the RGC TIA versus a 50 Ω impedance termination. Measurement of the electro-optical response of the photodiode demonstrated bandwidth enhancements of up to 1000% depending on the photodiode area.

- Identified the photodiode series resistance as a major bandwidth-limiting element, especially when the photodiode is loaded by a low input impedance TIA. Such bandwidth limitation was verified through measurements and

modelling of several commercially available photodiodes, which led to the identification of a full photodiode passive equivalent circuit model that accurately predicts the photodiode behaviour as described in Chapter 7.

- Proposed a new circuit technique to combat the bandwidth-limiting effect of the photodiode series resistance, which is described in Chapter 7. The technique is based on using Linvill's negative impedance converter circuit to generate negative resistance in series with the photodiode series resistance, hence, offsetting its bandwidth-limiting effect and extending the receiver bandwidth. Simulation studies of the negative resistance circuit with the RGC/modified RGC TIAs and the full photodiode passive equivalent circuit model predicted substantial bandwidth enhancement of the two TIAs due to the effective neutralisation of the photodiode series resistance.

The research work presented in this thesis resulted in five publications, to date, comprising of four conference proceedings and one journal article. These publications are listed chronologically, as follows:

1. A. Kassem and I. Darwazeh, "A High Bandwidth Modified Regulated Cascode TIA for High Capacitance Photodiodes in VLC," IEEE International Symposium on Circuits and Systems (ISCAS), 2019.

2. A. Kassem and I. Darwazeh, "Exploiting Negative Impedance Converters to Extend the Bandwidth of LEDs for Visible Light Communication," 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019.

3. A. Kassem and I. Darwazeh, "Demonstration of Negative Impedance Conversion for Bandwidth Extension in VLC," IEEE International Symposium on Circuits and Systems (ISCAS), 2020.

4. A. Kassem and I. Darwazeh, "Use of Negative Impedance Converters for Bandwidth Extension of Optical Transmitters," in IEEE Open Journal of Circuits and Systems (OJCAS), vol. 2, pp. 101-112, 2021.

5. A. Kassem and I. Darwazeh, “Practical Demonstration of RGC and Modified RGC TIAs for VLC systems,” IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2021.

Chapter 2

Negative Impedance: Concept & Techniques

2.1 Introduction

The synthesis of negative impedance using active devices has been long seen as an interesting feature that could boost the performance of many applications, such as the bandwidth enhancement of amplifiers, design of active filters and non-Foster matching of electrically small antennas. There are many different techniques for the generation of negative impedance. This chapter surveys various realisations of negative impedance, where it is identified that negative impedance can either be realised by using an assemblage of active devices known as negative impedance converters (NICs) or by exploiting feedback around a non-inverting amplifier and the Miller effect. Key circuit implementations of each of the negative impedance realisation techniques are described, with a view of identifying the most suitable for applications involving high capacitance devices such as those found in VLC applications.

2.2 Negative Impedance Preliminaries

Starting with Ohm's law, applying a voltage to an arbitrary load impedance Z_L results in a proportional current flow through the load. The direction of the current flow is positive, and the impedance value is given as $Z = V/I$, where V is the applied voltage in volts and I is the current in ampere. Equivalently, passing a current through Z_L will result in voltage drop across its terminals. With an ordinary positive load, applying voltage or passing current results in power dissipation in the form of heat equals $P = IV$. However, it is possible to assemble a network of active devices that function to maintain the ratio of voltage and current across two terminals yet reverse the voltage or current polarity relative to what a positive load impedance would present. This implies that such a network presents negative load impedance for Ohm's law to stand. A negative load impedance would inject energy into the circuit in contrast to an ordinary power-consuming resistive load. The internal arrangement of the active devices in such networks determines the mechanism by which the negative impedance is generated. A network where the input and output voltages are of opposite polarity is termed a voltage inversion type. Alternatively, a network where the current at one port is inverted relative to the other port is of a current inversion type.

Negative impedance can be in the form of negative resistance, capacitance or inductance. Each can be either in a grounded or a floating form to allow for either a series or shunt connection. Negative impedance elements, including negative capacitors and inductors, are known as non-Foster elements. This name is given because such elements defy Foster's reactance theorem, which states that the driving point impedance of a passive and lossless one port network must be positive and its reactance must always strictly increase with frequency (positive slope) [47]. However, a network with active devices may not obey Foster's theorem and can have a reactance with a negative slope when behaving like a negative inductor or negative capacitor. Figure 2.1 illustrates that the reactance of a conventional capacitor and inductor has positive dX/df. In contrast, a negative capacitor and inductor show a negative dX/df. It is important to note that Foster's theorem has been derived

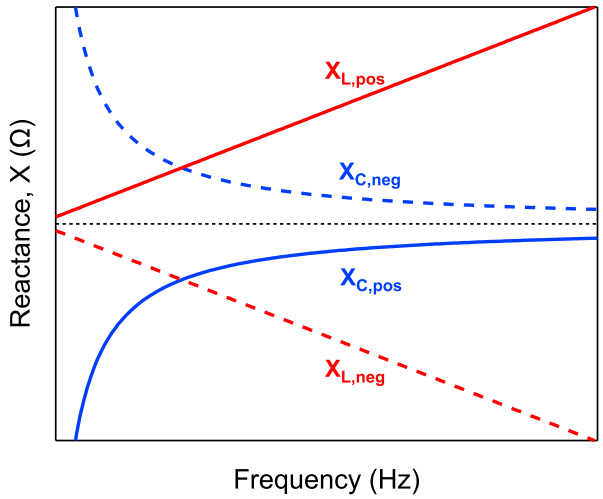


Figure 2.1: Solid: reactance of positive (Foster) reactive elements, dashed: reactance of negative (non-Foster) reactive elements

assuming no losses are present, as such negative resistance should not be termed as a non-Foster element. Nevertheless, one might say that negative capacitors, negative inductors and negative resistors form a hypothetical group of negative circuit elements that are considered linear and lossless.

Due to the anomalous characteristics of such elements, the synthesis of both negative resistance and non-Foster elements using active circuits has become highly desirable across different applications. For example, the generation of negative resistance using the cross coupled transistor pair circuit [48, 49] has been long used as the basis for the design of several digital logic circuits, such as flip-flops, and also in the design of oscillator circuits. In addition to, the use of negative resistance in the compensation of resistive losses in transmission lines in telephone repeaters [50]. Furthermore, the generation of non-Foster elements including negative capacitors and inductors using networks known as negative impedance converters (NICs) has been used extensively in the non-Foster matching of small electrical antennas to resolve the poor impedance matching of passive matching [51–55]. In addition to, the use of non-Foster elements in the synthesis of active RC filters [56, 57] and more recently, in controlling the dispersion of meta-materials [58, 59]. Whereas, the generation of negative capacitors in particular, is commonly used in enhancing the band-

width of amplifiers by neutralising bandwidth-limiting capacitances as in [60–66].

There are several means of generating negative impedance (negative resistance and non-Foster elements), all of which use positive feedback to achieve the necessary phase inversion of either the load current or voltage to obtain the desired negative impedance [67]. It was found that circuit techniques used to realise negative impedance can be classified as: (i) Networks known as NICs [50, 67–70] and negative impedance inverter (NII) [54, 71, 72], which are mainly based on two-transistor configurations that again rely on the use of positive feedback to achieve the necessary phase relationship. (ii) Circuits based on non-inverting amplifiers that utilise positive feedback and the Miller effect [60–66]. Within the scope of this work, the focus is on circuit techniques used to generate negative capacitance. However, it is worth noting that most of the techniques to be described in this chapter, with the appropriate modifications, are applicable for the generation of negative resistance and inductance.

The major challenge in designing active networks for the generation of negative capacitance is stability, mainly because the essence of operation of such networks depends on the use of positive feedback. Hence, it is crucial to identify and study the necessary conditions in achieving network stability when designing such networks. The specific stability criterion of such networks depends on the particular circuit configuration being used, yet are mainly based on ensuring that the network function does not have any poles in the right-hand side of the s-plane [55, 68, 73].

The following sections describe some of the key negative impedance circuit techniques, including their principle of operation, merits and drawbacks to identify the most appropriate means of generating negative shunt capacitance for the bandwidth extension of LEDs when used in VLC.

2.3 Negative Impedance Circuit Techniques

This section reviews some of the commonly used circuit techniques to generate negative impedance, particularly negative capacitance. The circuit techniques to be reviewed are: NICs including the well-known Linvill NIC circuit [68], the NIC operational amplifier (op-amp) implementation [74, 75] and negative capacitance circuits using the Miller effect [60–63].

2.3.1 NIC Fundamentals & Configurations

An ideal NIC is considered to be a limiting case of a linear active two-port network, referring to Figure 2.2, the limit occurs when the input impedance Z_{in} equals the negative terminating load impedance Z_L with a conversion factor K. In an ideal NIC, $K = 1$, so that $Z_{in} = -Z_L$. Two basic types of NICs can be realised; voltage inversion negative impedance converter (VNIC) and current inversion negative impedance converter (INIC). The necessary conditions to realise VNICs and INICs are described in more detail as given by the interrelationships of terminal voltages and currents of the two-port network in [69].

The initial concept of negative impedance converters was devised by Marious Latour in 1928 [76]. Merrill then introduced the first practical vacuum tube-based realisation of NICs in 1951 to generate negative resistance to compensate for resistive transmission line losses in long-line telephony repeaters [50]. In 1953, Linvill demonstrated the first transistorized version of VNIC to generate negative resistance [68], which ensued the adoption of NICs in the application of active filters synthesis [56, 57]. In 1975, Larky and Yanagisawa reported the INIC and also showed experimental results [69, 70]. Consecutively, different realisations of NICs were reported

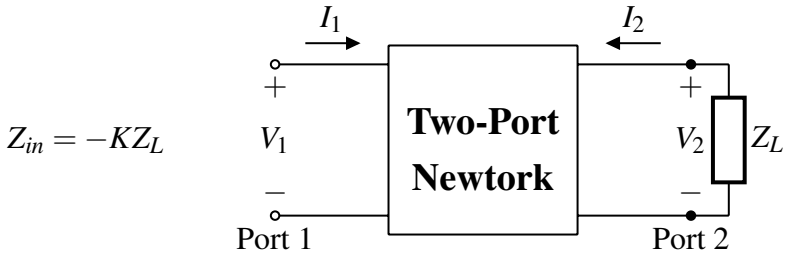


Figure 2.2: Ideal two-port network representation of NICs

either based on two-transistor configurations [52] or op-amp NIC configurations [57, 75, 77]. It is worth noting that another limiting case of the two-port network is known as negative impedance inverters (NIIs), this network can be used to generate either negative capacitance or inductance. An example of NII is reported in [66], which improves the gain of distributed amplifiers using NIIs to generate negative capacitance ameliorate the loading effects of parasitic capacitors of gain cells. This allows for increase in the gain of the distributed amplifier while maintaining the desired bandwidth performance.

In conducting the literature review, it was realised that there are tens of NIC circuit realisations, most of which include theoretical analysis or high-level concepts of the NIC proposed. In [52] a catalogue of different two-transistor based NIC realisations is reported, out of these realisations, only Linvill's NIC [68] and Yanagisawa's NIC [70] circuits were practically demonstrated. In addition to, the op-amp [74] and current conveyors [78] based NIC realisations were also practically demonstrated. This is because NICs are generally prone to become unstable. The stability of NICs has been identified as one of the main challenges hindering their practical demonstration [79, 80], mainly due to the nature of their operation, which relies on positive feedback. Hence, rigorous stability analysis is often indispensable for practical NIC circuit realisation.

As such, this section opts to focus on reviewing NIC circuits that are known to have been practically demonstrated, rather than proposals of high-level or theoretical concepts that may not be practically feasible. These circuits are the Linvill NIC and the op-amp NIC implementations. It is worth noting that the functionality of generating negative impedance by employing positive feedback is the same for all the different NIC configurations yet, the key difference often lies in the conversion factor K, which determines the conversion quality of the respective NIC circuit.

Linvill's NIC Circuits

The NIC topologies proposed by Linvill are of a voltage inversion type. In his paper, Linvill introduced two NIC varieties that were classified in accordance to their stability to be open circuit stable (OCS) and short circuit stable (SCS) [68]. Each

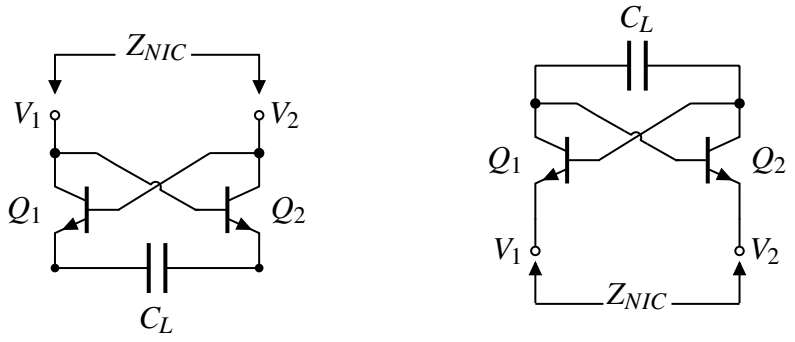


Figure 2.3: Linvill's balanced NIC implementation generating negative capacitance (a) SCS NIC (b) OCS NIC

design was constructed in balanced and unbalanced forms suggesting the negative impedance generated is either floating or grounded impedance. Grounded type NIC is designed to be connected as a shunt element, whereas the floating type NICs is to be connected as in series element to a network.

Figure 2.3a and Figure 2.3b illustrate examples of the OCS and SCS balanced Linvill NIC circuits used to generate negative capacitance, respectively. The circuits are based on a cross coupled pair of transistors Q_1 and Q_2, where the base of Q_1 is connected to the collector of Q_2 and the base of Q_2 is connected to the collector of Q_1 to form a positive feedback loop, which results in a phase inversion so that the difference in the output current $(I_1 - I_2)$ will have opposite polarity to the difference in output voltage $(V_1 - V_2)$. Hence, the load Z_L appears as negative at the respective input. In Figure 2.3, the load Z_L is C_L to generate negative capacitance, yet C_L can be replaced by either a resistor or an inductor to generate negative resistance or inductance if desirable. As previously mentioned, these circuits can also be configured in an unbalanced form to generate grounded negative impedance. Details on the unbalanced Linvill NIC realisation can be found in [51, 68], in addition to, the appropriate biasing network for both the balanced and unbalanced circuits [51, 53, 55].

The key difference between each of the realisations is in the terminals at which the input is taken and hence dictating the NIC stability condition and impedance. If the input is taken between the collector terminals, then the NIC is SCS, where the

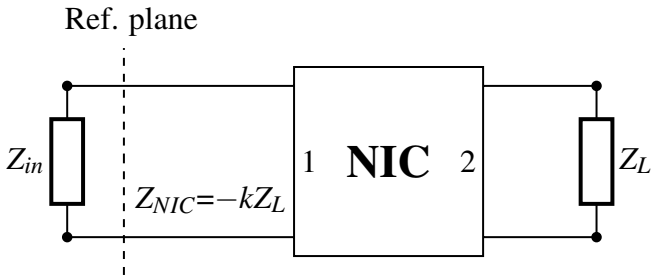


Figure 2.4: NIC stability using reference plane method as in [79]

impedance Z_{NIC} between the collectors can be approximated as in [68]:

$$Z_{NIC} = -\frac{2}{g_m} + \frac{j}{\omega C_L} \tag{2.1}$$

Where g_m is the transconductance of the transistors (assuming Q_1 and Q_2 operate at equal g_m). A special case of the SCS NIC is when $Z_L = 0$ (short), the NIC exhibits negative resistance equals $-2/g_m$, serving numerous applications such as oscillators. When the input is taken between the emitter terminals, then the NIC is OCS, where Z_{NIC} at the emitters can be approximated as in [68]:

$$Z_{NIC} = \frac{2}{g_m} + \frac{j}{\omega C_L} \tag{2.2}$$

Clearly, the main difference between (2.1) and (2.2) is the sign of the real part of the NIC impedance, which also dictates their stability conditions. The conditions governing Linvill's SCS and OSC NIC stability relates to whether the circuit should be voltage or current driven. In his paper, Linvill stated that if the NIC input is the transistor emitter, then the NIC will be OCS by ensuring it sees an open circuit at its input (current-driven) [57, 73]. However, if the NIC input is the transistor collector, then the NIC is SCS by ensuring it sees a short circuit at its input (voltage-driven) [57, 73]. In other words, the SCS condition states that the absolute value of the impedance at port 1 in Figure 2.4 should satisfy the following condition:

$$|Z_{in}| \leq |Z_{NIC}| \tag{2.3}$$

Whereas, the OCS condition states the absolute value of the impedance at port 1 in Figure 2.4 should satisfy the following condition:

$$|Z_{in}| \geq |Z_{NIC}| \tag{2.4}$$

The SCS and OCS are well-known stability conditions for NIC circuits, yet in practice, it was found that NIC circuit stability is also sensitive to device parasitics, bias networks and distributed effects from the layout. As such, the above conditions are necessary but are not always sufficient for NIC stability [55, 79, 81], since they do not take into account the nature of the NIC load and are based on assumptions of ideal circuits, which are not valid for practical NICs as was shown in [55]. Unfortunately, there is no simple stability criterion that applies to all NIC circuits, and often rigorous stability analysis is required to understand the stability limits of individual NIC circuits. In fact, classical ways of assessing the stability of microwave circuits like K-factor or μ-factor were proven to be unreliable and insufficient to assess NIC stability [82]. Other linear methods to analyse the stability of NIC circuits, including transient stability analysis or frequency domain analysis such as normalized determinant functions, were also proposed as in [55]. All these stability analysis methods are based on the Nyquist criterion to check that the NIC network function does not have any poles lying in the right half of the complex plane (RHP).

Despite the stability challenges associated with Linvill NICs, they are widely adopted in a number of applications. One of the most widely adopted and successful applications of Linvill NICs is the non-Foster impedance matching of electrical small-antennas to resolve the poor matching encountered with passive matching [51, 53, 54]. This type of matching is based on negative image modelling, which introduces negative elements $-L$ and $-C$, to cancel the corresponding positive parasitic elements L and C of the antenna equivalent model. Hence, achieving maximum power transfer within wide bandwidths, which otherwise is impossible to achieve with traditional passive matching due to physical limitations imposed by gain-bandwidth product of the antenna [81].

The quality of the non-foster impedance matching is often affected by the in-

herent $2/g_m$ component seen in (2.1) and (2.2), which accompanies the generated non-foster elements ($-C$ and $-L$). This resistive component is usually minimised by increasing the NIC transistor currents to enhance g_m, yet this approach may degrade stability and noise performance [80]. Other approaches proposed the addition of a diode-connected as a resistance to the output of the Linvill SCS NIC to offset the $-2/g_m$ component as in [59]. Sussmon-fort (2006), stated that the inherent conditional stability of NICs constrains the magnitude of the impedances that can be connected to the NIC OCS port and to the SCS port as shown in Figure 2.4. Such that, in practice, the inequalities in (2.3) and (2.4) often must be satisfied by at least a factor of two [81]. This certainly has an impact on the quality of the antenna's impedance matching, where negative elements might sometimes have unfavourable impedance levels. As such, usually careful design and optimisation are essential to achieve good matching while maintaining the NIC stability.

Razavi (2014) presents an overview of the operation and properties of Linvill's NIC circuit (also known as the cross coupled pair (XCP)) and its usage to boost the performance of a variety of analogue and digital circuit applications [48, 49]. Among these applications is the neutralisation of bandwidth-limiting capacitances to boost the bandwidth of amplifiers. An example of using Linvill NIC to improve the performance of wide-band amplifiers is reported by Han *et al.* (2012), where both negative resistance and negative capacitance are utilised to enhance the gain and bandwidth of a gigabit limiting amplifier for the application of optical receivers in [83]. The negative resistance and capacitance are realised by independent NIC stages. The first stage generates negative resistance in parallel with the limiting amplifier output load resistor, boosting the amplifier output resistance and, in turn, the amplifier voltage gain. However, this leads to a significant reduction in the amplifier's bandwidth due to the increase in the output resistance and capacitance due to the additional capacitances associated with the NIC stage. Therefore, a second NIC stage is used to generate negative capacitance to offset the additional parasitic capacitance and hence, widen the bandwidth of the amplifier.

Rashekh *et al.* (2016) proposed the use of Linvill's NIC to improve the gain-

bandwidth product of op-amps at minimal power consumption by using negative capacitance to decrease the effective parasitic capacitance at the critical nodes, as such pushing the frequency of the dominant pole to higher frequencies [65]. Whereas, recent work proposed by Kari *et al.* (2020) uses the cross coupled pair to generate negative capacitance to improve the bandwidth of a modified regulated cascode (RGC) TIA when driving a relatively large capacitive load. The proposed TIA is based on a cross coupled RGC, which is used to generate negative capacitance at the output of the amplifier to compensate for the dominant output pole, leading to 56% bandwidth enhancement in comparison to the design without the negative capacitance [84].

Hence, it can be concluded that adopting Linvill's NIC boosts the performance of amplifiers effectively. Nevertheless, it has to be noted that because the impedance presented by Linvill's NIC circuit is neither purely negative capacitance nor it is negative at all frequencies. Hence, using such compensation techniques to enhance the bandwidth of amplifiers usually requires careful design optimisation to achieve the desired bandwidth enhancement without compromising the amplifier stability.

Another application of Linvill's NIC was proposed by Galal *et al.* (2003), which improves the matching and bandwidth of electrostatic discharge (ESD) circuit of the input and output pads in complementary metal oxide semiconductor (CMOS) technology [85]. The bandwidth extension is achieved by offsetting the load capacitance seen by the ESD circuit by generating a parallel negative capacitance. More recently, NICs has also been proposed to enhance the functionality of meta-materials by controlling their inherent dispersion and losses and, as such, improving the operational bandwidth as reported in [58, 59].

Op-amp NIC Configurations

NIC implementations reported in [68–70] generate negative impedance by assembling two transistors circuits to achieve phase inversion of the input current or voltage. However, the realisation of negative impedance is not exclusive to these designs. Since negative impedance can be generated by connecting the output of an amplifier to its input in series or shunt, in the right phase relationship [67]. Hence,

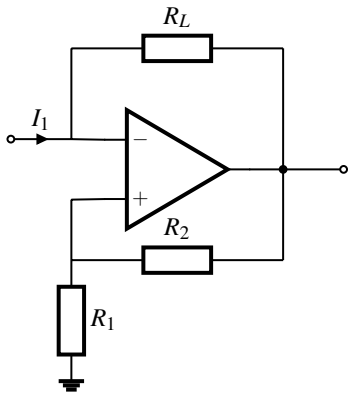


Figure 2.5: Op-amp current inversion NIC circuit

another realisation of negative impedance utilising op-amps [74, 75] or current conveyor have been reported.

NICs implemented using op-amps, offer several advantages in terms of intuitive study and fewer elements that require tuning. An op-amp based NICs was first proposed by Antoniou in [74], where two op-amp NIC configurations of a voltage inversion and current inversion type were described. These configurations then found wide application in the design of active filters [57] and in a few reports on the use of NICs for the non-Foster matching of small electrical antennas [86]. Figure 2.5 illustrates an example of a current inversion NIC used to generate an arbitrary negative resistance R_L. This arrangement provides positive feedback that alters the input current so that it's 180° out of the phase with the input voltage. This effect creates a current source with an I-V curve with a linear (resistive) negative slope, indicating the negative resistance.

An ideal op-amp is assumed, therefore no current flows into the op-amp and all the current must pass through R_L so that I_L

$$I_L = \frac{V_{in} - V_{out}}{R_L} \tag{2.5}$$

where V_{out} is given by

$$V_{out} = (1 + \frac{R_2}{R_1})V_{in} \tag{2.6}$$

hence,

$$I_L = \frac{V_{in} - (1 + \frac{R_2}{R_1})V_{in}}{R_L} \tag{2.7}$$

$$R_{in} = -\frac{R_2}{R_1}R_L \tag{2.8}$$

Although its very simple to arrange op-amps to generate negative resistance, for high-frequency operation, the non-ideal op-amp characteristics (finite input impedance, non-zero output impedance) skew the I-V curve from resistive linearity to undergo transitions from negative resistance to reactance to positive resistance, which restrict the range of usable negative resistance frequencies. Similarly, if the NIC is configured to generate negative capacitance or inductance, the synthesised negative inductors or negative capacitors will undergo frequency-dependent impedance transitions [87]. This frequency-dependent behaviour is due to the locations of poles and zeros of the op-amp transfer function. Therefore, the desired behaviour for NIC is observed only for frequencies lower than the op-amp lowest frequency pole [77]. There are several studies investigating such limitations, especially in the application of the non-Foster impedance matching of electrically small antennas, where it was concluded that using op-amp NICs to generate small negative capacitance for matching an electrically small antenna often limits the efficiency of the whole matching network. This is because the impedance of op-amp NICs presents a large negative resistance component, which severely reduces the quality of the generated negative capacitance and, in turn, limits the advantage of NICs in the application of matching small electrical antennas [77, 86, 88].

There have been studies investigating techniques to extend the usable negative impedance bandwidth of op-amp NICs. For instance, Beal *et al.* (2018) proposed a nested NIC technique to extend the operational bandwidth of op-amp NICs generating negative resistance [75]. The extension is achieved by placing a NIC as the feedback network for another NIC to push the pole and zero location of the op-amp to higher frequencies. The technique was demonstrated using a commercially available op-amp with 3 MHz unity-gain bandwidth, achieving an improvement of up to a factor of 3, yet the circuit operational frequencies are still limited to few MHz.

2.3.2 Negative Capacitance Circuits using Miller Effect

Miller effect describes a phenomenon associated with feedback circuits, which unfavourably occurs in wide-band inverting amplifiers leading to severe bandwidth limitations. Nevertheless, the Miller effect can be advantageously utilised in other applications such as capacitance multiplier circuits to implement high-value capacitors in integrated circuits without occupying a large chip area [89]. Furthermore, it can be also used to generate negative capacitances to minimise the undesirable effects of parasitic capacitances in high-speed amplifiers [60, 64, 90]. This section describes the Miller effect and how it can be used to generate negative capacitance. Moreover, it discusses several negative capacitance circuit implementations using the Miller effect.

Miller's theorem states that in a two-port linear circuit, if there is any floating impedance Z_F between the input and output node of an amplifier circuit, that it is possible to obtain an alternative circuit representation, which is equivalent in terms of impedance and voltage gain by replacing Z_F with equivalent grounded impedances at the input Z_{in} and output Z_{out} of the circuit. The values of Z_{in} and Z_{out} is determined by the circuit voltage gain A, such that $Z_{in} = Z_F(1-A)$ and $Z_{out} = Z_F(1-1/A)$. Miller's theorem is extensively used to simplify the analysis of several two-port networks such as common emitter (CE)/common source (CS) amplifiers.

In inverting amplifiers with voltage gains $-A$, such as the CS/CE stages, it is well-known that the Miller effect introduced by the local negative feedback associated with the base collector capacitance (C_μ) causes it to appear as $C_\mu(1-(-A))$ at its base, as such increasing the amplifier apparent input capacitance, which reduces the amplifier bandwidth through what is known as a pole-splitting action. The result of this action is the creation of a low-frequency dominant input pole that significantly reduces the bandwidth of the amplifier. For many years, the Cascode configuration has been used to enhance the bandwidth of CE/CS stages by shifting the frequency of its dominant input pole to higher frequencies as a result of neutralising the Miller effect presented by C_μ. Similarly, bandwidth enhancement

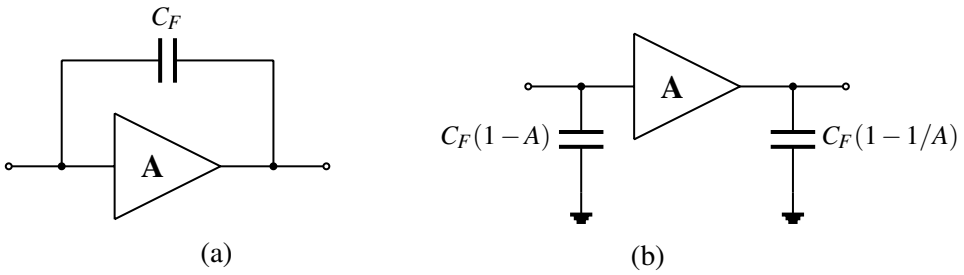


Figure 2.6: Negative capacitance circuit and its Miller equivalent circuit

techniques such as the use of bridge neutralisation [91] and C_c compensated transistors [92] was proposed to compensate for the Miller capacitance presented by C_μ in differential amplifier stages. Alternatively, negative capacitance generator circuits were also proposed to neutralise the bandwidth-limiting effect of C_μ as will be discussed [61–63, 90].

In contrast, in non-inverting amplifiers with voltage gains A, such as the common base (CB)/common gate (CG) and the common collector (CC)/common drain (CD) stages, the Miller effect can be utilised to enhance the bandwidth of the amplifier. The bandwidth enhancement is achieved by placing a feedback capacitor C_F between the input and output of the amplifier to create a positive feedback loop, which results in the generation of negative capacitance. Figures 2.6a and 2.6b illustrate an example of a non-inverting amplifier with a feedback capacitor C_F and its Miller equivalent representation, respectively. The amplifier gain determines whether the negative capacitance is created at the input or output node. With gains smaller than 1, the Miller effect creates negative capacitance seen at the output node of this stage, while slightly increasing the capacitance at the input node. With gains greater than 1, the Miller effect creates negative capacitance seen at the input node of this stage, while slightly increasing the capacitance seen at the output node. This negative capacitance can offset any internal bandwidth-limiting capacitances within the amplifier.

On the other hand, negative capacitance circuits can be used as additional circuitry that minimises unwanted capacitances when attached to any node with excessive capacitance. Figure 2.7 illustrates an example of the application of a negative

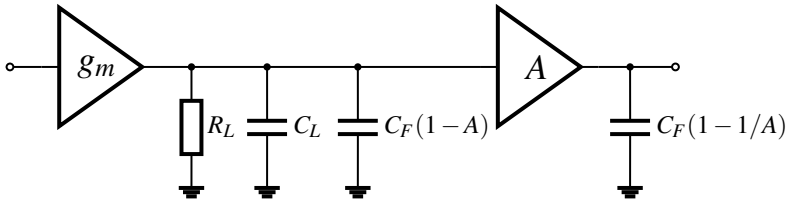


Figure 2.7: Negative capacitance circuit (A $>$ 1) attached to an amplifier output to compensate for its output load capacitance C_L

capacitance circuit to enhance the bandwidth of a single-pole voltage amplifier with output resistance R_L and output capacitance C_L. Hence, the amplifier bandwidth is dictated by $1/(2\pi R_L C_L)$. Adding a negative capacitor circuit to the amplifier output, consisting of a non-inverting amplifier with capacitive feedback, will reduce its output capacitance to become $C_L + C_F\ (1-A)$. Reducing the amplifier output capacitance will increase its pole frequency to become $1/2\pi R_L(C_L + C_F(1-A))$ and, as such, provide greater bandwidth.

Neutralising for bandwidth-limiting capacitances of amplifiers using negative capacitance circuits (parasitic capacitance compensation circuits) has been long applied to differential amplifiers [61–63, 90] and for single-ended amplifiers to [46, 93, 94]. Whilst the interest of this research work is towards single-ended negative capacitance circuits; the subsequent sections describe both key differential and single-ended negative capacitance circuits that utilise the Miller effect to give a rather comprehensive overview of the different negative capacitance circuit implementations.

Negative Capacitance for differential Configurations

In differential stages, C_μ of each of the transistors significantly increases the input capacitance as a result of the Miller effect, which leads to severe bandwidth limitation. Figure 2.8a illustrates a common simple scheme traditionally used to cancel the effect of C_μ known as bridge neutralisation [91], which exploits the symmetrical DC and asymmetrical AC signal nature of differential amplifier to counteract the effect of C_μ on the bandwidth. The technique works by adding two capacitors (C_1 and C_2) between the base and collector nodes of Q_1 and Q_2 in a cross coupled manner. The AC signal at the collectors of Q_1 and Q_2 have the same amplitude but

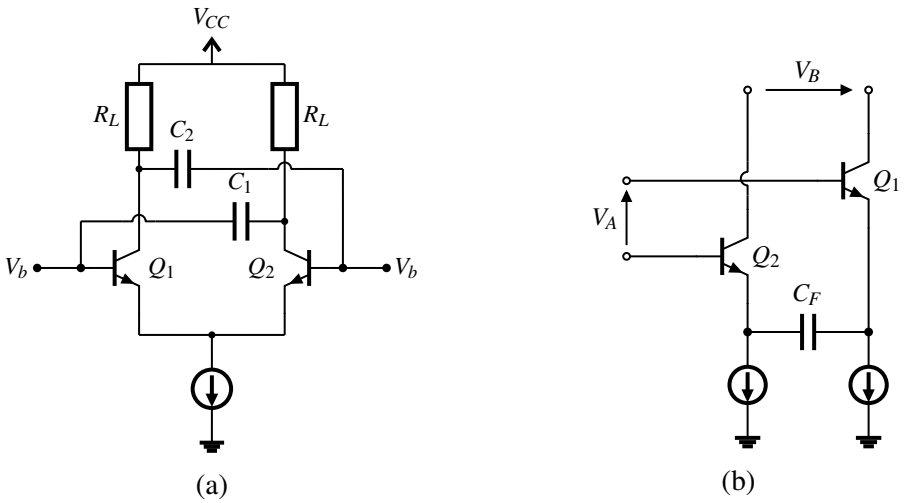


Figure 2.8: (a) C_c neutralisation in differential stages (b) Parasitic capacitance compensation circuit proposed by Wakamito in [61]

differ in phase by 180 °. Therefore, the feedback through C_1 and C_2 to the bases of Q_1 and Q_2 is out of phase with the internal feedback due C_μ. Therefore, it is possible to neutralise the Miller effect of C_μ by selecting C_1 and C_2 to have the same value as C_μ. However, in practice, this technique has a physical limitation on matching the values of C_1 and C_2 to C_μ. Moreover, discrete capacitors cannot track the variations of C_μ as a function of the device operating point, frequency, and temperature. A refinement of this technique proposed the use of C_μ of dummy transistors as the compensation capacitors instead of discrete capacitors (C_1 and C_2) to match the compensating capacitances to C_μ of the differential pair; this is known as C_c compensated transistors [91]. Nevertheless, such dummy transistors will have the unwanted effect of acting as the load capacitance for the differential pair and may potentially reduce its output pole, so it's not suitable for an amplifier in which the output pole is dominant.

Wakimoto *et al.* (1990) proposed a parasitic capacitance neutralisation circuit that can be configured to compensate either the input or the output capacitance of a differential pair depending on the way it's connected [61]. The proposed circuit is shown in Figure 2.8b, which is based on two transistors Q_1 and Q_2, with a compensating capacitor C_c connected between the emitter nodes. The input and output for this circuit are the base and collector nodes of the two transistors, respectively,

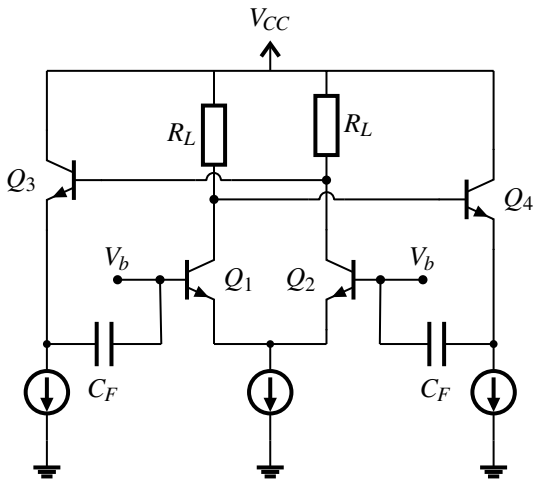


Figure 2.9: Parasitic capacitance compensation circuit proposed by Vadipour in [62]

at which the negative capacitance is seen at the collector nodes. Details on how to connect this negative capacitance circuit to the differential pair can be found in [61], which are essentially based on forming a positive feedback loop that connects the input and outputs of the differential pair. The feedback loop is formed by connecting the output of the negative capacitance circuit (collector nodes presenting negative capacitance) to the differential amplifier's input or output, depending on whether it is used to compensate for the input or output capacitance. The main advantage of this technique is its flexibility in compensating for either the input or output capacitance of the differential pair. Nevertheless, this circuit strictly needs a differential feed to generate negative capacitance and, as such, limits its application to differential stages only. Furthermore, Vadipour (1993) argued that this technique proposed by Wakamito is based on an independent active feedback network, thus requiring additional transistors, which can impose limitations on the input common-mode voltage range of the differential pair, in particular for the case when configured to compensate for the differential input capacitance [62]. Furthermore, frequency limitations of the transistors of the compensation circuit may limit the neutralisation of the undesirable capacitances, and even if the effects of the undesired capacitances are eliminated, the poles and zeroes of the compensation circuit will affect the frequency response of the amplifier and may potentially limit its bandwidth, introduce peaking and present instability.

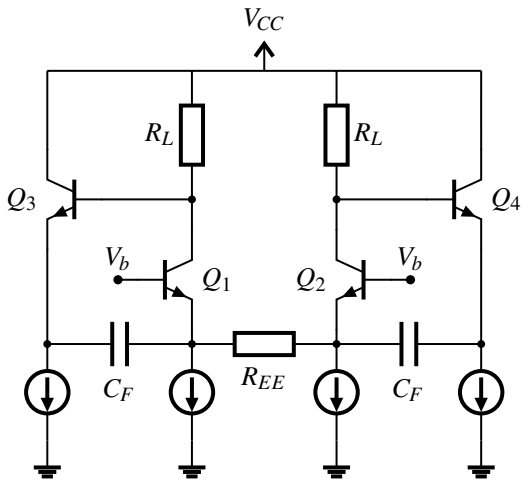


Figure 2.10: Parasitic capacitance compensation circuit proposed by Centurelli in [63]

Therefore, Vadipour proposed an alternative capacitance neutralisation technique that uses buffered differential pair without any additional stages. As illustrated by Figure 2.9, the technique uses two equals feedback capacitors C_F between the buffer outputs and the differential pair inputs, whereas the buffer inputs are connected to the differential pair outputs in a cross coupled manner to form a positive feedback loop so that C_F appears as a negative capacitance in parallel to C_μ. As such, this arrangement obtains a compensation similar to the one proposed by Wakimoto yet with no additional stages, but with the direct result of improving its frequency behaviour. Hence, this technique can provide improved capacitance neutralisation and, greater bandwidth enhancement of the differential pair. Yet again, the utility of this circuit is limited to differential stages, especially because of the cross-coupling in the feedback loop.

Figure 2.10 illustrates an adaptation of Vadipour's capacitance compensation circuit proposed by Centurelli *et al.* (2002). The proposed capacitance compensation circuit is also based on a buffered differential stage as in [62], yet C_F is placed between the outputs of the buffers and the emitters of the degenerated differential pair to close a high-frequency positive feedback loop [63]. As the frequency increases, the feedback voltage gain gets near unity resulting in a bootstrapping action, which neutralises C_μ by generating a parallel negative capacitance. In

this circuit, the degeneration resistor R_{EE} is used to enhance the differential input impedance, which provides an additional degree of freedom in the design of the feedback network. In contrast to parasitic capacitance neutralisation circuits in [61, 62], this circuit does not have to be implemented in a differential structure. One of the key features of this circuit is that the desired positive feedback is achieved without cross-coupling between transistors of the differential pair, so it can also be implemented in a single-ended form.

In comparison to other bandwidth extension techniques used to neutralise the Miller capacitance associated with C_μ, like cascoding, bridge neutralisation and C_c compensated transistors, using negative capacitance circuits based on the Miller effect, can be useful in compensating for undesirable capacitances at either the input or output, which is particularly useful if the output pole is dominant. Furthermore, when used to compensate for the bandwidth-limiting effect of C_μ in CE and differential amplifier stages, using negative capacitance circuits were shown to be more effective than traditional Cascode configurations [61, 63]. This is because negative capacitance circuits extend the amplifier's bandwidth through positive capacitive feedback that presents an anti-pole-splitting action. The result of this action, when positive feedback dominates the effect of C_μ ($C_F \gg C_\mu$), is to move the poles of the amplifier closer together to become a complex conjugate pole, where the maximum bandwidth with flat frequency response is obtained at damping factor $\zeta = 1/\sqrt{2}$. As a result, the use of positive capacitive feedback may allow for larger bandwidth enhancement than by simply increasing the frequency of the dominant input pole as a result of neutralising the Miller effect of C_μ as with Cascode configurations.

Negative Capacitance for Single-ended Configurations

The preceding section has discussed some negative capacitance circuits in the context of differential amplifiers. Out of these circuits, only the circuit proposed by Centurelli *et al.* in [63] can work as a single-ended negative capacitance circuit. This section describes the operation of other circuit realisations of single-ended negative capacitance circuits.

As previously discussed, one of the simplest realisations of a single-ended

negative capacitance circuit is by using capacitive feedback in a non-inverting amplifier as illustrated by Figure 2.6. For instance, Drew *et al.* (1996) proposed to extend the bandwidth of optical receivers by utilising capacitive feedback around a CG amplifier to generate negative capacitance at its input, which is useful in cancelling the input capacitance presented by the photodiode [60]. Whereas, Shem *et al.* (2004) proposed to improve the unity gain and phase margin of high-speed op-amps by using a compensation method based on generating negative capacitance [64]. The negative capacitance was generated using the output buffer of the op-amp with capacitive feedback, with voltage gain less than 1, as such generating negative capacitance at the output, which results in bandwidth extension of the op-amp while also improving its phase margin.

Cromer *et al.* (2006) proposed to extend the bandwidth of CMOS differential amplifiers by generating negative capacitance to compensate for their dominant output pole in a similar manner as illustrated by Figure 2.7. Nevertheless, Cromer extends the analysis of such arrangement by accounting for the frequency limitations and non-ideal behaviour of the negative capacitance circuit, such as the circuit input capacitance and output resistance, instead of assuming an ideal negative capacitor. It was shown that these non-ideal factors result in a frequency-dependent negative capacitance, which leads to a system with a complex conjugate pole rather than a simple real pole, hence, requiring careful tuning of the negative circuit parameters to obtain effective neutralisation of the load capacitance of the voltage amplifier and as such optimal bandwidth extension [90].

Golden *et al.* (2009) proposed a negative capacitance circuit with similarities to that reported by Centerulli *et al.* in [63], yet in a single-ended form [46]. Golden proposed to reduce the non-linearity or harmonic distortion in amplifiers, which occur primarily due to the gate-source (or base-emitter) capacitance (C_{gs} or C_{π}) of their output stage, by connecting a parallel negative capacitance circuit with the undesirable capacitance. Hence, reducing the net capacitance causing the distortion. Figure 2.11a illustrates the negative capacitance circuit consisting of a CC stage Q_1 and a CB stage Q_2. The circuit synthesises negative capacitance using a positive

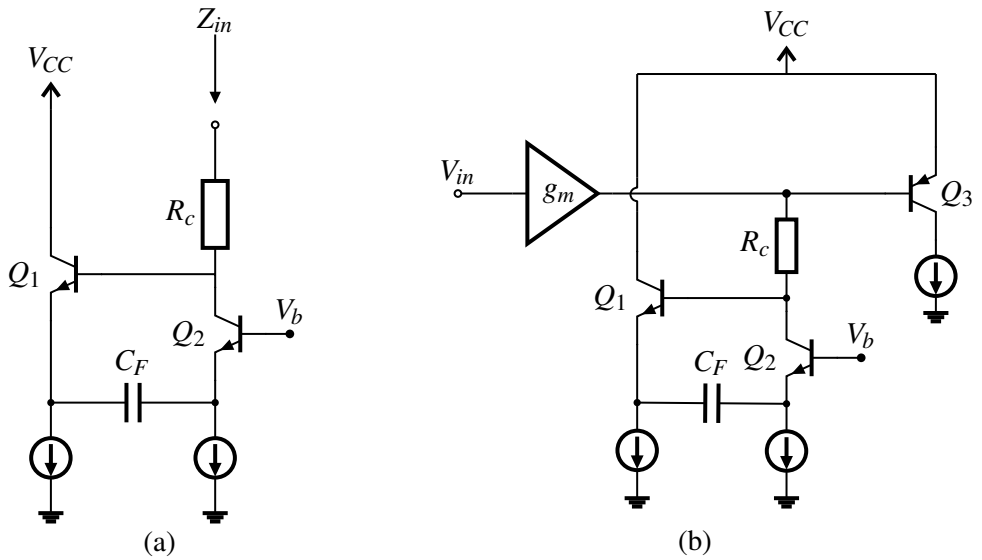


Figure 2.11: Negative capacitance circuit proposed by Golden in [46]

feedback loop that includes Q_1, Q_2 and the capacitor C_F. The input of the positive feedback loop is the base of Q_1, and the output of the positive feedback loop is the collector of Q_2, with the input and the output being tied together to perform the desired feedback. Assuming ideal transistors, the input impedance (Z_{in}) at the input node of the negative capacitance circuit is given by:

$$Z_{in} = -\frac{1}{j\omega C_F} - \frac{2}{g_m} + R_c \tag{2.9}$$

Clearly, this circuit presents an input impedance that is a combination of negative capacitance and negative resistance, where the negative capacitance is equivalent to the feedback capacitance C_F and the negative resistance component is a function of the g_m of the two transistors. Ideally, the negative resistance should be zero to obtain pure negative capacitance; alas, this is practically impossible since it is a function of g_m of the transistors. Nevertheless, increasing the transistor bias currents would reduce the negative resistance, enhancing the quality of the negative capacitance generated. Alternatively, series compensating resistor R_c can be added at the input node to neutralise the negative resistance components ($-2/g_m$) by setting $R_c = 2/g_m$. Figure 2.11b illustrates the application of the negative capacitance circuit to reduce the base-emitter capacitance of the output stage (Q_3) of

an amplifier. Here, the negative capacitance circuit is connected in parallel with the base-emitter capacitance of the output stage to shunt its base-emitter capacitance, thereby reducing distortion. The advantage of this negative capacitance circuit is that it can function independently as a negative capacitance element, provided that suitable biasing of Q_2 is achieved.

Similar circuit implementation was also proposed by Prokopenko *et al.* (2014) to compensate for bandwidth-limiting capacitances in classical amplifier configurations including the CE, CC and CB stages [93, 94]. The proposed negative capacitance circuit is based on two transistors and a capacitor assembled to achieve the positive feedback required for the negative capacitance generation. In this work, the negative capacitance is connected to the output of each of the amplifier stages to provide active frequency correction for the dominant output pole by offsetting C_μ of the transistors in the case of the CE and CB and C_π and C_L in the case of the CC stage. Prokopenko showed that the bandwidths of each of the stages could be extended by a factor of up to 2.5 without compromising voltage gain.

2.4 Summary & Discussion

The chapter has commenced with a general introduction to the concept of negative impedance in its different forms, including negative resistance, capacitance and inductance. Then it presented different methods of realising negative impedance with a primary interest in generating negative capacitance. The review included negative impedance circuit techniques based on two-port networks known as NICs and circuits using the Miller effect. In reviewing NICs, two key NIC circuit implementations were discussed, namely: the Linvill NIC, including its two varieties and the op-amp based NIC. On the other hand, negative capacitance circuits using the Miller effect were also discussed in differential and single-ended forms.

From the reviewed circuit techniques, three key similarities were observed: i) The mechanism of generating negative impedance is achieved by incorporating positive feedback in an amplifier to manipulate the current-voltage phase relation of a given load impedance, which appears negated at the amplifier input. Therefore, due to the necessity of positive feedback, negative impedance circuits are inherently unstable, which often impose some design challenges in realising high quality stable negative elements, ii) The impedance of negative impedance circuits will inevitably present a resistive component that is a function of the transistors g_m with an absolute value equals $2/g_m$, irrespective of the nature of the load to be negated. As such, when generating negative capacitance, it is important to minimise this resistive component to enhance the quality of the generated negative capacitance, iii) Some of the reviewed circuits can function independently as a negative impedance element [46, 63, 68, 74] and as such are more versatile in their applications. In contrast, others generate negative capacitance only when integrated within a specific structure like a differential stage as in [61, 62], which limits their utility to a particular application. Table 2.1 presents a summary of some of the key negative capacitance circuit discussed in the chapter.

The chapter also reviewed some of the wide-ranging applications of negative impedance circuits, such as the non-Foster impedance matching of small antennas and the compensation of undesirable bandwidth-limiting capacitances in am-

plifiers, which has inspired the idea of generating negative capacitance to alleviate the bandwidth-limiting junction capacitance of optoelectronic devices used in VLC systems (LEDs or PDs). Initial investigations of the idea predicted that using negative capacitance to enhance the bandwidth of LEDs is more appropriate, since the receiver can be more critical due to the noise added by the additional active devices, which might also be amplified by the TIA. Furthermore, the use of negative capacitance to extend the bandwidth of LEDs was thought to be promising since, in such a case, the bandwidth enhancement does not come at the expense of reduced optical power as encountered in most RC equalisers used in VLC systems. This is particularly important since the received signal level is usually weak due to limitations imposed by the free-space channel and characteristics of the receiver's photodiode, such as small area and poor responsivity.

Going by the conducted review of negative capacitance circuits, the use of NICs based on Linvill's circuit or op-amps seemed inappropriate, mainly because; firstly, the stability challenges encountered in their practical realisation, which is influenced by several factors such as the biasing network and the nature of the external load impedance connected to the NIC. This, in particular, presents a downside for applying NICs to extend the bandwidth of LEDs, since modulating LEDs require stable drive circuits. Second, the limited operational bandwidth, especially encountered with NIC based on op-amps, which could restrict the achievable bandwidth extension of LEDs. On the other hand, negative capacitance circuits based on the Miller effect, such as [46, 60–62], seemed to be more suitable since they are

Table 2.1: Summary of the key negative impedance circuits

Ref	**Topology**	**Impedance**
[68]	Cross coupled transistor pair	Floating and grounded negative R, C and L
[74]	Op-amp NIC	Floating and grounded negative R, C and L
[61]	Two transistor circuit	Negative C within a differential pair
[62]	Buffer-cross coupled differential pair	Negative C within a differential pair
[63]	Buffer-differential pair	Grounded negative C
[46]	Two transistor circuit	Grounded negative C

relatively more stable and have wide operational frequencies. As such, presenting a practically viable alternative in the application of extending the bandwidths of LEDs.

The next chapter investigates the design and optimisation of a negative capacitance inspired from circuits described in [46, 63], which is to be used as a bandwidth extension circuit to offset the bandwidth-limiting junction capacitances of LEDs.

Chapter 3

Negative Capacitance Circuit for VLC Applications

3.1 Introduction

This chapter presents the design and verification of a negative capacitance circuit proposed to cancel the effect of the large LED junction capacitance and hence, yield higher transmission speeds in VLC systems. The chapter includes newly developed studies and design optimisations of a negative capacitance circuit, reported in [46]. The negative capacitance circuit is independently modelled and simulated to understand the nature of its input impedance under different conditions such as terminating loads and bias currents. The performance of the negative capacitance circuit is evaluated through the measurement of the scattering parameters of a circuit constructed using discrete components on a PCB. Measurements show that stable high-quality negative capacitance is achieved, which suggests it to be a good candidate for the equalisation of the bandwidth-limiting junction capacitance associated with LEDs for high capacity VLC systems. Work presented in this chapter includes results presented in two conference papers[1].

[1] A. Kassem and I. Darwazeh, "Exploiting Negative Impedance Converters to Extend the Bandwidth of LEDs for Visible Light Communication," 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019.
A. Kassem and I. Darwazeh, "Demonstration of Negative Impedance Conversion for Bandwidth Extension in VLC," IEEE International Symposium on Circuits and Systems (ISCAS), 2020

3.2 Design Concept

This work proposes a new application of negative capacitance circuits; that is the bandwidth extension of LEDs, when used, for example, in high capacity VLC systems. It is well-known that the modulation bandwidth of commercially available LEDs is typically limited to a few MHz, which severely inhibits transmission rates in VLC. The bandwidth is mostly limited by the carrier lifetime and the RC time constant set by the LED dynamic resistance of the LED (r_d) and the junction capacitance of the LED (C_j). This work proposes a new LED bandwidth extension technique based on the utilisation of a negative capacitance circuit to generate shunt negative capacitance. As such, the bandwidth extension is achieved by offsetting the bandwidth-limiting effect of C_j through the introduction of the generated shunt negative capacitance in parallel with C_j, hence reducing the overall capacitance dictating the bandwidth.

The negative capacitance is synthesised through the design of a simple negative capacitance circuit [95, 96] with similarities to those in [46, 61, 93]. As discussed earlier, the main challenges in designing negative capacitance circuits arise due to their narrow operational bandwidth, hence, the frequency range at which the negative capacitance is observed is limited. Moreover, such circuits can be prone to instability, due to the nature of their operation, which incorporates positive feedback. Hence, it is important to take these factors into consideration to design a stable high-quality shunt negative capacitance.

3.3 Negative Capacitance Circuit Design

3.3.1 Negative Capacitance Circuit Design & Modelling

This section describes the design and modelling of a negative capacitance circuit reported in [46], with some differences in biasing and the input current drive. Such circuit was originally used to neutralise the undesirable intrinsic capacitances of the output buffer stage in amplifiers to improve non-linearity. This section includes newly developed design optimisations of the negative capacitance circuit suitable for the generation of negative shunt capacitances to extend the bandwidth of LEDs.

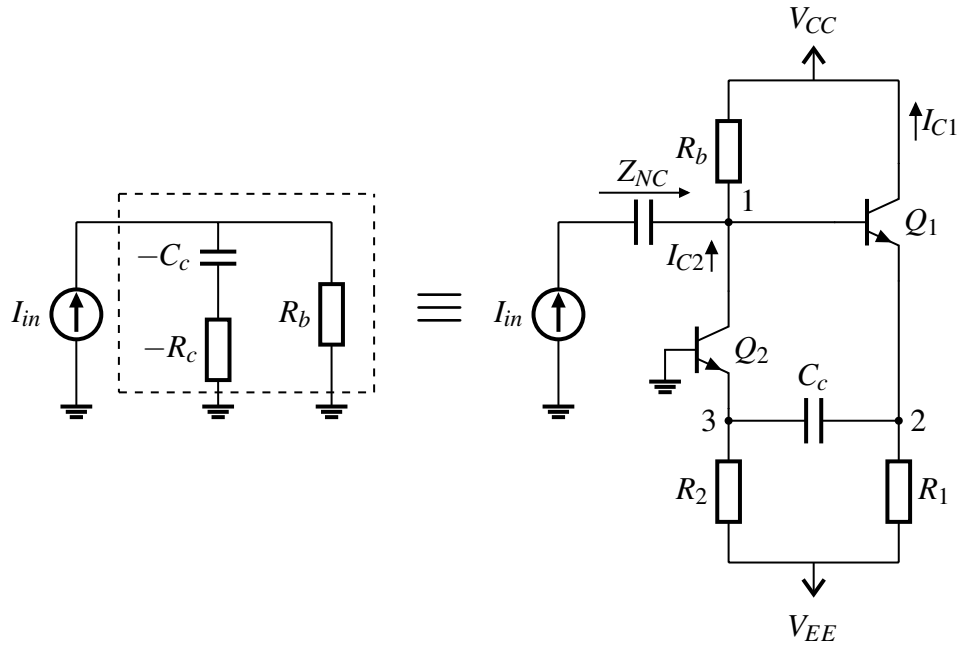


Figure 3.1: Proposed negative capacitance circuit

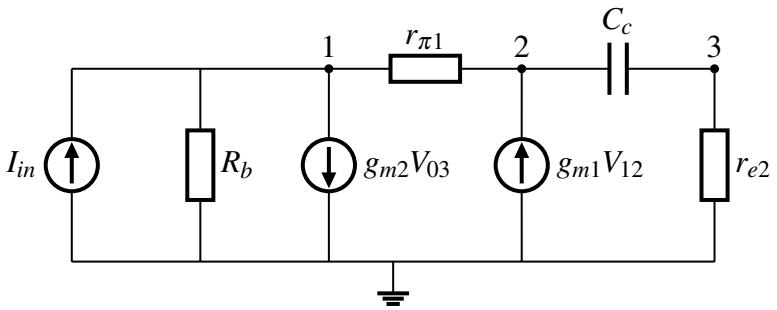


Figure 3.2: Simplified equivalent circuit model of the negative capacitance circuit

The negative capacitance circuit shown in Figure 3.1 consists of a CC stage Q_1 and a CB stage Q_2. The circuit synthesises negative capacitance using a positive feedback loop, which includes transistors Q_1 and Q_2 and the compensating capacitor (C_c). The input of the positive feedback loop is the base of Q_1 and the output is the collector of Q_2, with the input and output tied together (at node 1 in Figure 3.1 and Figure 3.2) to achieve the desired positive feedback. In other words, the AC voltage at the base of Q_1 is fed to the emitter of Q_1, hence driving one terminal of the capacitor. The other terminal is held constant by the emitter of Q_2, which is a constant voltage set by the ground minus the base-emitter voltage of Q_2. Therefore, the current flowing through C_c is due to the voltage variation on the emitter of

Q_1, but flows to the input node through the emitter of the transistor Q_2, giving the desired positive feedback.

Figure 3.2 shows the simplified equivalent model of the negative capacitance circuit in Figure 3.1. The model is based on standard low frequency hybrid-π and T-transistor models, for the CC and CB parts, similar to those in [97]. Applying nodal analysis, assuming a current source input, yields the following equations of summed currents at nodes 1, 2 and 3, respectively.

$$(1/R_b + 1/r_{\pi 1})V_1 - 1/r_{\pi 1}V_2 - g_{m2}V_3 = I_{in} \tag{3.1}$$

$$-(g_{m1} + 1/r_{\pi 2})V_1 + (1/r_{\pi 1} + g_{m1} + j\omega C_c)V_2 - j\omega C_c V_3 = 0 \tag{3.2}$$

$$-j\omega C_c V_2 + (1/r_{e2} + j\omega C_c)V_3 = 0 \tag{3.3}$$

where R_b is a biasing resistor, g_{m1}, g_{m2} and $r_{\pi 1}$ and r_{e2} are Q_1 and Q_2 transconductance and input resistances, noting that the CB input resistance is $r_{e2} = r_{\pi 2}/\beta$. This analysis makes reasonable simplifying assumptions of ideal transistors Q_1 and Q_2, with negligible internal resistive losses and capacitances and large bias resistors (R_1 and R_2), resulting in negligible loading. Consequently, a compact equation for the circuit input impedance Z_{NC} is obtained. Hence, Z_{NC} is given by:

$$Z_{NC} = \frac{g_{m2}R_b(1 + g_{m1}r_{\pi 1}) + j\omega C_c R_b(1 + g_{m1}r_{\pi 1} + g_{m2}r_{\pi 1})}{g_{m2}(1 + g_{m2}r_{\pi 1}) + j\omega C_c(1 + g_{m1}r_{\pi 1} + g_{m2}r_{\pi 1} - g_{m1}g_{m2}r_{\pi 1}R_b)} \tag{3.4}$$

Given transistors with large current gain β or $g_{m1}r_{\pi 1} \gg 1$, then to a good approximation, Z_{NC} can be simplified to:

$$\begin{aligned} Z_{NC} &= -R_c + jX_c \\ &= \left(-\frac{g_{m1} + g_{m2}}{g_{m1}g_{m2}} + \frac{j}{\omega C_c}\right) \parallel R_b \end{aligned} \tag{3.5}$$

The negative capacitance circuit presents an impedance that consists of real and imaginary parts R_c and X_c, respectively. The R_c is equivalent to a negative resistance

$-R_c$, which is a function of g_{m1} and g_{m2}. For the special case of equal transistor collector currents $I_{C1} = I_{C2} = I_C$, hence, $g_{m1} = g_{m2} = g_m$, then R_c becomes:

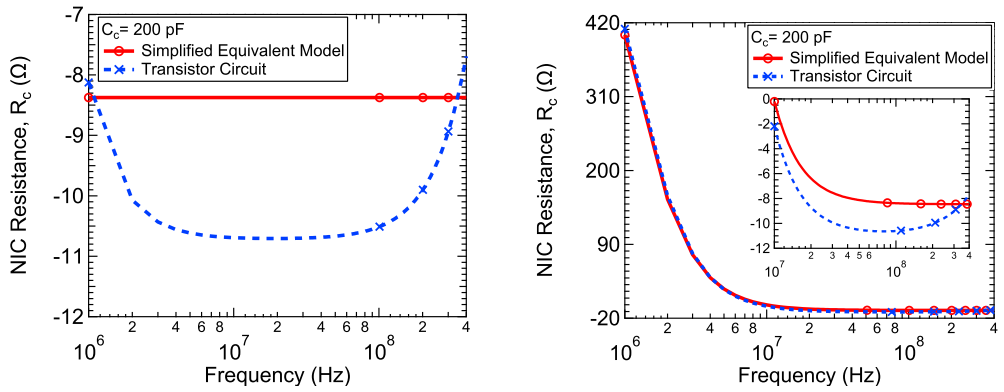
$$R_c \approx -\frac{2}{g_m} \tag{3.6}$$

X_c, the reactance of a negative capacitance $-C_c$, which in turn has the magnitude of the compensating capacitor C_c. Note the impedance of a negative capacitor $(-C_c)$ is $Z = -1/j\omega C_c$, where the voltage leads the current as a result of the current phase reversal, in contrast to the case of a positive capacitor $Z = 1/j\omega C_c$, where the voltage lags the current. Hence, Z_{NC} can be emulated by a passive equivalent circuit that is a combination of $-R_c$ in series with $-C_c$ in parallel with R_b as shown in the dashed box in Figure 3.1.

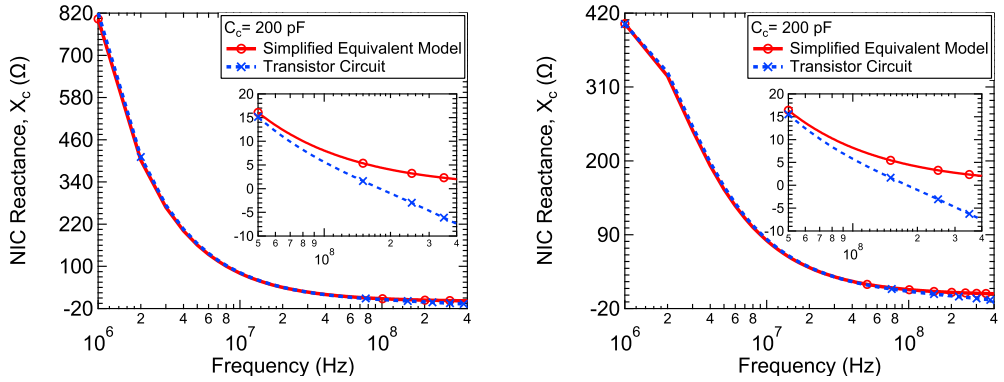
To verify the accuracy of the simplified equivalent model and analysis, the negative capacitance circuit is simulated with two silicon NPN transistors, BFR93, with transit frequency $(f_T) = 6$ GHz for arbitrary chosen $C_c = 200$ pF under $I_C =$ 6 mA. The simplified equivalent model is compared to the full transistor circuit in terms of its accuracy in predicting the negative capacitance circuit impedance components and generated negative capacitance; R_c, X_c and $-C_c$, where $-C_c$ is derived from X_c using $-1/2\pi f X_c$.

Initially, the effect of R_b on Z_{NC} is omitted, as expressed in (3.5), by setting $R_b = \infty$, this is done to clearly show the circuit impedance independently. Subsequently, the effect of R_b is considered, where $R_b = 800\ \Omega$. Figures 3.3a-3.3c illustrate the simulated impedance components; R_c, X_c and the derived $-C_c$, respectively. Note that figures shown on the left side illustrates R_c, X_c and C_c without the effect of R_b ($R_b = \infty$), whereas figures shown on the right are with the effect of R_b.

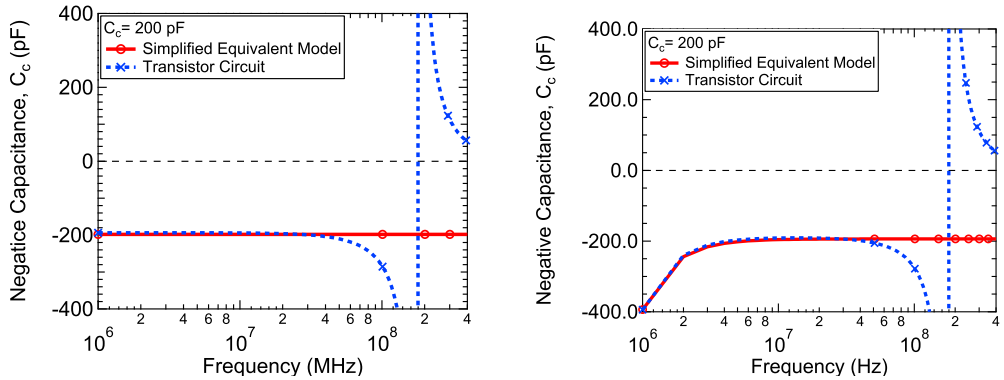
The simplified equivalent model is shown to be reasonably accurate in comparison to the full transistor circuit in estimating the magnitudes and low frequency behaviour of R_c, X_c and $-C_c$, yet is apparently limited in mimicking the negative capacitance circuit behaviour at higher frequencies. Starting with Figure 3.3a (top left), the simplified equivalent model shows that R_c is a constant negative resistance value irrespective of the frequency, which corresponds to approximately $-8.5\ \Omega$ as



(a)



(b)



(c)

Figure 3.3: Simulations of negative capacitance simplified equivalent circuit model vs. full transistor circuit (a) R_c (b) X_c (c) derived $-C_c$. Figures on the left $R_b = \infty$, Figures on the right $R_b = 800\ \Omega$

given by (3.6). Whereas, the full transistor circuit shows slightly higher magnitude of R_c of approximately $-10.5\ \Omega$, with frequency dependence at both very low frequencies and higher frequencies. This slight discrepancy in R_c is because the simplified equivalent model assumes ideal transistors, hence, it does not account

for the additional emitter lead resistances and intrinsic capacitances of both transistors, which results in enhanced R_c with such frequency-dependent behaviour, respectively. On the other hand, when considering the effect of R_b on R_c as shown in Figure 3.3a (top right), it is clear that R_b has dominating effect only at low frequencies, whereas at higher frequencies, the R_c component simplifies to be $-2/g_m$ only, as shown by the inset plot depicting similar negative resistance behaviour to that shown in Figure 3.3a (top left).

In Figure 3.3b (middle left), the negative capacitance is apparent from the negative slope of X_c. The simplified equivalent model and full transistor circuit appear to coincide at all frequencies, yet such agreement is only at low frequencies. In fact, by inspecting the inset plot at high frequencies, it is clear that the two curves are different, where the simplified model curve continues to exhibit $-1/j\omega C_c$ gradient, hence, a consistent negative capacitance behaviour. Nevertheless, the full transistor circuit slowly deviates from $-1/j\omega C_c$ gradient to become negative, which suggests that it ceases to show negative capacitance behaviour. On the other hand, similar behaviour can be observed when considering the effect of R_b on X_c as shown in Figure 3.3b (middle right), yet the only difference is in the low frequency magnitudes of X_c when compared to X_c without the effect of R_b, which suggests that R_b might be imposing a low cut-off-frequency beyond which the negative capacitance is observed.

The behaviour observed in simulations of X_c is directly reflected in the derivation of $-C_c$ shown in Figure 3.3c (bottom left). Clearly, the model gives an accurate prediction of the magnitude and behaviour of $-C_c$ at low frequencies, yet fails to show the high cut-off-frequency of the generated negative capacitance in comparison to the full transistor circuit. The simplified model shows that $-C_c$ is a constant value irrespective of frequency, in practice, this is not achievable, merely due to resonance effects caused by the contact inductances of the non-ideal transistors. As such, these resonance effects limit the frequency range at which $-C_c$ is observed and beyond which the negative capacitance behaviour ceases, as depicted by the resonance frequency in the full transistor circuit. Noting that the high cut-off-frequency

of the generated negative capacitance is dependent on the value of the generated $-C_c$ and transistor contact inductances as will becomes evident in the next section. On the other hand, when considering the effect of R_b on C_c as shown in Figure 3.3b (bottom right), it is clear that it only has an effect on the very low frequency behaviour, where $-C_c$ appears to be scaled but only up to 2 MHz. The significance of R_b on the low cut-off-frequency will be studied in more detail in the next section.

Based on simulations of the negative capacitance simplified equivalent model versus full transistor circuit, it can be concluded that (i) The simplified model is reasonably accurate in predicting the magnitude and low frequency behaviour of its impedance components R_c and X_c (ii) The model fails to reflect the high cut-off-frequency of the generated $-C_c$ (iii) The effect of R_b is apparent only at low frequencies, which reduces its significance on the overall performance, yet its effect will be further evaluated in the next section.

From these conclusions, it can be inferred that the simplified equivalent model can act as a good starting point in designing the negative capacitance circuit, yet a more complex model is required to correctly estimate the frequency range of $-C_c$.

3.3.2 Semi-Empirical Negative Capacitance Circuit Model

Initial investigation showed that the simplified negative capacitance equivalent circuit model shown in Figure 3.2 presents a reasonably accurate prediction of Z_{NC} at low frequencies, yet it fails to reflect the high cut-off-frequency of the generated negative capacitance, when compared to the full transistor circuit. Hence, the simplified negative capacitance circuit model is extended to a semi-empirical model. Figure 3.4 shows the extended model including the intrinsic parasitic components of both Q_1 and Q_2, namely the base and emitter contact inductances and the emitter contact resistances denoted as L_{b1}, L_{b2}, L_{e1}, L_{e2} and R_{e1}, R_{e2}, respectively. Collector contact inductance and resistance are ignored for simplicity and since their small values, in comparison to the base and emitter contacts, have negligible effect.

To verify the accuracy of the semi-empirical circuit model, the model is compared to simulations of the full transistor circuit under the same test conditions as previously conducted for the simplified equivalent model case (same transistors,

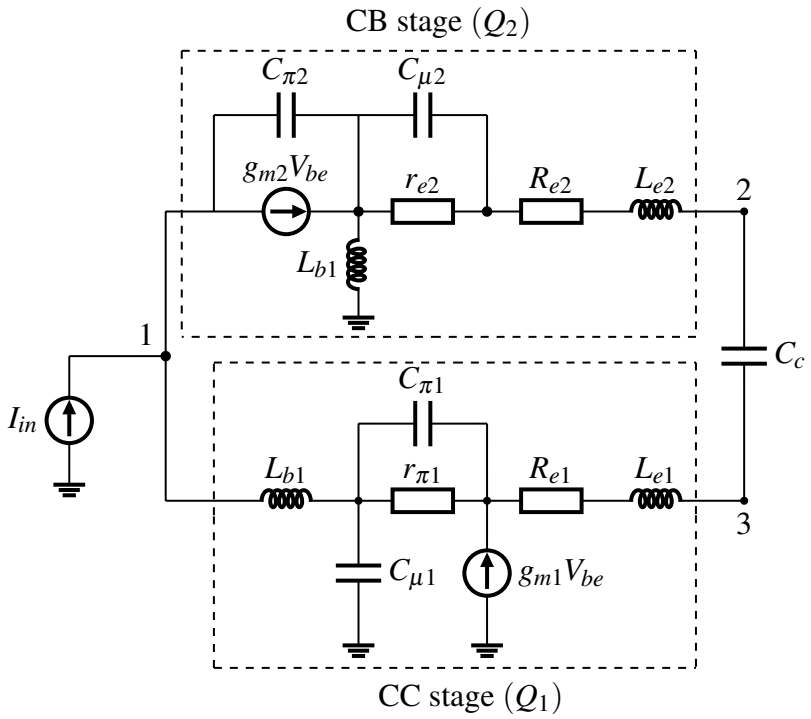


Figure 3.4: Semi-empirical equivalent circuit model of the negative capacitance circuit with reference to nodes in Figure 3.1

bias current and C_c). The parameter values of the semi-empirical circuit model were obtained by curve fitting the model to simulations of the full transistor circuit as presented is in Table 3.1. The model was then compared to the full transistor circuit in the same sequence in terms of its accuracy in predicting the negative capacitance circuit impedance components and generated negative capacitance; R_c, X_c and $-C_c$ again with and without the effect of R_b.

Figures 3.5a-3.5c illustrate the simulated negative capacitance circuit impedance components; R_c, X_c and the derived $-C_c$, respectively. Again Figures shown on the left side illustrates R_c, X_c and C_c without the effect of R_b ($R_b = \infty$), whereas Figures shown on the right are with the effect of R_b. Simulations of the semi-empirical circuit model shows excellent agreement with the full transistor circuit. Starting with Figure 3.5a (top left), the semi-empirical model improves the prediction of the R_c behaviour, showing the correct magnitude and slight variations in the frequency behaviour. This is because the effects R_{e1} and R_{e2} are considered.

In Figure 3.5b, showing X_c with and without the effect of R_b, it can be seen that

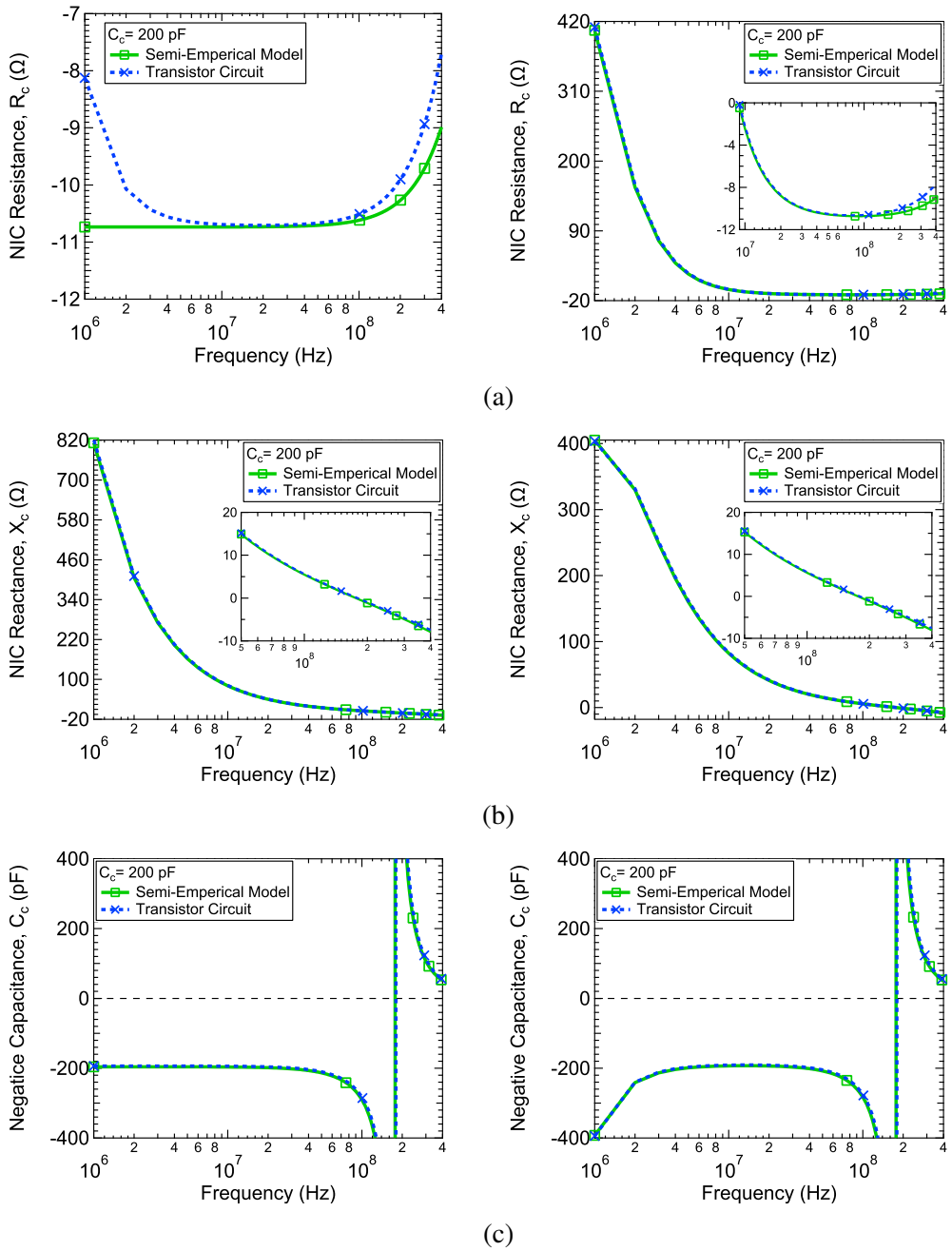


Figure 3.5: Simulations of the negative capacitance circuit semi-empirical vs. full transistor circuit (a) R_c (b) X_c (c) derived $-C_c$. Figures on the left $R_b = \infty$, Figures on the right $R_b = 800\ \Omega$

discrepancy seen at high frequency between the simplified equivalent model and the transistor circuit illustrated in Figure 3.3b is corrected by the semi-empirical model. Clearly, the semi-empirical model exhibits similar frequency behaviour as the full transistor circuit by showing deviation from the $-1/j\omega C_c$ gradient to become

negative, which suggests that the semi-empirical model does not present negative capacitance at these frequencies. Such behaviour is reflected in the derived $-C_c$ curve shown by Figure 3.3b, where $-C_c$ is seen to be almost constant then it shows a resonant behaviour beyond which the negative capacitance behaviour diminishes. Noting that the frequencies at which the resonance occurs is similar to where X_c goes negative for both curves shown Figure 3.3b (middle-left and middle-right). Whereas the only difference between the middle-left and middle-right Figures is the low frequency behaviour, which is a result of R_b, which modifies the $-C_c$ at low frequencies (up to 2 MHz). Hence, based on simulations of the semi-empirical circuit model versus full transistor circuit of the negative capacitance circuit, it can be concluded that the semi-empirical circuit model improves the accuracy of predicting the high frequency behaviour of the negative capacitance circuit when compared to the simplified equivalent circuit model, especially in reflecting the high cut-off-frequency of the generated negative capacitance. As such, presenting a more accurate prediction of the operational bandwidth of the negative capacitance circuit. Noting that although simulations of the model were limited to only 400 MHz, however the model validity was found to extend to above 1 GHz.

Table 3.1: The negative capacitance circuit semi-empirical equivalent circuit model parameters

Parameter	**Value**
g_m	120 mS
$r_{\pi 1}$	833.3 Ω
r_{e2}	8.33 Ω
C_π	2.5 pF
C_μ	0.8 pF
R_e	0.8 Ω
L_b	1 nH
L_e	1.3 nH

3.4 Performance Assessment based on Modelling and Simulations

In this section, the performance of the negative capacitance circuit is investigated by varying different design parameters such as I_C and C_c. This is important to assess the effect of $-R_c$ on the quality of the generated negative capacitance. Furthermore, the effect of the biasing resistor R_b is also considered to assess its loading effect on the frequency range of the achievable negative capacitance. These studies are conducted based on the simplified equivalent model shown in Figure 3.2. Subsequently, a progressively more complex equivalent model is developed by considering the effect of the non-ideal transistors. The model is developed such that the effect of each new parasitic element is evident on the performance of the negative capacitance circuit. Simulations of the model are then compared to the full transistor circuit.

3.4.1 Effect of $-R_c$ on the Quality of $-C_c$

Based on the simplified equivalent model analysis of the negative capacitance circuit, it was predicted that $-R_c$ is a function of g_m of both Q_1 and Q_2. As such, this study aims to examine the effect of $-R_c$ on the quality of the generated $-C_c$ by varying g_m. Initially, the dependence of $-R_c$ on g_m is illustrated by plotting the input resistance while varying g_m. Subsequently, the effect of $-R_c$ on the quality of the effective negative capacitance is assessed by attempting to neutralise a given positive capacitor placed at the circuit input to investigate the efficacy of the negative capacitance circuit in offsetting this capacitance. These studies are conducted by simulating the simplified equivalent circuit model of the negative capacitance shown in Figure 3.2, yet without R_b.

Figure 3.6 illustrates the dependence of $-R_c$ on g_m by plotting the input resistance at $g_m = 120$ mS, 240 mS, 480 mS and 960 mS. Clearly, the magnitude of $-R_c$ is reduced (becomes less negative) as g_m increases, which verifies the simplified equivalent model analysis conducted in the previous section as given by (3.6). It is worth noting, that $-R_c$ would appear to be slightly frequency-dependent when simulating the semi-empirical or the full transistor circuit as shown by Figure 3.5a,

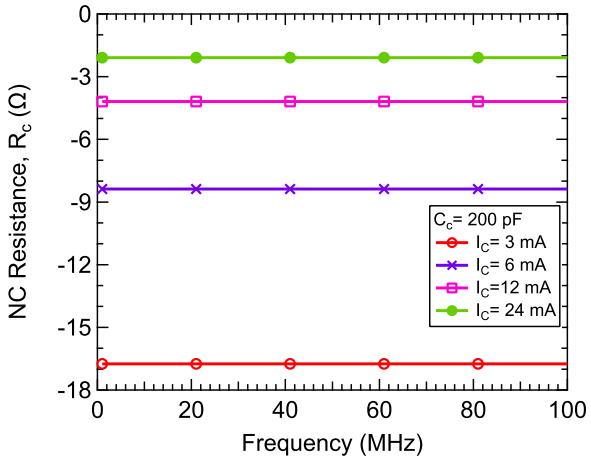


Figure 3.6: Simulations of $-R_c$ of the simplified equivalent circuit model of the negative capacitance circuit with increasing g_m

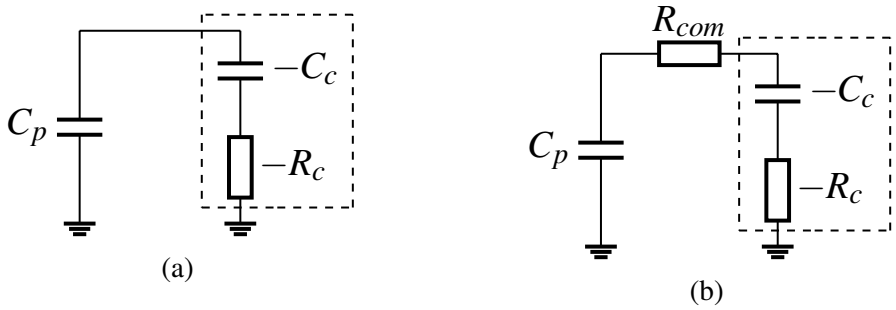


Figure 3.7: Passive equivalent circuit model of the simulation set-up used to assess the effect of $-R_c$ on the negative capacitance circuit efficacy in neutralising C_p

which will be accounted for later when assessing the effect of non-ideal transistors on the performance of the negative capacitance circuit.

As previously mentioned, the value of $-R_c$ is particularly important in dictating the quality of the generated negative capacitance and, as such, the effectiveness of the negative capacitance circuit in neutralising any undesirable capacitances. In other words, although X_c is independent of g_m as given by (3.5), yet the quality of the overall negative capacitance seen at the circuit input is affected by g_m. Since Z_{NC} is a combination of a resistive and a capacitive component. Therefore, to have a high quality effective negative capacitance, it is essential to reduce $-R_c$ to obtain the closest to a purely capacitive impedance as possible.

The effect of the inevitable $-R_c$ on the quality of the generated negative capac-

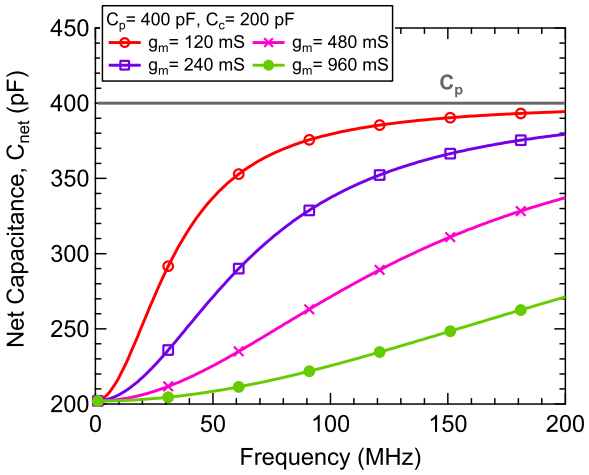


Figure 3.8: Simulations of the net capacitance C_{net} at varying g_m

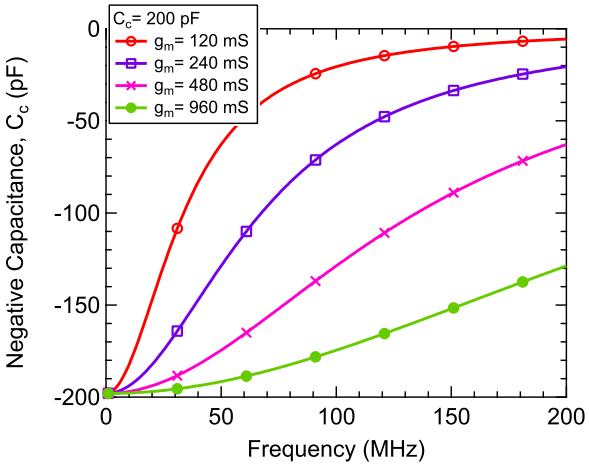


Figure 3.9: De-embedded effective negative capacitance at varying g_m

itance is examined by simulating the negative capacitance circuit simplified equivalent circuit model with a capacitor C_p placed at its input, so that Z_{NC} consisting of $-C_c$ in series with $-R_c$ appears to be in parallel with C_p as shown by the passive equivalent model in Figure 3.7a. The value of C_p is chosen to be 400 pF and $C_c =$ 200 pF. Ideally, if Z_{NC} is a purely negative capacitance $-C_c$ and $-R_c$ is not present, then the net capacitance C_{net} resulting from the parallel combination of C_p and $-C_c$ will be C_p minus C_c. However, since Z_{NC} is not purely capacitive, so C_{net} would deviate from the ideal case, as imposed by the value of $-R_c$, as such it is important to examine the effect of $-R_c$ on the quality of neutralising C_p for different g_m.

Figure 3.8 and Figure 3.9 illustrate C_{net} and the de-embedded $-C_c$ at $g_m =$

120 mS, 240 mS, 480 mS and 960 mS, respectively. From Figure 3.8, it is clear that in all cases of g_m there is reduction in capacitance in comparison to C_p. Yet, higher values of g_m yield a less frequency dependent C_{net}, meaning that the quality of offsetting C_p for the given range of frequencies is improved, this improvement is a result of the reduction in the magnitude $-R_c$ for higher g_m. The same results can also be viewed by plotting the de-embedded negative capacitance as shown by Figure 3.9, obtained by subtracting C_{net} from the value of C_p. Clearly, it can be seen that increasing g_m provides a less varying value of $-C_c$. Again, this is because increasing g_m directly reduces the magnitude of $-R_c$ (becomes less negative). Hence, obtaining a less varying value of $-C_c$ across the operational frequency of the negative capacitance circuit.

Hence, based on the aforementioned results, it can be inferred that $-R_c$ limits the quality at which the negative capacitance circuit can neutralise any given capacitance. However, such undesirable effect of $-R_c$ can be minimised by increasing g_m, and as such, the quality of generated effective negative capacitance is improved. Nevertheless, in practice, such behaviour is not practical in terms of power consumption, since operating at $g_m = 960$ mS to obtain the best quality of neutralisation of C_p would mean that the transistors need to be biased at $I_C =$ 24 mA. Furthermore, biasing the transistors at such high I_C means that the voltage drop across R_b becomes significantly high, especially for high values of R_b. As such, the value of R_b would have to be reduced, which might affect the low frequency behaviour of the negative capacitance circuit. Furthermore, it was shown that the circuit tends to be more stable when operating at lower g_m, as shown by stability studies of several negative capacitance circuits as in [55]. For these reasons, it might not be optimal to operate the circuit at such high currents.

An alternative solution to improve the quality of the effective negative capacitance, without having to increase g_m and in turn I_C, is the addition of a compensating resistor R_{com} in series between C_p and the negative capacitance circuit as illustrated by the passive equivalent model in Figure 3.7b. In such case, the magnitude of $-R_c$ is reduced by the addition of R_{com} so that the resistance is now given by:

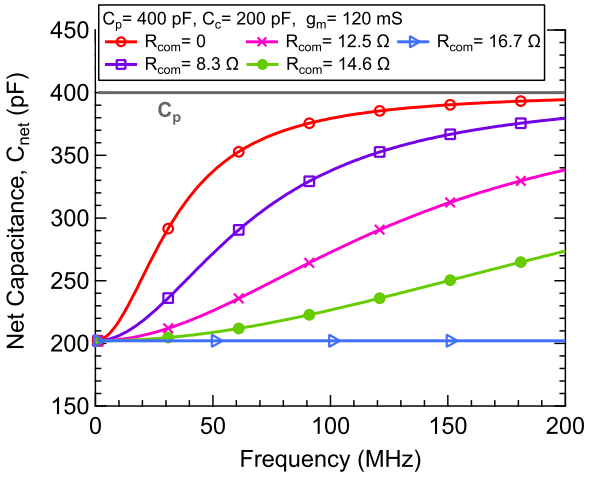


Figure 3.10: Net Capacitance at $g_m = 120$ mS with the addition of compensating resistor R_{com}

$$-R_c = -\frac{2}{g_m} + R_{com} \tag{3.7}$$

Ideally, $-R_c$ can be nullified if $R_{com} = 2/g_m$. Unfortunately, in practice, this is not the case when considering either the semi-empirical model or the full transistor circuit where R_b is present, as such limiting the complete nullification of the $-R_c$ component. The effect of adding R_{com} is investigated by simulating the simplified equivalent model with C_p at its input and R_{com} placed in series between C_p and the negative capacitance circuit. The effect of R_{com} on the quality of the effective negative capacitance is illustrated by plotting C_{net} as shown by Figure 3.10, while g_m is constantly set to 120 mS (equivalent to $-R_c \approx 16.7$ Ω) and the magnitude of $-R_c$ is reduced by the addition of R_{com}. The value of R_{com} is chosen to be 8.3 Ω, 12.5 Ω and 14.6 Ω, which is equivalent to the values of $-R_c$ if the circuit was operating at $g_m = 240$ mS, 480 mS and 980 mS (equivalent to $I_C = 6$ mA, 12 mA and 24 mA), respectively, without the addition of R_{com}. In addition to, the ideal case where $R_{com} = 2/g_m = 16.7$ Ω and such $-R_c = 0$ and this is equivalent to the case if circuit was operating at $g_m = \infty$ and $I_C = \infty$ without the addition of R_{com}.

From Figure 3.10, it can be clearly seen from the C_{net} curves that the addition of R_{com} has the same effect as increasing I_C shown in Figure 3.8. Firstly, it can be seen that C_{net} becomes gradually less frequency dependent as R_{com} is increased, this

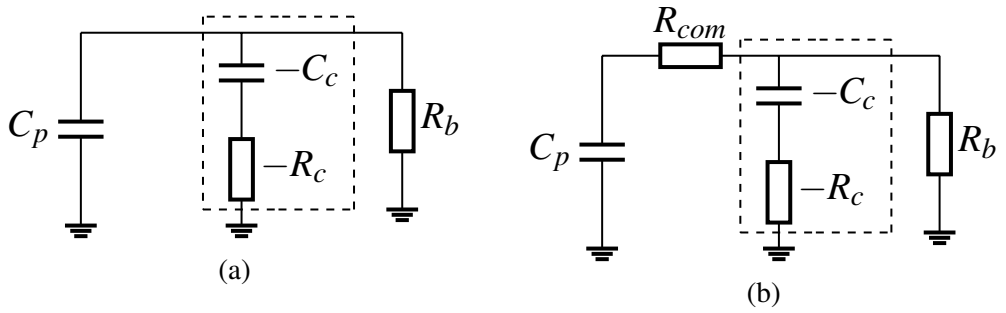


Figure 3.11: Passive equivalent model of the simulation set-up used to assess the effect of $-R_c$ on the negative capacitance efficacy to neutralise C_p

is a result of the diminishing magnitude of the negative resistance component $-R_c$. Second, in the case where $R_{com} = R_c$, it is clear that perfect partial neutralisation of C_p is obtained across the given frequency range, this is because the resistive component is completely omitted and Z_{NC} is now given by a purely capacitive component. This confirms the undesirable effect of $-R_c$ on the quality of the effective negative capacitance generated by the circuit.

3.4.2 Effect of R_b on the Frequency Range of $-C_c$

The effect of R_b on the low frequency behaviour of $-C_c$ was briefly illustrated in Section 3.3.1 by Figures 3.3c and 3.5c, where it was shown that for $R_b = 800\ \Omega$ and $-C_c = -200$ pF, $-C_c$ deviates from its expected value at very low frequency (from 1 to 3 MHz only). While, such effect falls at very low frequency, yet it is important to asses its extent for different values of R_b and $-C_c$. In this section, the effect of R_b is further investigated for different values of R_b at $C_c = 200$ pF and 20 pF. This study is conducted by simulating the negative capacitance simplified equivalent circuit model shown in Figure 3.2 for two cases where Case 1: the circuit is operating at $g_m = 960$ mS (equivalent to $I_C = 24$ mA) and in Case 2: $g_m = 120$ mS and $R_{com} = 14.6\ \Omega$ for each of the chosen value of $-C_c$. The negative capacitance circuit is specifically examined in these two cases to further investigate the effects of $-R_c$ on the quality of the effective negative capacitance, yet while considering R_b for the two scenarios where the circuit is operating at high g_m (960 mS) or otherwise lower g_m (120 mS), yet R_{com} is added. The simulation set-up of the two chosen cases is also illustrated by the passive equivalent circuits shown by Figure 3.11.

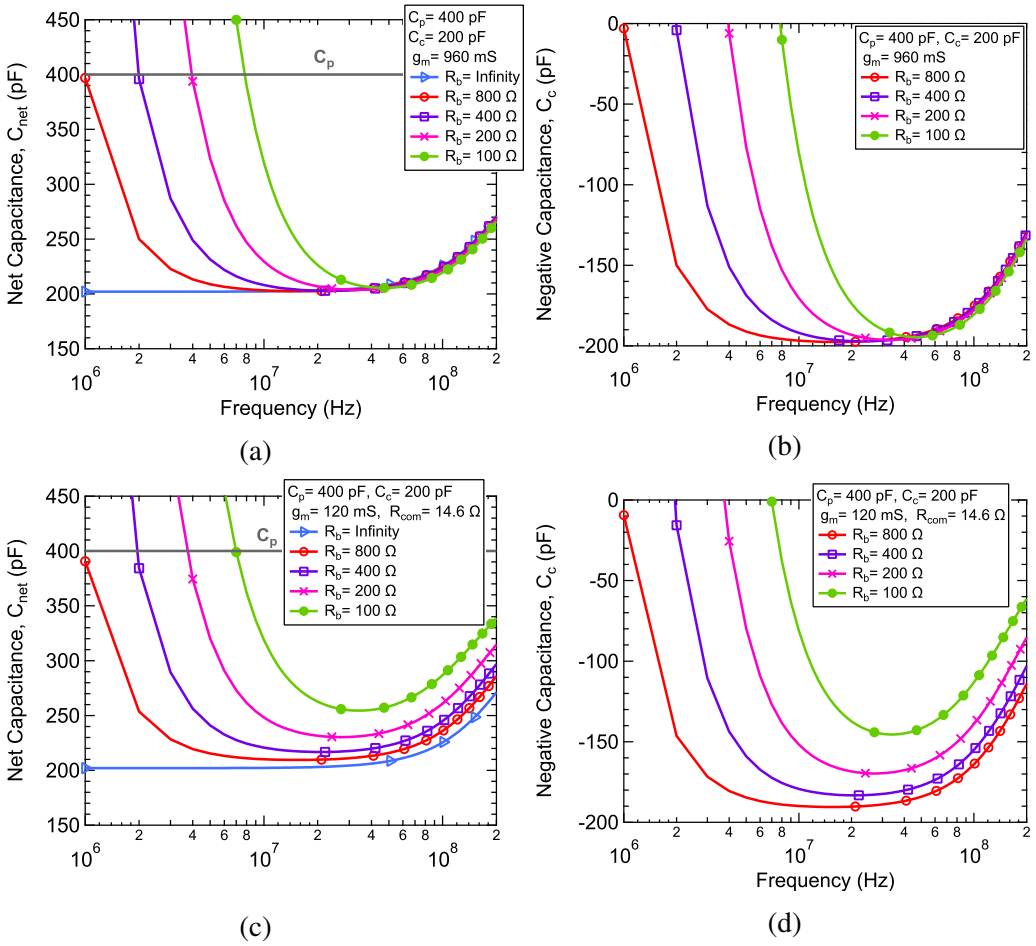


Figure 3.12: Simulations of C_{net} and de-embedded $-C_c$ of the negative capacitance circuit simplified equivalent model including R_b at $C_c = 200$ pF at different I_C (a)-(b) $g_m = 960$ mS (c)-(d) $g_m = 120$ mS, $R_{com} = 14.6\ \Omega$

Initially, the effect of R_b on the frequency range of $-C_c$, is investigated for Cases 1 and 2 for $C_c = 200$ pF and R_b is varied. Figure 3.12a and Figure 3.12b illustrate C_{net} and the de-embedded $-C_c$ for the different R_b values at Case 1, respectively. Whereas, Figure 3.12c and Figure 3.12d illustrate C_{net} and the de-embedded $-C_c$ for the different R_b values at Case 2, respectively.

From Figure 3.12a, illustrating Case 1, it is clear that C_{net} shows reduction in C_p for all value of R_b. Nevertheless, the low cut-off-frequency at which the reduction of C_p is observed is different depending on the value of R_b, where clearly reducing R_b shifts the low cut-off-frequency of the generated negative capacitance to higher frequencies. That said, R_b does not affect the circuit behaviour at higher

frequencies. The same behaviour can be viewed by plotting the de-embedded $-C_c$ shown in Figure 3.12b, where it can be clearly seen that reducing R_b increases the low cut-off-frequency at which $-C_c$ is observed to approximately 8 MHz for the worst case where $R_b = 100\ \Omega$, whereas, the high-frequency behaviour is clearly independent of R_b.

From Figure 3.12c, illustrating Case 2, it is clear that C_{net} shows reduction in C_p for all value of R_b. Nevertheless, in such case, reducing R_b does not only affect the low frequency cut-off-frequency at which the reduction in C_{net} is observed, yet also the high frequency behaviour. Where at higher frequencies, reducing R_b leads to considerable increase in C_{net} and as such degrading the efficacy of the negative capacitance circuit in neutralising C_p. The same behaviour can be observed by plotting the de-embedded $-C_c$ shown in Figure 3.12d, where clearly $-C_c$ becomes less negative for lower values of R_b. This high-frequency scaling of $-C_c$ can be explained by inspecting the passive equivalent circuits illustrating Cases 1 and 2 shown in Figure 3.11. In Case 1, the circuit operates at $g_m = 960$ mS to reduce the undesirable effect of $-R_c$ on the efficacy of the negative capacitance circuit in neutralising C_p and in this case, variations in R_b would only affect the low frequency behaviour of the circuit. Whereas, in Case 2, the circuit operates at $g_m = 120$ mS and an additional compensating resistor $R_{com} = 14.6\ \Omega$ is added to offset the effect $-R_c$ while operating at lower g_m. As previously explained, this is done for power consumption and stability reasons. While, this approach of compensating the undesirable effect $-R_c$ on the integrity of C_{net}, by the adding of R_{com}, has worked and, in fact, has shown the same effect on C_{net} as with increasing g_m, without exhibiting the undesirable high frequency scaling as shown by Figure 3.8 and Figure 3.10. Nevertheless, this was demonstrated without considering the effect of R_b. Therefore, considering R_b modifies the circuit resistive component and, as such limits the effectiveness of R_{com} in neutralising $-R_c$ and therefore, leads to this considerable high frequency scaling effect of $-C_c$, especially at lower values of R_b. As such, when operating at low g_m combined with the use of R_{com} to compensate for $-R_c$, it is important to pick high values of R_b, where the effect of the high-frequency

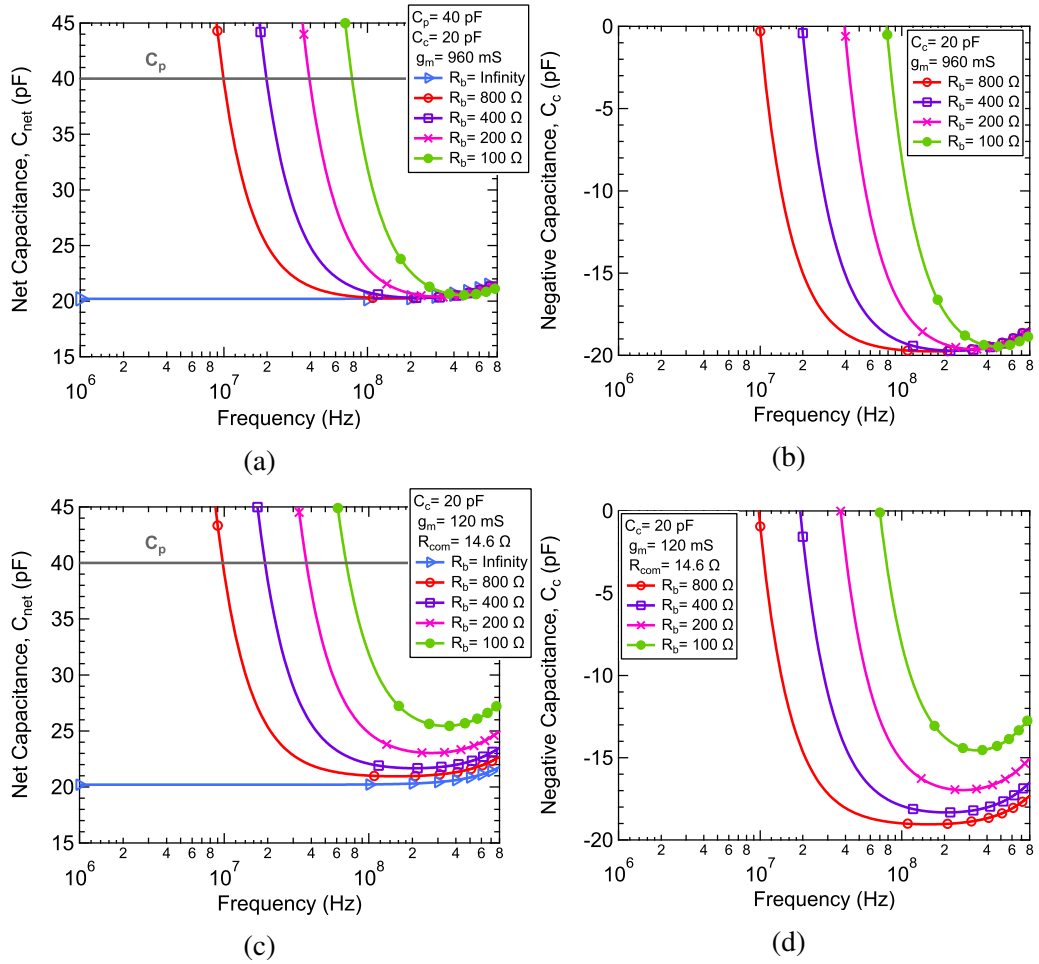


Figure 3.13: Simulations of C_{net} and de-embedded $-C_c$ of the negative capacitance circuit simplified equivalent model including R_b at $C_c = 20$ pF at different I_C (a)-(b) $g_m = 960$ mS (c)-(d) $g_m = 120$ mS, $R_{com} = 14.6\ \Omega$

scaling of $-C_c$ is insignificant. Hence, the low power consumption and improved stability advantages of operating at lower g_m are maintained without compromising the negative capacitance circuit efficacy in neutralising any given capacitance.

On the other hand, the effect of R_b on the range of $-C_c$ is also examined at $C_c = 20$ pF, this is done to demonstrate the performance of the negative capacitance circuit at lower $-C_c$ and to highlight any additional considerations that needs to be taken as imposed by the value of $-C_c$. Again the simplified equivalent model is simulated as illustrated by the passive equivalent circuits of Cases 1 and 2, shown in Figure 3.11, where C_p is now set to 40 pF. Figure 3.13a and Figure 3.13b illustrates C_{net} and the de-embedded $-C_c$ for the different R_b values at Case 1, respectively.

Whereas, Figure 3.13c and Figure 3.13d illustrates C_{net} and the de-embedded $-C_c$ for the different R_b values at Case 2, respectively.

From Figure 3.13a, illustrating C_{net}, it can be seen that C_{net} exhibits similar behaviour for the different values of R_b to that illustrated earlier for the $C_c = 200$ pF case in Figure 3.12a, where it is clear that C_{net} shows reduction in C_p for all values of R_b. Yet again the low cut-off-frequency at which this reduction is observed is dependent on the value of R_b. Whereas, the higher frequency behaviour is independent of the value of R_b. The same behaviour can be observed by inspecting the de-embedded $-C_c$ shown by Figure 3.13b, where again the reduction of R_b shifts the low cut-off-frequency at which $-C_c$ is observed to higher frequencies, yet it does not affect its high frequency behaviour. Whereas, in Case 2, where $g_m = 120$ mS and $R_{com} = 14.6\ \Omega$, again similar frequency behaviour is observed in both the C_{net} and $-C_c$ plots shown by Figure 3.13c and 3.13d, respectively. Where, clearly reducing R_b increases the low frequency cut-off-frequency of $-C_c$ and limits the efficiency of the negative capacitance circuit at higher frequencies as a result of the high frequency scaling of the generated negative capacitance.

Hence, it can be noted that the negative capacitance circuit exhibits the same frequency behaviour for $C_c = 20$ pF as with the $C_c = 200$ pF case investigated earlier. Nevertheless, the important thing to note in such a case, is the severity of the effect of R_b on the low cut-off-frequency of $-C_c$ when $C_c = 20$ pF. For instance, the low cut-off-frequency of $-C_c$ at $R_b = 100\ \Omega$ is approximately 80 MHz, which can be potentially high depending on the application at which the negative capacitance circuit is utilised. Therefore, in this case, it is important to employ higher values of R_b or possibly modify the circuit bias by employing a current mirror bias, in order to present significantly high AC impedance. Nevertheless, it is worth noting that for the application of interest, which is the bandwidth extension of LEDs in VLC systems, the range of negative capacitance to be generated is from few hundred pico-Farads to few nano-Farads. As such, the considerations outlined for low values of $-C_c$ is irrelevant, yet might be more significant if this negative capacitance circuit is to be used in other applications. Hence, based on the aforementioned ef-

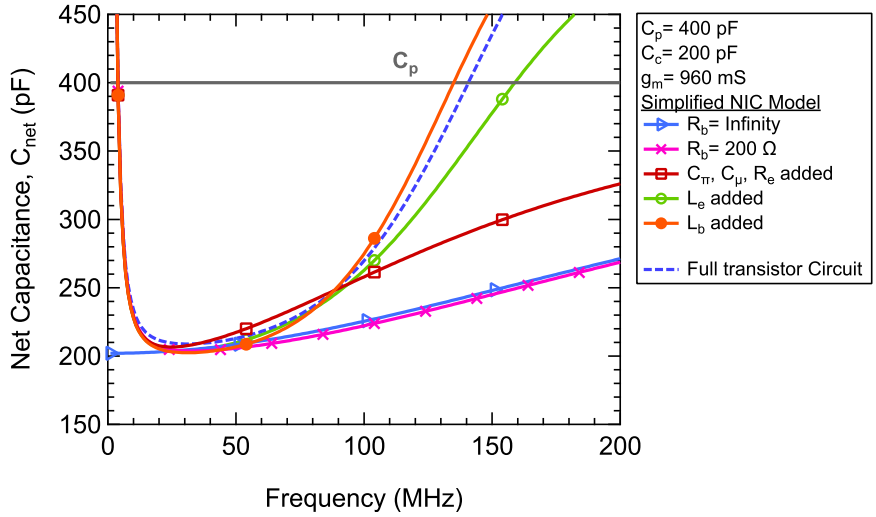
fects of R_b on the frequency range and quality of $-C_c$, it can be concluded that the significance of R_b on the negative capacitance circuit performance largely depends on its operating conditions and, more importantly, the application where the circuit is to be utilised.

3.4.3 Effect of Non-Ideal Transistors on the Range of $-C_c$

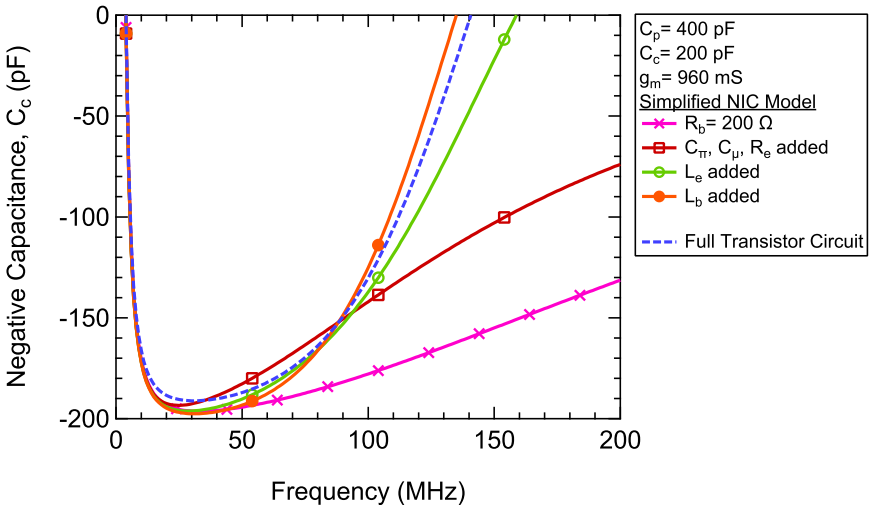
Thus far, studies of the negative capacitance circuit performance were based on the simplified equivalent model shown in Figure 3.2, assuming ideal transistors. While such studies are important to understand the circuit behaviour yet, as previously discussed in Section 3.3.1, the simplified equivalent model does not faithfully reflect the high cut-off-frequency of the generated negative capacitance. Hence, it tends to overestimate the operational frequencies of the negative capacitance circuit.

This section aims to give an insight into the effect of the intrinsic elements associated with the transistors on the operational frequency of the negative capacitance circuit. The effect of the transistor's parasitic elements is illustrated individually by progressively adding each element to the simplified equivalent circuit model, such that the effect of each parasitic element on the circuit performance is evident. This study is conducted by simulating the simplified equivalent model shown in Figure 3.2 at $g_m = 960$ mS (equivalent to $I_C = 24$ mA) for two cases where Case 1: $C_p = 400$ pF and $C_c = 200$ pF and Case 2: $C_p = 40$ pF and $C_c = 20$ pF.

Figure 3.14a and Figure 3.14b illustrate C_{net} and the de-embedded $-C_c$ for Case 1, respectively. From Figure 3.14a, it can be seen that when simulating C_{net} (pink curve) for the equivalent model without any parasitic elements, that the reduction in C_p is seen across all the simulated frequency range (200 MHz) with slight frequencies dependence. In contrast to the C_{net} curve (dashed blue) of the full transistor circuit, where the reduction in C_p is limited up to only 120 MHz. Such behaviour is also depicted in Figure 3.14b, where $-C_c$ is seen to be equal to -200 pF for the given frequency range with relatively moderate variations of approximately 25%, which comes at great discrepancy with the curve of the full transistor circuit, where the negative capacitance is not seen beyond 120 MHz. This is because in such a case, the variations in C_{net} and $-C_c$ across frequency is only caused by the



(a)



(b)

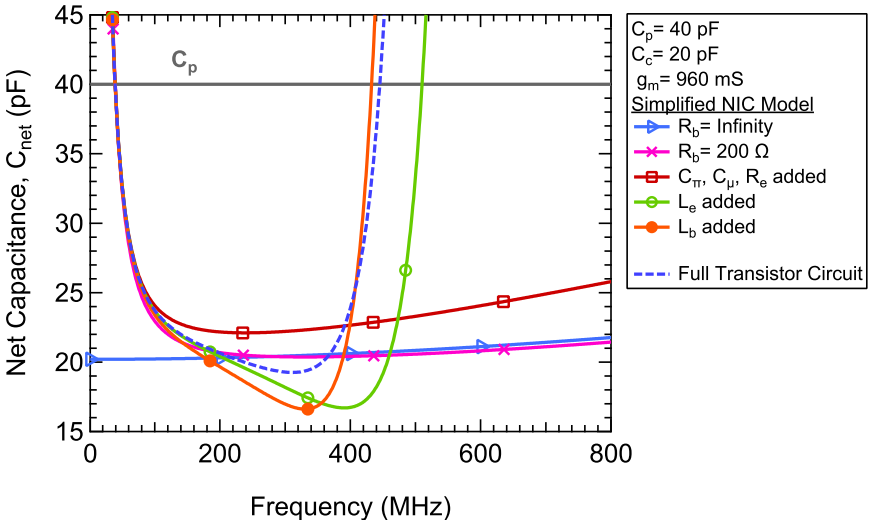
Figure 3.14: Simulations illustrating the effects of the non-ideal transistors vs. full transistor circuit at $C_c = 200$ pF (a) C_{net} (b) $-C_c$

presence of the $-R_c$ component, which causes slight degradation in the quality of neutralising C_p. Whereas, such frequency dependence of C_{net} and $-C_c$ is seen to be aggravated by the addition of the transistor capacitances C_π and C_μ and emitter contact resistance R_e (red curve), as such slightly reducing the discrepancy when compared to the full transistor circuit. Nevertheless, even by adding C_π, C_μ and R_e, the model still falls short in accurately emulating the circuit operational frequency by exhibiting negative capacitance behaviour across the whole simulated frequency range. In contrast, adding the transistor contact inductances L_e and L_b (green and

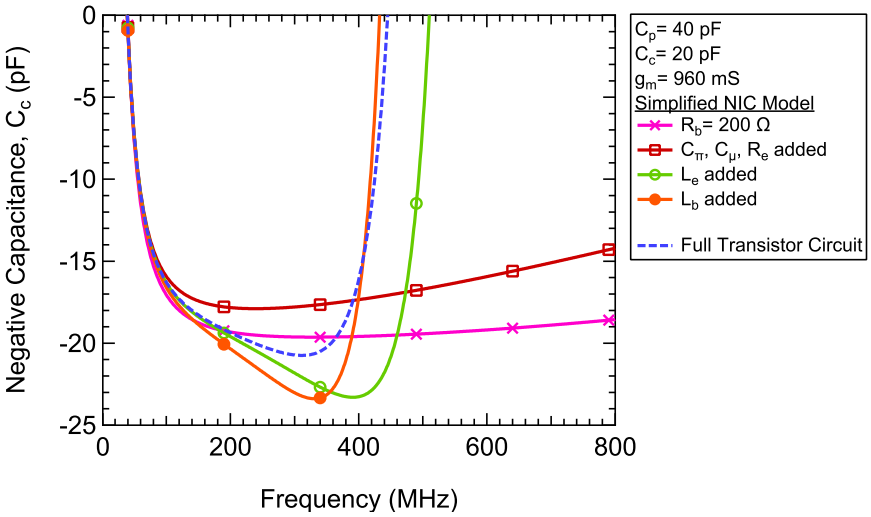
orange curves) not only increases the frequency-dependent behaviour of C_{net} and $-C_c$ but also leads to a substantial reduction in the frequency range at which the negative capacitance is observed, where the operational frequency is limited to approximately 120 MHz. Hence, closely emulating simulations of the full transistor circuit (blue dashed curve) and as such leading to a more accurate prediction of the negative capacitance circuit operational frequency. Adding the transistor contact inductances results in the resonance effect seen in Section 3.3.2 (semi-empirical model), which imposes an upper cut-off-frequency on the generated negative capacitance beyond which the negative capacitance behaviour is ceased. This high cut-off-frequency is not seen without adding the transistor inductances and is mainly dictated by the value of $-C_c$ and contact inductances.

From Figure 3.15a and Figure 3.15b, illustrating C_{net} and $-C_c$, respectively, for Case 2 where $C_p = 40$ pF and $C_c = 20$ pF. It can be seen that the C_{net} and $-C_c$ curves for the simplified equivalent model with no parasitic elements and when gradually adding each parasitic element exhibits similar behaviour to that illustrated earlier for Case 1 in Figure 3.14a and Figure 3.14b. Again, it can be observed that C_{net} and $-C_c$ of the simplified equivalent model (no parasitic effects) presents a favourable performance of the negative capacitance circuit, which can not be practically realised due to the effect of the non-ideal transistors. Whereas, adding the transistor parasitic elements results in a more than 50% reduction in the frequency range of generated negative capacitance, from more than 800 MHz to less than 400 MHz and, therefore, provides more accurate results when compared to the full transistor circuit. Moreover, it is clear that the operational frequency of the negative capacitance for $C_c = 20$ pF, for the full transistor circuit, is seen across larger frequencies (up to 400 MHz), when compared to $C_c = 200$ pF, hence, verifying that the upper cut-off-frequency at which the resonance occurs is a function of the generated negative capacitance.

Therefore, it can be concluded that there are a few important considerations to be made when designing the negative capacitance circuit; i) The simplified equivalent model is not sufficient to estimate the upper-cut-off-frequency of the generated



(a)



(b)

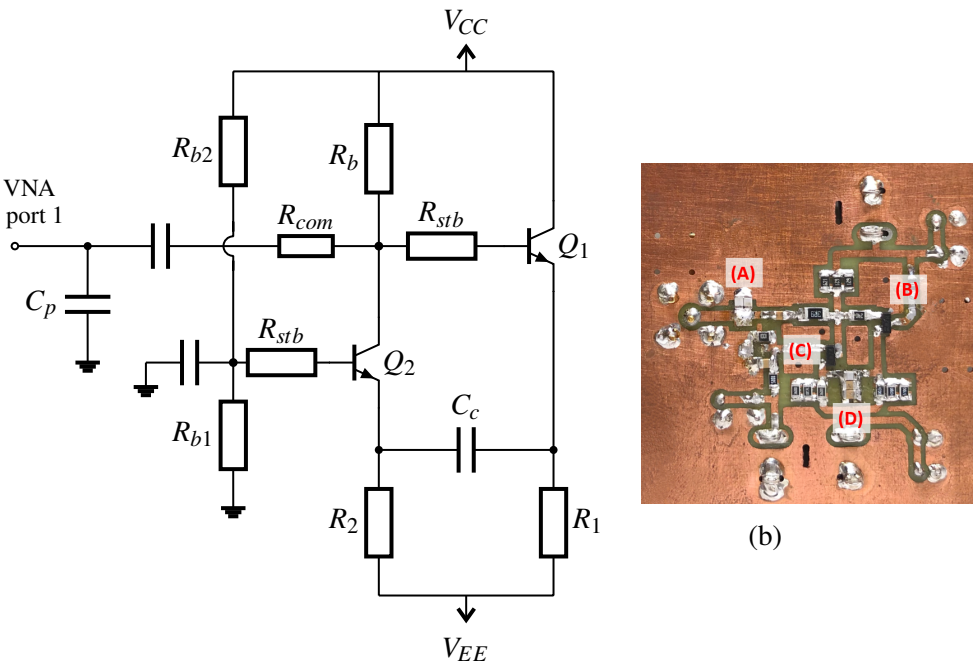
Figure 3.15: Simulations illustrating the effects of the non-ideal transistors vs. full transistor circuit at $C_c = 20$ pF (a) C_{net} (b) $-C_c$

negative capacitance, so it should be only used for preliminary design stages ii) It is important to opt for high f_T transistors with minimal contact resistances and inductances to maximise the operational frequency of the negative capacitance circuit iii) It is also important to carefully design the circuit PCB layout to reduce any additional inductances that arise from the interconnections between the transistors as such avoid further degradation in the circuit operational frequency.

3.5 Experimental Verification & Testing

Using discrete components, a stable negative capacitance was built and tested based on the negative capacitance circuit shown in Figure 3.1 with the addition of a voltage divider bias resistors R_{b1} and R_{b2} to set the base of Q_2 at a constant voltage and stabilising resistors R_{stb} at the bases of Q_1 and Q_2 as shown by the circuit in Figure 3.16a. Figure 3.16b shows the negative capacitance circuit fabricated on a FR4 double-sided PCB. The PCB is populated using silicon NPN transistors BFR93 (f_T = 6 GHz) and surface mount devices (SMD) including all resistors and capacitors. The negative capacitance circuit were tested at a fixed $V_{CC} = 9$ V and $V_{EE} = -3$ V for all measurements, yet the bias resistors R_1 and R_2 were changed to allow changes in the transistor operating current.

The performance of the negative capacitance circuit is verified by conducting one-port reflection measurements to obtain the return loss (S_{11}) of the fabricated circuit using the vector network analyser (VNA). These are then converted into the corresponding impedance parameters (Z_{11}) to obtain the generated negative capac-



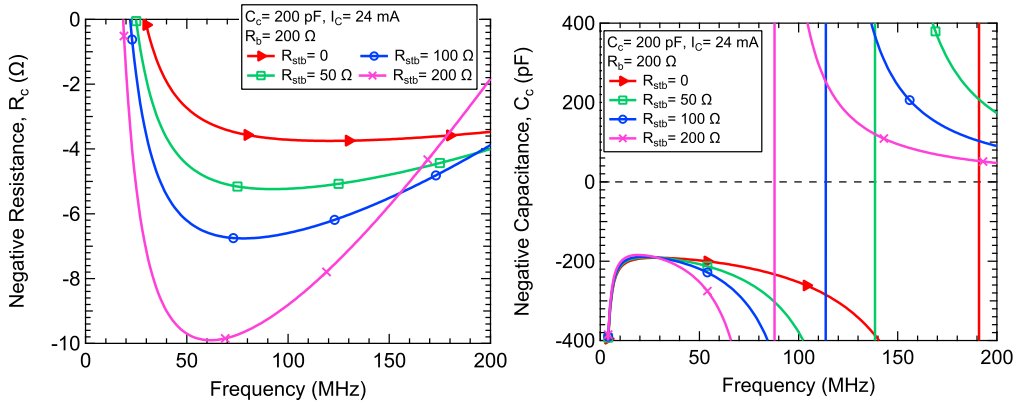
(a) (b)

Figure 3.16: (a) Full negative capacitance circuit (b) Fabricated negative capacitance circuit PCB (A) C_p (B) CC stage (Q_1) (C) CB stage (Q_2) (D) C_c

itance. The negative capacitance is measured by placing a shunt capacitance C_p at the circuit input, and the circuit is terminated with the chosen value of C_c. As discussed in Sections 3.3.1 and 3.4.1, this C_c appears at the input in parallel with C_p as negative capacitance $-C_c$ in series with negative resistance $-R_c$ as illustrated by the passive equivalent model in Figure 3.11. Hence, reducing C_{net} seen by the VNA port 1.

The stability of the negative capacitance circuit is one of the key challenges hindering its practical implementation. Such stability constraints often limit the magnitude of the generated negative capacitance to adhere to the circuit stability conditions. The stability conditions of such circuits have been extensively studied in the literature [55, 73, 79]. As discussed in Section 2.3.1, the necessary conditions for the circuit stability are mainly based on the Nyquist stability criterion so that the network function does not have any poles in the right-hand side of the s-plane. This condition is satisfied by ensuring the input loop impedance is always positive, which is achieved by having a stabilising element at the input. The nature of the stabilising element is determined by the load being converted. For instance, if the circuit is negating a load resistor R_L then a stabilising input resistance R_{in} is required so that the net resistance remains positive $R_{net} = R_{in} - R_L > 0$. Therefore, in the case of the negative capacitance circuit of Figure 3.1, to prevent any instability, C_{net} must remain positive, i.e., $C_{net} = C_p - C_c > 0$. Usually, its the undesired impedance (resistance or capacitance) to be neutralised that acts as the stabilising element. Since, C_c has to be smaller than C_p for $C_{net} > 0$, as such this condition only allows for partial neutralisation of C_p.

While C_c must always be smaller than C_p, such a condition is necessary but not sufficient for a stable operation. In practice, negative capacitance circuit stability is also sensitive to device parasitics and distributed effects from the layout. Studies in [55] showed that the length of the transmission lines of the layout in the feedback loops has a significant impact on the stability of the circuit despite their short electrical length ($\gg \lambda$). To enhance the circuit stability, it is necessary to reduce the length of the interconnections between the discrete components in the feedback



(a) (b)

Figure 3.17: Simulations of the negative capacitance transistor circuit showing the effect of R_{stb} on (a) $-R_c$ (b) $-C_c$

loop. Moreover, it was found that operating at lower g_m improves stability since it reduces the feedback loop gain. Nevertheless, lower g_m results in larger negative resistance $-R_c$ accompanied with the negative capacitance. Therefore, there is a trade-off between the degree of potential instability and $-R_c$ for most negative capacitance circuits. Another way of improving stability is by adding stabilising resistors R_{stb} at the base of Q_1 and Q_2. Yet again, the quality of the generated negative capacitance degrades when R_{stb} is added, as it increases the magnitude of $-R_c$. Whereas the DC power consumption and bias are not affected by R_{stb}, since the base current of the transistors is negligible. The choice of R_{stb} value depends on each layout. Ideally, designing a good layout should allow for stable operation at best without the addition of R_{stb} or even with small R_{stb} values to avoid compromising the quality of $-C_c$.

The effects of R_{stb} on $-R_c$ and $-C_c$ are made clear through simulations of the negative capacitance transistor circuit at $I_C = 24$ mA for $C_c = 200$ pF, without R_{stb} and for $R_{stb} = 50\ \Omega$, $100\ \Omega$ and $200\ \Omega$. Figure 3.17a and Figure 3.17b illustrate the simulated $-R_c$ and $-C_c$ for the different values of R_{stb}, respectively. In Figure 3.17a, when $R_{stb} = 0$, $-R_c$ approximates to $-4\ \Omega$, which expectantly corresponds to (3.6) enhanced by the emitter contact resistances of Q_1 and Q_2. The addition of $R_{stb} = 50\ \Omega$ results in slight increase in the magnitude of $-R_c$. Whereas, for $R_{stb} = 100\ \Omega$ and $200\ \Omega$ leads to considerable increase in $-R_c$, which would

significantly degrade the quality of the $-C_c$. This deterioration in quality of $-C_c$ is reflected from the de-embedded $-C_c$ values shown in Figure 3.17b, where increasing R_{stb} results in reduction in the circuit resonance frequency and as such reducing the frequency range at which the circuit exhibits negative capacitance. Hence, imposing a trade-off between its stability and quality of the generated $-C_c$.

In the proposed negative capacitance circuit, the layout was carefully designed to shorten the length of the transmission lines in the feedback loop. Nevertheless, the circuit appeared to be unstable when operating at high I_C. Therefore, $R_{stb} = 50\ \Omega$ were added at the bases of Q_1 and Q_2, which would slightly degrade the quality of $-C_c$ yet it guaranteed stable operation for all I_C values.

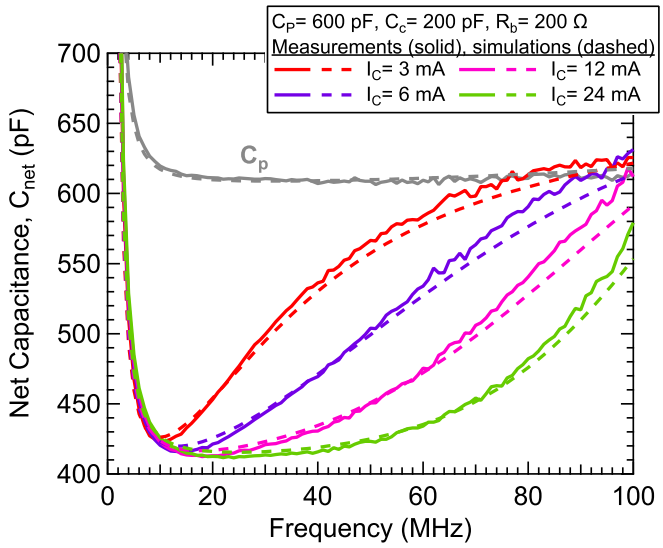
3.5.1 Verification of the Effect of $-R_c$ on the Quality of $-C_c$

The extent to which C_p is neutralised versus frequency by the negative capacitance circuit is dependent on $-R_c$. Ideally, $-R_c$ should be zero to obtain pure negative capacitance and hence, optimal neutralisation. Unfortunately, this is not practically achievable since $-R_c$ is a function of g_m, which is set by the transistors bias currents I_C. However, the magnitude of $-R_c$ can be reduced (becomes less negative) by increasing I_C, hence minimising its undesired effect on the neutralisation of C_p.

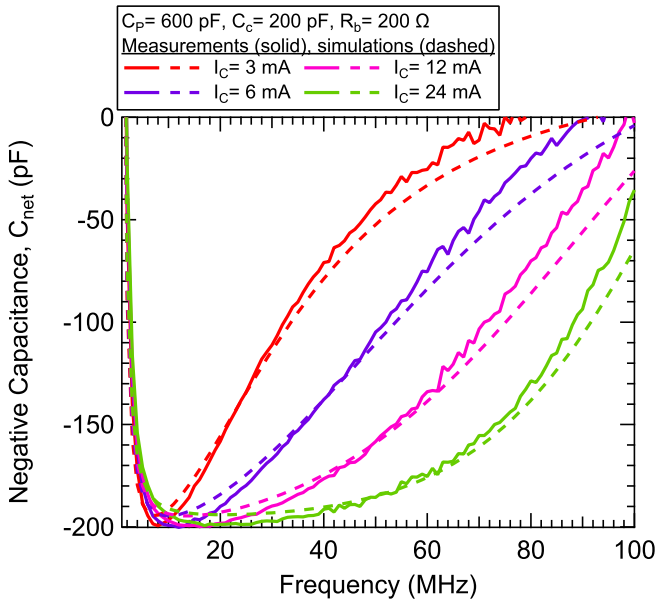
The effect of the unavoidable $-R_c$ on the quality of neutralising C_p is investigated by measuring S_{11} of the negative capacitance circuit for different I_C. Whereas, I_{C1} and I_{C2} are varied by changing the values of R_1 and R_2, whilst maintaining the appropriate bias conditions. The bias conditions for Q_1 and Q_2 are set so that $I_{C1} = I_{C2} = I_C$. Using two port parameter conversion techniques as in [97], the S_{11} values are converted into corresponding Z_{11} values to obtain C_{net}, which in turn is obtained from the reactive component $X_{in} = \Im(Z_{11})$ using:

$$C_{net} = \frac{1}{2\pi f \Im(Z_{11})} \tag{3.8}$$

The measured results are then compared to simulations, where the simulations are based on a full transistor circuit and post PCB layout. The simulation takes into account the effect of a) PCB parasitic effects, b) input transmission lines and c)



(a)



(b)

Figure 3.18: Measured and simulated C_{net} and $-C_c$ for $C_p = 600$ pF and $C_c = 200$ pF at varying I_C

capacitor models.

Figure 3.18a shows the simulated and measured C_{net} at I_C equals 3 mA, 6 mA, 12 mA and 24 mA, where $C_p = 600$ pF and $C_c = 200$ pF so ideally $C_{net=}$ 400 pF. Initially, we take a measurement of capacitance C_p while connected to the negative capacitance circuit, yet with no compensating capacitor C_c (open circuit). This mea-

surement is taken to serve as a comparator for cases where the circuit is terminated by C_c and at different I_C. Considering all cases of I_C, it is clear that all measurements closely agree with correspondent simulations. In all cases considered, the use of negative capacitance circuit results in a reduction of C_p. Expectantly, such reduction is seen to be frequency-dependent, which is due to $-R_c$. Hence, increasing I_C, reduces the magnitude of $-R_c$, giving a more uniform frequency behaviour. Figure 3.18b shows the de-embedded $-C_c$ generated by the negative capacitance circuit, which is simply obtained from the difference between C_{net} and C_p. Negative capacitance is observed across a relatively wide frequency range, albeit with varying profiles of frequency dependence, determined by I_C.

Conclusively, in order to design a negative capacitance circuit that generates a constant negative capacitance, it is desirable to minimise the effect of the series negative resistance component. The negative resistance is inversely proportional to the g_m of the transistors therefore, increasing I_C is effective in mitigating the effect of $-R_c$. Nevertheless, such an advantage comes at the expense of increased power consumption. Techniques used in a similar situation may be utilised to offset $-R_c$ such as the placement of a compensating series resistor R_{com} as in [46] or by adding a diode connected as a resistance to the output of a differential cross-coupled NIC as in [59].

3.5.2 Verification of the Effect of R_{com} on the Quality of $-C_c$

Analysis in Section 3.4.1 concluded that $-R_c$ limits the quality at which the negative capacitance circuit can neutralise any given capacitance, which was also verified through measurements in the preceding section. However, it was inferred that the undesirable effect of $-R_c$ can be minimised by increasing I_C. Alternatively, it is possible to offset $-R_c$ by adding a series compensating resistor R_{com} at the circuit input as shown by Figure 3.16a. The addition of R_{com} offset $-R_c$ so that its is given by (3.7). In theory, if $R_{com} = 2/g_m$, then $-R_c$ can be nullified and as such ideal neutralisation of any given capacitance can be achieved as illustrated by simulation of the simplified equivalent model in Figure 3.10. Nevertheless, further simulations in Section 3.4.2 showed that complete neutralisation of $-R_c$ by R_{com} is not attain-

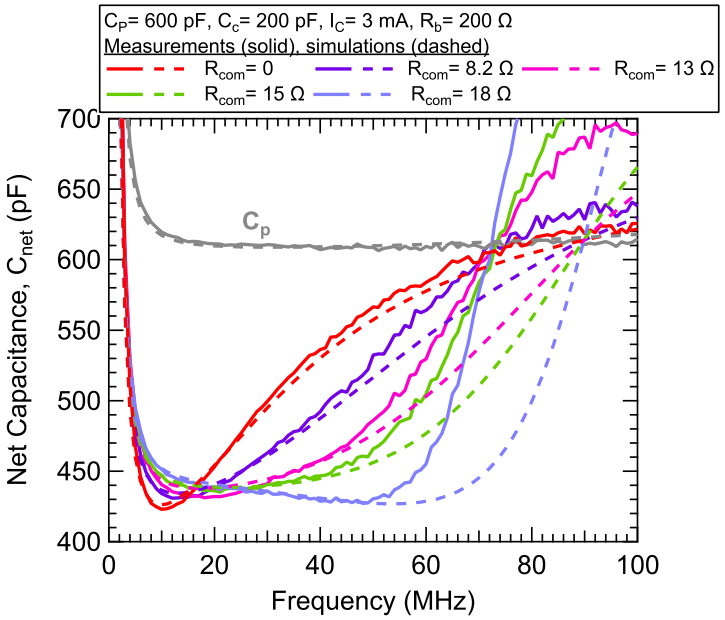


Figure 3.19: Measured and simulated C_{net} and $-C_c$ for $C_p = 600$ pF and $C_c = 200$ pF at $I_C = 3$ mA and varying R_{com}

able even for $R_{com} = 2/g_m$, due to the presence of the bias resistor R_b as shown by the passive equivalent model in Figure 3.11b. Hence, R_b modifies the resistive component given in (3.7) and as such limits the effectiveness of R_{com} in neutralising $-R_c$ and leads to a considerable high frequency scaling of $-C_c$, especially for low values of R_b, which was illustrated in Figure 3.12c and Figure 3.12d.

In this section, the advantage of adding R_{com} is assessed and verified by measuring the circuit at $I_C = 3$ mA (equivalent to $-R_c \approx 16.7\ \Omega$) again for $C_p = 600$ pF, $C_c = 200$ pF and $R_b = 200\ \Omega$. The magnitude of $-R_c$ is reduced by adding $R_{com} = 8.2\ \Omega$, $13\ \Omega$ and $15\ \Omega$ instead of increasing I_C. In theory, these R_{com} values should offset $-R_c$ to the correspondent values if the circuit was operating at $I_C = 6$ mA, 12 mA and 24 mA, respectively. In addition to, the case where $R_{com} = 18\ \Omega$ to approximately match the value of R_{com} to $-R_c$, which was shown to result in ideal neutralisation of C_p based on simulations of the simplified equivalent model (without R_b) as illustrated by Figure 3.10.

Figure 3.19 shows the simulated and measured C_{net} at $I_C = 3$ mA without R_{com} (equals zero) versus C_{net} at $I_C = 3$ mA with the addition of different values of R_{com}. Clearly, the addition of R_{com} improves the quality of neutralising C_p in

comparison to the case when R_{com} is not used. Furthermore, increasing R_{com} leads to more uniform frequency behaviour across the negative capacitance circuit operational bandwidth and as such better amelioration of C_p. Similar trend was observed in Figure 3.18a as a result of increasing I_C. Therefore, it can be concluded that R_{com} is effective in offsetting $-R_c$ and as such improving the quality of the generated $-C_c$ without increasing I_C. Nevertheless, it is clear that for all cases of R_{com}, the measured frequency range at which the negative capacitance is observed falls short by approximately 20 MHz in comparison to results predicted by simulations. This discrepancy between measurements and simulations is conjectured to be caused by additional parasitic inductances from the circuit layout, which can by reduced with better layout.

Using R_{com} for offsetting $-R_c$ to obtain better quality $-C_c$ without increasing I_C is particularly useful in scenarios where reducing power consumption is desirable. Nevertheless, power optimisation is not the main concern of this research work, yet, the focus is to generate high quality $-C_c$ for a broad frequency range, which is crucial for the application of interest that is the bandwidth extension of LEDs. As such, the two approaches of offsetting $-R_c$ either by increasing I_C or through fixing I_C and adding R_{com} are compared to determine which approach renders the best neutralisation of C_p.

Figure 3.20 compares the measured C_{net} obtained at $I_C = 3$ mA for $R_{com} =$ 8.2 Ω, 13 Ω and 15 Ω versus the measured C_{net} obtained at $I_C = 6$ mA, 12 mA and 24 mA without R_{com}. Clearly, the measured C_{net} curves obtained for the increasing I_C cases (dashed curves) exhibits significantly better frequency behaviour in comparison to the correspondent cases where $I_C = 3$ mA and R_{com} (solid curves) is increased. Moreover, it can be observed that using R_{com} to offset $-R_c$ results in reduced level of compensation of C_p, where C_{net} is seen to be approximately 450 pF for all R_{com} cases instead of 400 pF. This is a result of the scaling caused by the relatively low value of R_b, which was illustrated earlier in Figure 3.12c and Figure 3.12d.

Hence, based on the results above, it can be inferred that offsetting $-R_c$ by

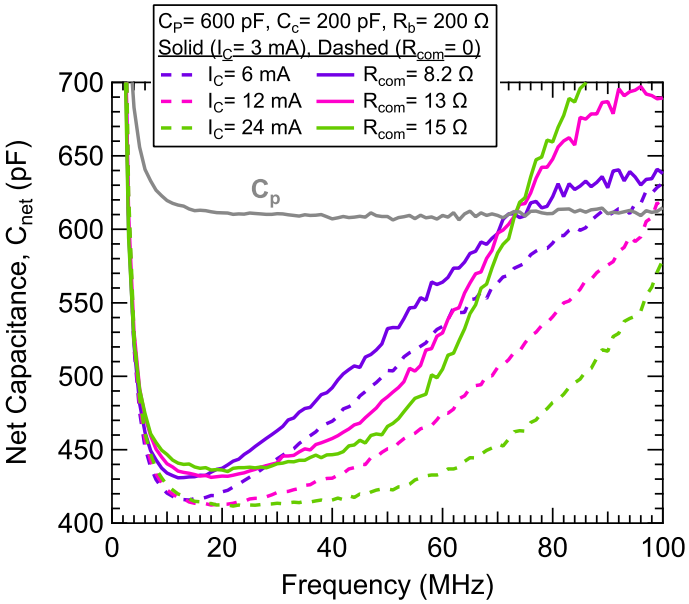


Figure 3.20: Comparison of measured C_{net} at varying I_C versus at fixed $I_C = 3$ mA and varying R_{com}

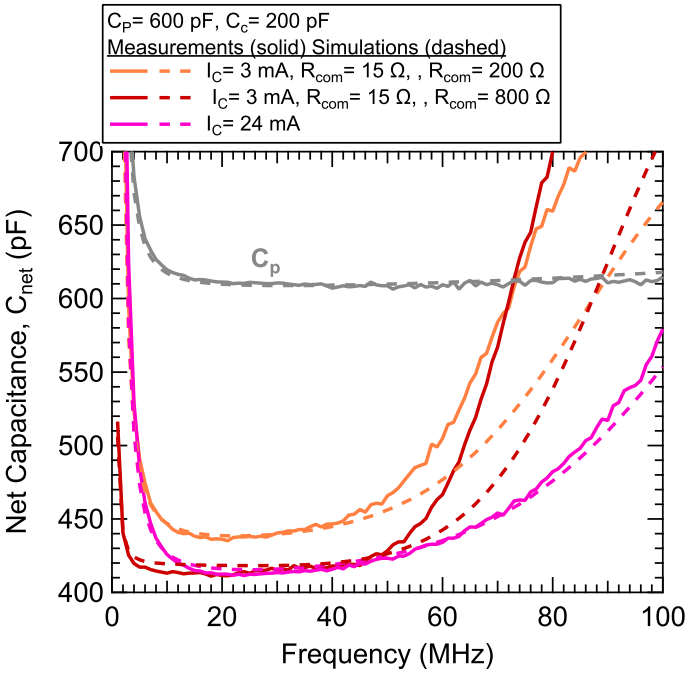


Figure 3.21: Comparison of measured and simulated C_{net} at $I_C = 3$ mA, $R_{com} = 15\ \Omega$ at $R_b = 200$ and $800\ \Omega$ versus for varying $I_C = 24$ mA

increasing I_C results in significantly better neutralisation of C_p in comparison to using the R_{com} approach. Moreover, it is evident that increasing I_C offers better

negative capacitance behaviour in terms of both the neutralisation frequency range and the level of compensation. While, it is possible to optimise the compensation level of C_{net} obtained from the R_{com} approach by employing larger values of R_b. Nevertheless, the increasing I_C would still surpass the latter approach in terms of the neutralisation frequency range.

The effect of employing higher R_b on the compensation level of C_{net} when using the R_{com} to offset $-R_c$ is investigated by measuring C_{net} for two cases. Case 1: $I_C = 3$ mA, $R_{com} = 15\ \Omega$ and $R_b = 200\ \Omega$ and Case 2: $I_C = 3$ mA, $R_{com} = 15\ \Omega$ and $R_b = 800\ \Omega$. These cases are compared to operating at $I_C = 24$ mA and $R_b = 200\ \Omega$ without R_{com}. Figure 3.21 shows the measured and simulated C_{net} for each respective case. Increasing R_{com} from 200 Ω to 800 Ω for the $I_C = 3$ mA and $R_{com} = 15\ \Omega$ eliminates the scaling of $-C_c$ introduced by low values of R_b, which in turn improves the compensation level of C_p. Furthermore, increasing R_b improves the low cut-off-frequency at which the neutralisation of C_p occurs (negative capacitance is observed), yet it does not affect the high cut-off-frequency that is limited to approximately 70 MHz. In contrast, operating at $I_C = 24$ mA yields higher frequency range of neutralisation, up to 100 MHz. Hence, it is evident that increasing I_C to offset $-R_c$ yields better quality $-C_c$ in comparison to using low I_C and adding R_{com}. Hence, operating at high I_C or at best adopting a combination of high I_C and smaller values of R_{com} is a more suitable design approach to generate high quality $-C_c$. While noting that such improvement in $-C_c$ comes at the expense of increased power consumption.

3.5.3 Verification of the Range of $-C_c$

Thus far, most measurements were conducted at a fixed $C_p = 600$ pF and $C_c = 200$ pF, at which design optimisations were concluded based on the measured C_{net} frequency behaviour. Nevertheless, it is also important to assess the extent to which C_p can be neutralised. As previously discussed, a fundamental condition for stability of circuits generating negative capacitance is that C_{net} must remain positive, i.e. $C_p - C_c > 0$. This is to satisfy the basic stability criterion discussed in Section 2.3.1 and expressed inequalities in (2.3) and (2.4), as such ensuring that the network

function does not have any poles in the RHP of the s-plane that could give rise to oscillations. Nevertheless, in practice, the circuit is also sensitive to factors such as the bias networks and distributed effects from the circuit layout, which can potentially reduce the stability margin of the circuit as such, limit the value of generated negative capacitance and, in turn, the extent of neutralising C_p. This compromise between stability and the values of the generated negative elements is commonly encountered in applying NICs in the non-Foster matching of small electrical antennas, where stability usually imposes a limit on the negative image modelling. Hence, limiting the quality of matching and the maximum power transfer within the antenna's operational bandwidth and stability [55].

This section demonstrates the extent to which C_p can be neutralised without compromising the circuit stability by measuring C_{net} for different values of C_c. It is worth noting that stability optimisations are dependent on the nature of the circuit load. For example, in the LED case, which will be discussed in the next chapter, the negative capacitance circuit will see the LED impedance at its input. Hence, in such a case, the stability optimisation and analysis of the circuit will have to account for such load instead of just a capacitor. The nature of the load that the circuit sees is dependent on the application at which the circuit is integrated, and in turn, an independent stability analysis has to be conducted for each application. Nevertheless, measuring the range of negative capacitances the circuit presents without compromising stability, will still give a reflection of its robustness and versatility.

Figure 3.22 illustrates C_{net} at $I_C = 24$ mA for $C_p = 600$ pF and C_c is varied in steps of 100 pF from 100 pF to 500 pF. By looking at all cases of C_c, it is clear that there is a reduction in C_p, yet with different levels of neutralisation and frequency dependency. Low values of C_c, like $C_c = 100$ pF, yields an almost frequency independent reduction in C_p. As such C_{net} is seen to be relatively flat for the given range of frequencies. As C_c is increased to 200 pF, C_{net} starts to show deviation from its corresponding value at higher frequencies. Such deviation of C_{net} from its corresponding value is seen to aggravate as C_c is increased further ($C_c = 300$ pF to 500 pF), leading to a reduction in the range of the negative capacitance circuit

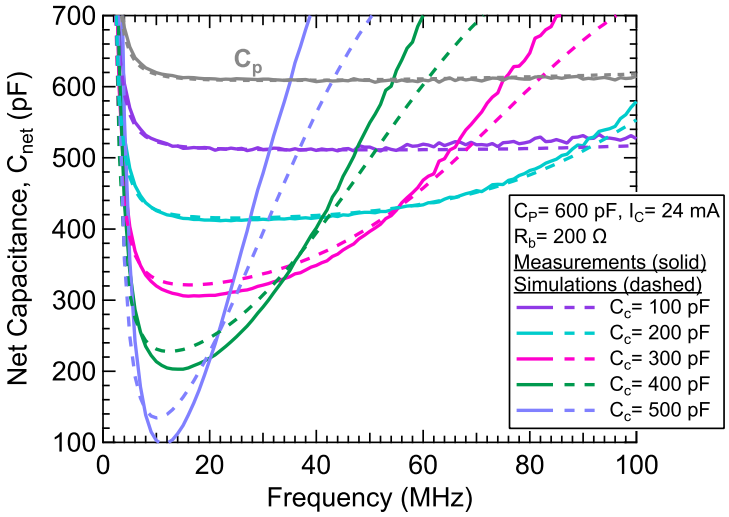


Figure 3.22: Measured and simulated C_{net} at $I_C = 24$ mA for varying C_c

validity. In other words, for higher C_c, the range of frequencies of the negative capacitance is reduced, in addition to becoming more frequency-dependent. Such behaviour results from the presence of the $-R_c$ component, which has a more significant effect for higher values of C_c. Hence, degrading the quality of neutralising C_p across frequency for higher C_c. Notwithstanding, such frequency-dependent behaviour, yet even for $C_c = 500$ pF, a reduction in C_p is observed for a frequency range of approximately 30 MHz without compromising the circuit stability.

3.6 Conclusions

This chapter describes the full design and verification of a negative capacitance circuit based on circuit reported in [46]. The chapter included new mathematical derivations of the input impedance of the negative capacitance circuit based on nodal analysis of the simplified equivalent model assuming ideal transistors. The model was then extended to a semi-empirical model, which includes the intrinsic parasitic elements of the transistors to improve the prediction of the range of generated negative capacitance of the proposed circuit. The circuit equivalent models predicted that the impedance of the proposed circuit can be approximated by a combination of a negative capacitance $-C_c$ in series with a negative resistance $-R_c$. The negative resistance component was found to be a function of the transistors g_m. It was also found that $-R_c$ degrades the efficacy of the negative capacitance circuit in neutralising a given capacitance. However, this undesirable effect can be minimised by increasing g_m through increasing I_C, which significantly improves the frequency behaviour of the generated negative capacitance. Alternatively, a series compensation resistor R_{com} can be placed at the circuit input to offset the $-R_c$ component. Altogether, based on the modelling and simulation studies of the negative capacitance circuit, it can be concluded that in order to generate a wide-band stable negative capacitance successfully, the following design optimisations have to be taken:

- Minimise the negative resistance component $-R_c$ by increasing the transistor bias currents I_C or by adding a series compensating resistor R_{com} at the input. This reduces the frequency dependence of the generated negative capacitance within the circuit operational frequencies.

- Maximise the bias resistor R_b either by opting for high value or by using a current mirror. The value of R_b sets the lower cut-off-frequency of the generated negative capacitance; hence, using large R_b allows for low cut-off-frequency.

- Opt for high f_T transistors with small intrinsic capacitances, since high tran-

sistor intrinsic capacitances lead to increased frequency dependence of the generated negative capacitance.

- Careful layout design, in particular, it is important to minimise the lengths of transmission lines within the circuit feedback loop to avoid compromising the circuit stability. Moreover, minimise the lengths of the input feedline, since it adds undesirable inductance that degrades the quality of the generated negative capacitance seen at the input.

Following the considerations above, the negative capacitance was constructed using discrete components on a PCB. The performance was verified by measuring the scattering parameters of the constructed circuit. Measurements showed that a stable high quality negative capacitance can be achieved, which suggests it is a good candidate for equalising the bandwidth-limiting junction capacitance associated with LEDs for high capacity visible light communication systems.

Chapter 4

Negative Capacitance for LED Bandwidth Extension

4.1 Introduction

This chapter presents the design and verification of a new LED bandwidth extension technique based on introducing a parallel negative capacitance to offset the bandwidth-limiting LED junction capacitance, hence extending its operating bandwidth. The negative capacitance is achieved by exploiting the specially designed circuit of Chapter 3. In addition, the chapter includes the design principles and optimisations to achieve optimal bandwidth extension of the LED based on derivations of the impedance characteristics of the passive equivalent circuit model of both the LED and the negative capacitance. The performance of the proposed bandwidth extension technique is evaluated by measuring the scattering parameters of a circuit constructed using discrete components on a PCB. Experimental demonstration of a VLC system, with commercially available blue and red LEDs, was set up and tested with and without the negative capacitance compensation. Test results demonstrate a remarkable bandwidth extension of up to 500%, with no power loss and minimal signal distortion. The analytical and circuit design techniques proposed here would be applicable in areas beyond VLC and may have utility in other optical systems operating at much higher data rates and with different types of LEDs. Work presented in this chapter includes results presented in a journal article[1].

[1] A. Kassem and I. Darwazeh, "Use of Negative Impedance Converters for Bandwidth Extension of Optical Transmitters," in IEEE Open Journal of Circuits and Systems, vol. 2, pp. 101-112, 2021

4.2 A Brief Review of LED Modelling

Establishing a simple and reasonably accurate LED model is fundamental for designing the LED bandwidth extension proposed in this research work. Moreover, it is generally important to design efficient drivers and equalisers to extend the LED modulation bandwidth. This section describes some of the basis of the operation of the LED as a pn junction, which aids in describing a basic LED model and a high frequency LED model.

An LED is a pn junction and therefore has a depletion region with width W_D given by: [98]

$$W_D = \sqrt{\frac{2\varepsilon_r\varepsilon_o(N_A^+ + N_D^-)(V_D - V_B)}{qN_A^+N_D^-}} \tag{4.1}$$

where ε_r is the dielectric constant of the material, ε_o is the relative permittivity of vacuum, N_A^+ and N_D^- is the concentration of acceptor and donor atoms, respectively, V_D is the diffusion voltage, and V_B is the diode bias voltage. Taking the charge carrier parameters as constant at any instantaneous time, W_D is determined by the difference between V_D and V_B. An external bias voltage, therefore, decreases or increases W_D for forward or reverse bias, respectively. Applying positive V_B (forward bias) leads to a reduction in W_D, and as such, it becomes easier for charge carriers to diffuse, which is a desirable condition for LEDs. In contrast, if V_B is negative (reverse bias), W_D increases and as such, charge carriers require more energy to cross the semiconductor, which is a desirable condition for photodiodes.

The relationship between the applied bias voltage and forward current in a pn junction was first defined by Shockley and expressed by:

$$I_f = I_s exp[\frac{qV_B}{KT} - 1] \tag{4.2}$$

where I_s is the reverse saturation current, q is the electron charge, K is the Boltzmann constant, and T is the temperature measured in Kelvin. The slope of the I-V curve at a given current defines the diode dynamic resistance r_d and conductance

g_m as given by:

$$g_m = \frac{1}{r_d} = \frac{dI_f}{dV_B} \tag{4.3}$$

The depletion region has an associated capacitance, which relates to its width as expressed by:

$$C_{dep} = \sqrt{\frac{\varepsilon_r \varepsilon_o q N_A^+ N_D^-}{2(N_A^+ + N_D^-)(V_{bi} - V_B)}} = \frac{\varepsilon_r \varepsilon_o}{W_D} \tag{4.4}$$

which by inspection is similar to the expression for parallel plate capacitance, thus by introducing a term for the cross sectional area A_D (m^2), the depletion capacitance becomes:

$$C_{dep} = \frac{\varepsilon_r \varepsilon_o A_D}{W_D} \tag{4.5}$$

It is also important to account for capacitance as a result of the transport of the charge carriers known as the diffusion capacitance C_d, which is given as a function of the capacitor charge Q by:

$$C_d = \frac{dQ}{dV} \tag{4.6}$$

Hence, the total LED junction capacitance C_j is given by:

$$C_j = C_{dep} + C_d \tag{4.7}$$

Based on the relations defining a pn junction behaviour, it can be inferred that LEDs have a low pass transfer function, which can be simply emulated by an equivalent first-order low pass RC filter impedance model with a cut-off-frequency dictated by the product of the junction capacitance C_j and the dynamic resistance r_d.

One-port reflection measurement, based on the return loss (S_{11}), is a commonly used approach to characterise the impedance model of devices such as lasers and LEDs [99, 100]. Cheung *et al.* (1999) describes the modelling and extraction procedure of the small-signal LED parameters based on impedance measurements [99]. The LED model was found to be equivalent to resistance in series with a parallel RC as illustrated by Figure 4.1a. Furthermore, the LED equivalent model was con-

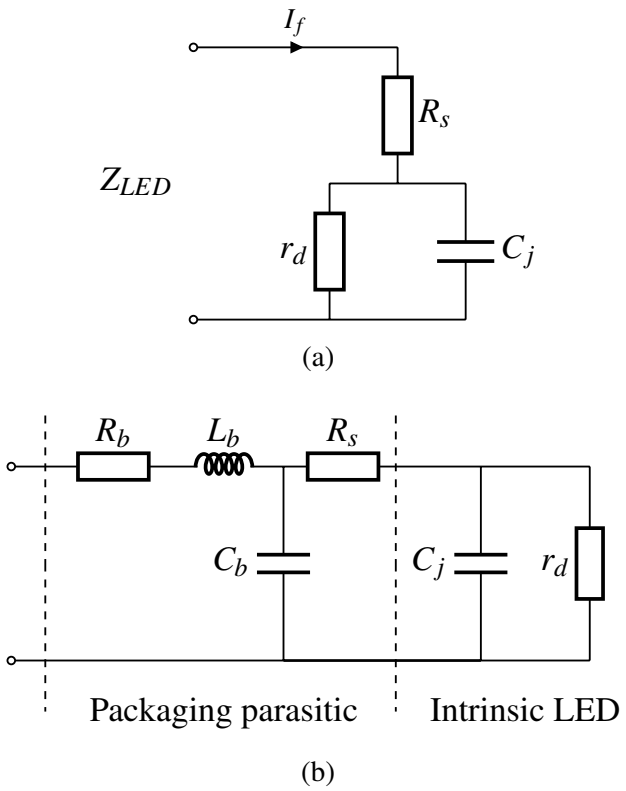


Figure 4.1: (a) Low frequency LED passive equivalent model reported in [99, 100] (b) High frequency LED equivalent model reported in [101]

firmed to be valid by the close agreement between the model and measurements of the LED impedance.

Figure 4.1a illustrates a basic LED equivalent circuit model. The LED model consists of the junction capacitance C_j, the small signal dynamic resistance r_d and the ohmic contact resistance R_s. By analysing the circuit in Figure 4.1a the LED impedance is given by:

$$Z_{LED} = R_s + \frac{r_d}{1 + j\omega r_d C_j} \tag{4.8}$$

The LED modulation bandwidth at a fixed forward current I_f is approximated by an RC time constant as given:

$$f_{3dB} = \frac{1}{2\pi f r_d C_j} \tag{4.9}$$

These equations together with the carrier lifetime of the LED form the ultimate limit on the modulation bandwidth of LEDs used in VLC. The carrier lifetime is associated with the average time for a minority carrier to recombine, which is dic-

tated by the physical properties of the material, like for example, the doping level, such that increased doping could shorten the carrier lifetime and therefore, increase the LED modulation bandwidth [98]. In [101, 102], a high frequency model for a high-power LED is derived, based on measurements of the S_{11} and S_{21} of several colour LEDs. The model considers both intrinsic LED limitations such as the carrier lifetime and junction capacitance C_j and other limiting parasitic inductance and resistance arising from the LED packaging as shown by Figure 4.1b. This model is highly accurate at high frequencies, where it shows that the LED additional packaging elements result in high-frequency resonance. Nevertheless, for low frequencies, it shows that the LED follows a first-order low pass filter. As such, the effect of the model's additional parasitic elements is significant at frequencies far above the LED cut-off-frequency. Therefore, based on these findings, this work elects to design the proposed LED bandwidth extension technique based on the basic LED model shown in Figure 4.1a, since it is generally sufficient to predict the LED bandwidth. Moreover, it simplifies the mathematical analysis of the LED impedance when connected to the negative capacitance circuit of Chapter 3 as will be presented in Section 4.4.

4.3 LED Bandwidth Extension Techniques

As previously explained, one of the key limitations in achieving high data rates in VLC is the low modulation bandwidth of LEDs. The bandwidth of off-the-shelf single colour LED is limited to a few MHz [13, 98, 101, 103]. Whereas, white LEDs based on blue LEDs coated with colour converting phosphorous have even lower bandwidth due to the slow response of the phosphorous. Typically, blue filtering is employed at the receiver to undo the effect of the slow yellow component and extract the fast blue response [26, 27], which can significantly extend the LED bandwidth, yet as previously discussed this can result in a considerable loss in the received signal power. Studies by Sung *et al.* (2014) debated the benefits of using blue filtering to enhance the transmission speeds in VLC by comparing two VLC links employing blue filtering and different modulations; namely on off keying (OOK) and DMT. Sung showed that when using DMT VLC, the use of blue filtering is unnecessary and may also degrade the transmission speeds due to the associated reduction in SNR, which often offsets its bandwidth extension advantage [104].

Apart from the phosphorous limitation, the main factors restricting the LED bandwidth are the carrier lifetime and the RC time constant associated with r_d and C_j as expressed by (4.9); such factors impose an overall limitation on the communication systems bandwidth. To overcome such limitations and improve the achievable transmission speeds in VLC, multi-level [105] and multi-carrier [4] modulation formats have become prevalent due to their higher spectral efficiency, which is useful in maximising the number of bits/symbol. Alternatively, variations of bandwidth expansion circuits were proposed to mitigate the bandwidth-limiting capacitive behaviour of LEDs.

There has been a number of proposals of circuit design techniques to enhance the LED bandwidth including: (i) analogue passive pre-equalisers based on multi-resonant circuits [15] and T-bridge equalisers [16–19] (ii) analogue passive post-equalisers [27] (iii) artificial pseudo transmission lines [20] (iv) pre-emphasis circuits [44, 106], (v) carrier sweep out circuits [107–109]. Techniques in (i)-(iii) aim to reduce the capacitive behaviour of LEDs by using high pass filters. While these

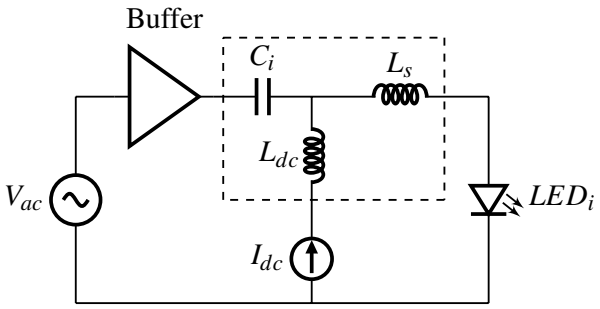


Figure 4.2: Multi-resonance circuit diagram, including bias-T and LED proposed in [15]

techniques have been demonstrated to enhance transmission speeds, they often incur a significant loss of signal power. On the other hand, techniques proposed in (iv) and (v) presents efficient circuit techniques that enhance the bandwidths of LEDs without compromising their signal power.

Other circuits are based on LED drivers utilising high-speed NAND gates with open collector were proposed to enhance the LED bandwidth, yet this approach is limited to pulse-based modulation schemes due to the on-off nature of the digital logic used to impress the data on the DC current [30]. Depending on the application, the LED driver can be designed for high power devices as in [109], which is based on traditional push-pull drivers with an additional carrier sweep out stage, driving a 10 W LED. On the other hand, other applications require drivers with dimming capabilities, which often adopt pulse width modulation with the relevant circuits as in [110, 111].

A commonly used approach to improving VLC transmission speeds is based on using analogue resonant circuit technique to equalise the low frequency behaviour of LEDs. Figure 4.2 illustrates one of the early examples of analogue passive pre-equalisers reported in [15]. A multi-resonant equaliser is based on a bias-T with a series inductance placed before the LED. A total of eight resonant circuits were designed to create different resonant frequencies, which, when aggregated, would extend the LED bandwidth. Nevertheless, such bandwidth extension is at the expense of optical power loss due to the resistive elements. Moreover, the use of numerous capacitors may cause attenuation of the low frequency component of the

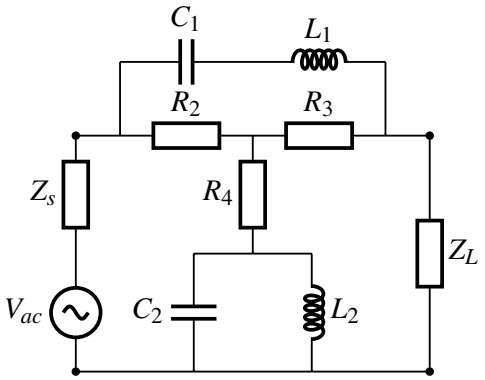


Figure 4.3: Symmetrical bridged-T amplitude equaliser reported in [19]

signal, which is known as baseline wander (BLW) phenomena; this is particularly problematic for base-band modulation, whereas a significant amount of power at the DC and low frequency components.

More sophisticated passive equalisers in the form of T-bridge networks, configured as single-stage [16, 19] and cascaded [17, 18], were demonstrated to extend the LED bandwidth by over an order of magnitude also at the expense of substantial loss in signal power. In comparison to simpler forms of passive equalisers in [15, 27], RC-based T-bridge passive equalisers exhibit constant characteristic impedance and stable high-frequency response, especially when the signal is several hundred megahertz. Figure 4.3 illustrates an example of a T-bridge equaliser reported in [19]. The pre-equaliser is designed to have high low frequency attenuation, and the attenuation decreases as the frequency increases, which is opposite to the frequency response of the LED. The level of low frequency attenuation is dictated by R_3 and the slope of the frequency response by C_1 and L_1. Low values of C_1 and L_1 means higher frequency range of equalisation yet at the expense of a higher level of attenuation of the output signal. Hence, despite the significant bandwidth extension achieved in reports employing this type of equalisers as in [19], where the LED bandwidth is extended from 45 MHz to 700 MHz, the loss in the signal power is over 25 dB. Whereas, in [17], the LED bandwidth is extended from 27 MHz to 376 MHz, yet with approximately 15 dB loss in signal power. Hence, the design of such equalisers often dictates a compromise between the bandwidth and the SNR level. Moreover, the design procedure of such equalisers is often based on a trial and error basis.

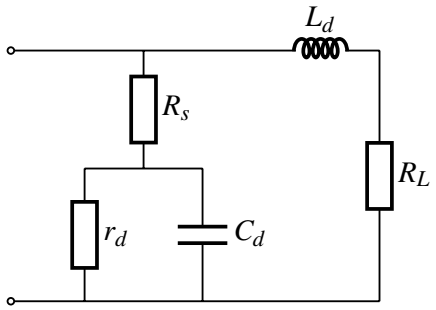


Figure 4.4: LED equivalent circuit with C_d incorporated into ATL reported in [20]

Another form of passive equalisation is reported in [20], which is inspired by techniques employed in the design of distributed amplifiers. In this work, the equaliser aims to incorporate the LED bandwidth-limiting diffusion capacitance into a pseudo-artificial transmission line that presents an inductive like behaviour as illustrated in Figure 4.4. As such, it can yield a significant bandwidth extension of approximately 400% at the expense of 60% loss in the LED impedance magnitude, resulting in a significant reduction of the optical signal power.

A common theme from the review of LED bandwidth extension circuits reports is the extensive use of passive equalisation and blue filtering. While such techniques have effectively demonstrated high data rates in VLC links by extending the transmitter bandwidth, their benefits will always be limited as they incur a significant loss in optical power. Hence, limiting the LED output light intensity and possibly the overall system capacity due to the reduction in SNR at the receiver. A recent study in [112] questions the benefits of analogue equalisers by comparing the system performance employing passive equalisers with the raw system without any SNR penalties. It shows that the unequalised VLC system with the multi-carrier modulation and bit-loading can achieve higher data rates than the equalised system because of the absence of SNR penalties and higher spectrum efficiency.

Another approach to extend the modulation bandwidth of LEDs is by employing efficient electronic circuits that treat the inherent limitations of the LEDs, without trading the optical signal power. In [44], a traditional active pre-emphasis technique is demonstrated using current mode logic (CML) and a common collector driver stage with a pre-emphasis circuit that extends the bandwidth by tenfolds. A

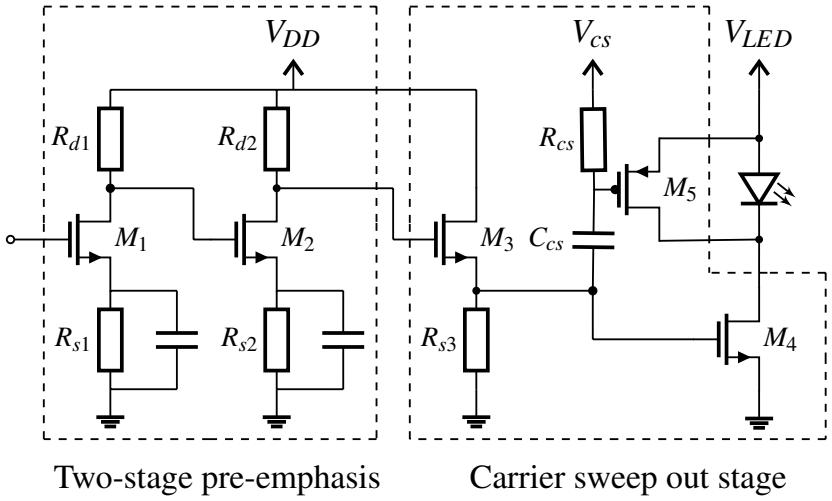


Figure 4.5: LED driver employing both pre-emphasis and carrier sweep out circuit

CML stage is a typical configuration for high-speed modulation that is often used to drive lasers. Nevertheless, in the case of the LED there is an additional requirement to drive the LED at a high current. Large switching current might degrade the high speed response of the CML stage, hence to avoid such degradation, the CML is followed by a common collector stage, where the LED in series with a parallel RC network act as the load for the common collector stage. Such arrangement allows for simple control of the LED current and the tuning of the RC network to improve the frequency response. Whereas, work in [107] is based on a CS stage and another carrier sweep out stage, which provides a drawing out path of remaining carriers in the depletion region, when the LED is off and thereby reduce the pulse fall time. The driver is fabricated using a 0.18μm CMOS process, where experimental results showed up to 88% increase in the achievable bit rate of a gallium nitride GaN-based LED. Whereas, work in [108] combines the use of techniques that incur optical power loss and lossless techniques by adopting a blue filer to extend the bandwidth of white LED from 3 MHz to 10 MHz with approximately 7 dB loss in power. Then, a 0.18μm CMOS LED driver combining both the pre-emphasis and carrier sweep, shown in Figure 4.5, was used to enhance the bandwidth of the filtered blue component of the LED to 80 MHz with no loss in optical power.

The LED bandwidth extension technique proposed in this work is fundamentally different from the techniques in [44, 107, 108], as it achieves bandwidth exten-

sion by synthesising a negative capacitance, which offsets the bandwidth-limiting effect of the LED junction capacitance. Hence, it can be tailored to the specific LED characteristics, as described in the following section.

4.4 Proposed LED Bandwidth Extension Technique

The proposed LED bandwidth extension technique is based on the utilisation of the negative capacitance circuit of Chapter 3 to generate negative capacitance in parallel to the LED junction capacitance. Hence, offsetting its bandwidth-limiting effect from determining the LED bandwidth. This section describes the design methodology followed to develop and verify the proposed LED bandwidth extension technique through extensive mathematical derivations, simulations of the passive equivalent circuit models and experimental verification. All the design and measurements included in this section are based on the passive equivalent circuit models of both the LED and the negative capacitance circuit, which serves to understand the design optimisation necessary to achieve optimal performance. Optical measurements based on the application of the proposed technique to commercially available LEDs are presented in the next section.

4.4.1 Design Methodology

The application of the negative capacitance circuit to extend the LED bandwidth is investigated based on the LED impedance characteristics. First, the LED impedance characteristics are examined by analysing the passive equivalent circuit models, both for the uncompensated LED and when compensated by connecting it to the negative capacitance circuit. From this, mathematical derivations of the compensated LED impedance behaviour (LED+NC) are obtained to understand the nature of the pole(s) dictating its bandwidth. Hence, optimise the design of the negative capacitance circuit according to the LED behaviour.

It is worth noting that the LED impedance characteristics are particularly relevant to this study, as when driven by a current source, the LED impedance exhibits similar frequency behaviour to the LED current and by extension to the LED optical power, as shown in [20, 95]. In this study, a simplified LED model is used as in Figure 4.1a. Such a simplified model is sufficient for a first-order approximation of the diode model and a reasonably accurate design of the negative capacitance circuit. The simulations of the LED passive equivalent circuit model are initially based on verified LED model parameters ($r_d = 15\ \Omega$ and $R_s = 1.8\ \Omega$ and $C_j =$

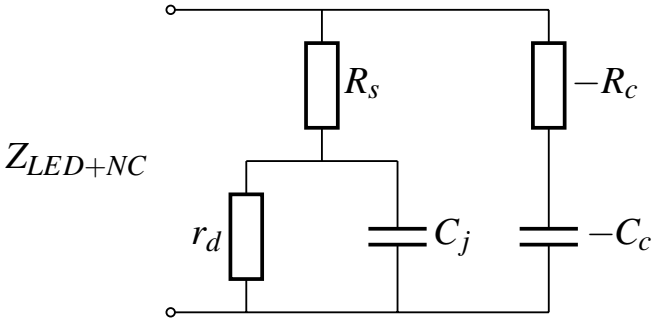


Figure 4.6: LED and NC simplified equivalent model

600 pF) reported in [99], which is based on a relatively high-speed Hamamatsu LED. The extracted LED model parameters were used only as an example to illustrate the behaviour of the LED with the negative capacitance circuit in simulations. Then, for verification purposes through measurements of the scattering parameters of the negative capacitance circuit PCB with the LED passive equivalent circuit model. However, in doing the experimental optical testing, this specific LED (manufactured by Hamamatsu) could not be obtained for further optical measurements, for which other LEDs were used.

4.4.2 Derivation of Compensated LED Equivalent Model

Figure 4.6 illustrates the simplified LED passive equivalent circuit model when connected to the negative capacitance. The LED bandwidth can be potentially extended by ameliorating the bandwidth-limiting effect of C_j through introducing a parallel negative capacitance $-C_c$, thereby reducing the net capacitance dictating the bandwidth so the LED bandwidth becomes:

$$f_{3dB} = \frac{1}{2\pi r_d (C_j - C_c)} \tag{4.10}$$

Ideally, the bandwidth can be infinitely increased if $|C_c| = C_j$. Nevertheless, as shown by (3.5), it is not possible to realise pure negative capacitance since the impedance given by the negative capacitance circuit consists of $-C_c$ in series with $-R_c$. Hence, analysing the LED impedance when connected to the negative impedance ($-C_c$ in series with $-R_c$) in Figure 4.6 yields the impedance given by:

$$Z_{LED+NC} = \frac{(R_s + r_d + sr_d R_s C_j)(1 + sR_c C_c)}{(r_d C_j C_c (R_c - R_s))s^2 + (r_d (C_j - C_c) + C_c (R_c - R_s))s + 1} \tag{4.11}$$

Clearly, the LED resistance at DC remains $R_s + r_d$. The LED impedance function has two real zeros given by (4.12) and (4.13) and two poles that can be either real or complex conjugates $p_{1,2}$.

$$Z_1 = \frac{R_s + r_d}{r_d R_s C_j} \tag{4.12}$$

$$Z_2 = \frac{1}{R_c C_c} \tag{4.13}$$

For the special case were $R_s = |R_c|$, then the second order frequency term becomes zero, the transfer function has just one real pole given by (4.10). However, when $R_s \neq |R_c|$, then the transfer function has a complex pole $p_{1,2}$ given by:

$$p_{1,2} = -\frac{\pi f_n}{Q} \pm j2\pi f_n \sqrt{(1 - Q^2)} \tag{4.14}$$

Where f_n and Q are the natural frequency and quality factor of $p_{1,2}$, respectively as expressed by:

$$f_n = \frac{1}{2\pi \sqrt{r_d C_j C_c (R_c - R_s)}} \tag{4.15}$$

$$Q = \frac{\sqrt{r_d C_j C_c (R_c - R_s)}}{r_d (C_j - C_c) + C_c (R_c - R_s)} \tag{4.16}$$

Hence, based on the analysis above, three main conclusions can be made: (i) When connected to the negative capacitance circuit, the LED bandwidth is no longer solely dictated by C_j and r_d. For the special case when the negative capacitance circuit is designed so that the magnitude of $-R_c$ in (3.6) is equal to R_s then, the LED bandwidth is set by the real pole expressed in (4.10). In practice, complete neutralisation of C_j (predicted in (4.10)) is not achievable, as it would compromise the stability of the negative capacitance circuit as analysed in [51, 55]. On the other

hand, in cases where $R_s \neq |R_c|$, as the value of $-C_c$ becomes more negative, the frequency of $p_{1,2}$ increases; thus, the circuit bandwidth is extended. (ii) Of the two zero frequencies Z_1 and Z_2 expressed in (4.12) and (4.13), respectively, only Z_2 is a function of the negative impedance ($-R_c$ and $-C_c$). Finally, (iii) the LED DC resistance is not reduced when connected to the negative capacitance circuit, which means there is no resistive loading. Hence, there will be no LED output power loss. However, this is dependent on the exact design of the negative capacitance circuit. In the case of the circuit in Figure 3.1, there will be additional loading due to the bias resistor R_b. However, if $R_b >> R_s + r_d$, such loading may be neglected. Therefore, the proposed LED extension technique does not impose the bandwidth-power trade-off seen in other commonly used compensation techniques in [15, 16, 19, 20].

Simulation Studies of the Compensated LED Passive Equivalent Circuit Model

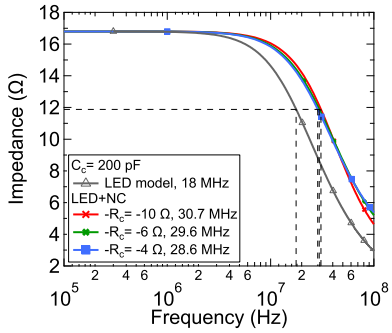
To illustrate the above analysis, the impedance frequency responses of both the compensated LED passive equivalent model (Figure 4.6) and the uncompensated (raw) LED equivalent model (Figure 4.1a) are simulated under different operating conditions. Simultaneously, the pole-zero action of each impedance response is examined to gain insight into the nature of the pole(s) dictating the LED bandwidth. Such analysis aids in choosing the values of C_c and $-R_c$ for optimal performance. As previously mentioned, the parameter values for the LED equivalent model is based on a verified equivalent model reported in [99] with characteristic values derived at 2 mA drive current being $C_j \approx 600$ pF, $r_d \approx 15\ \Omega$ and $R_s \approx 1.8\ \Omega$, which would present a bandwidth of 18 MHz, as given by the real pole dictating the LED bandwidth in (4.9) and one real zero Z_1 as in (4.12).

Figures 4.7a-4.7d show the impedance responses of the raw LED model versus the compensated LED model for given values of $-C_c$ and for three different transistor biases of 6, 12 and 24 mA, resulting in simulated $-R_c$ values of $-10\ \Omega$, $-6\ \Omega$ and $-4\ \Omega$, respectively. Whereas, Figures 4.8a-4.8d shows the corresponding pole-zero action for each of the impedance responses, respectively. The system poles are denoted by the cross symbol and the zeros by the solid circle symbol.

From Figure 4.7a, when $C_c = 200$ pF and $-R_c = -10\ \Omega$, the overall net capacitance is reduced, which results in improvement in the cut-off-frequency of approximately 67%. Whereas, increasing the value of $-R_c = -10\ \Omega$ to $-6\ \Omega$ and $-4\ \Omega$, results in only slight bandwidth reduction. This is evident from the corresponding pole-zero action shown in Figure 4.8a, the compensated response for $C_c = -200$ pF and $-R_c = -10\ \Omega$ results in a complex pole $p_{1,2}$ and an additional real zero Z_2 as in (4.13). Whereas, in cases where $-R_c = -6\ \Omega$ and $-4\ \Omega$, the system has two real poles and the location of the dominant low frequency pole determining the bandwidth is around 30 MHz for both cases overlaps, which explains the almost identical frequency responses.

In Figure 4.7b, C_c is increased to -300 pF which, results in further extension in bandwidth. Moreover, the effect of varying the values of $-R_c$ becomes notable. This can be explained by inspecting the corresponding pole action in Figure 4.8b for each of the $-R_c$ values. In cases where $-R_c$ equals $-10\ \Omega$ and $-6\ \Omega$, the system has a complex conjugate pole. Increasing the value of $-R_c$ shifts the complex poles to higher frequencies and away from the imaginary axis (as indicated by the arrow). Moreover, the increase in the LED bandwidth is demonstrated via the increase in the distance between each of the complex poles from the real axis, which is equivalent to the value of the damped natural frequency. Therefore, it is clear that when R_c is increased from $-10\ \Omega$ to $-6\ \Omega$, it increases the distance between each of the complex poles from the real axis, leading to the observed bandwidth enhancement. In Figures 4.7c and 4.7d, C_c is further increased to 400 pF and 500 pF, respectively where it is clear that increasing of $-R_c$ leads to significant bandwidth extension accompanied by enhanced peaking. The reason for this peak is that the value of the complex pole quality factor Q in (4.16) is a function of both C_c and R_c.

Conclusively, adding an appropriately chosen C_c results in significant bandwidth extension. Moreover, $-R_c$ can be designed to obtain further bandwidth extension, which gives the designer an additional degree of freedom by enabling a bespoke negative capacitance circuit design based on the LED model to obtain maximum bandwidth performance.



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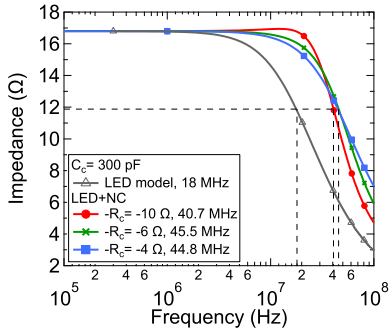

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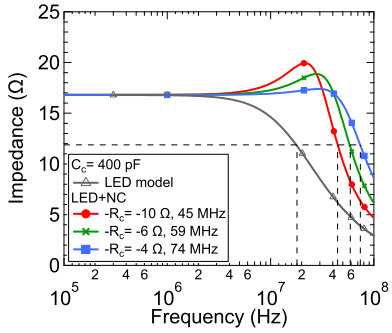

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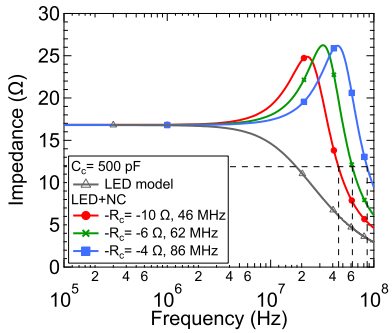
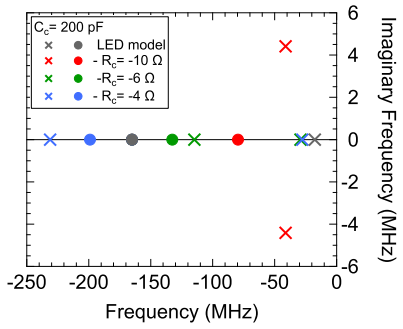


(d)

Figure 4.7: Impedance of the LED+NC model at variable $-R_c$ for C_c (a) 200 pF (b) 300 pF (c) 400 pF (d) 500 pF



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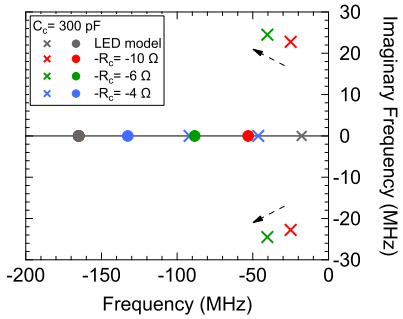

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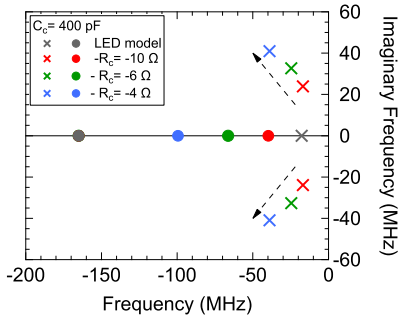

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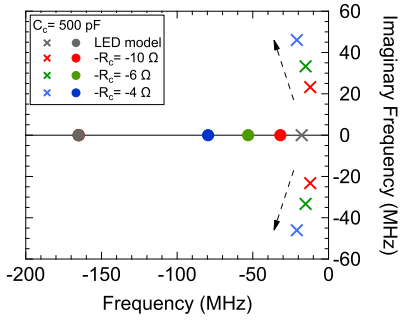


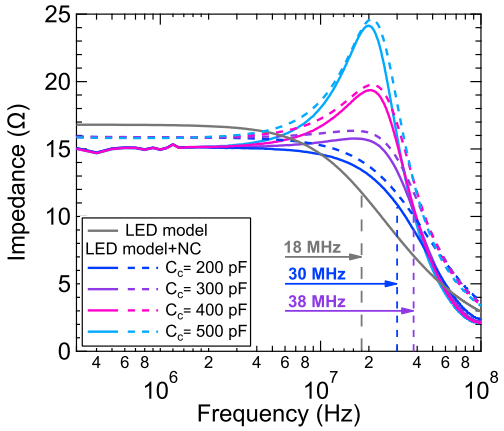
(d)

Figure 4.8: pole-zero action of LED+NC model at variable $-R_c$ for C_c (a) 200 pF (b) 300 pF (c) 400 pF (d) 500 pF

4.4.3 Negative Capacitance Circuit Measurements

This section demonstrates the effect of compensating for the bandwidth-limiting LED junction capacitance by utilising the proposed negative capacitance circuit of Chapter 3 to generate parallel negative capacitance. For consistency and fair comparison, the measurements of the LED is based on the verified equivalent model in [99], previously used in simulations of the compensated LED passive equivalent model in Section 4.4.2. The performance of the circuit is evaluated through measurements of the scattering parameters of the negative capacitance transistor circuit constructed on an FR4 PCB. The PCB is populated using the silicon NPN transistors BFR93 ($f_T = 6$ GHz) and SMD including all resistors and capacitors. Furthermore, the effectiveness of increasing C_c in extending the cut-off-frequency of the LED passive equivalent circuit model and the influence of the $-R_c$ is investigated by varying the bias current I_C of the negative capacitance circuit.

Figures 4.9a, 4.9b and 4.9c compares the compensated LED impedance response in four cases where I_C is a given value and C_c is varied in steps of 100 pF in the range of 200 pF to 500 pF. It can be seen that for all Figures, measurements closely agree with the simulation of the transistor circuit. Moreover, the fabricated circuit exhibits similar behaviour to simulations of the compensated passive equivalent model simulation in Section 4.4.2, which signifies that also the LED and negative capacitance circuit modelling were simplified yet, is accurate enough to predict the compensated LED behaviour. In Figure 4.9a, where $I_C = 6$ mA ($-R_c = -10\ \Omega$), results in significant increase in bandwidth for C_c equals 200 pF and 300 pF of up to 200% compared to the raw LED bandwidth. Whereas, in cases, $C_c = 400$ pF and 500 pF does not affect the bandwidth yet, results in enhanced peaking amplitude. In Figure 4.9b, $I_C = 12$ mA ($-R_c = -6\ \Omega$), similar behaviour is observed, where progressively increasing C_c leads to significant bandwidth extension, yet for cases $C_c =$ 400 pF and 500 pF results in significant peaking amplitude. In Figure 4.9c, $I_C =$ 24 mA ($-R_c = -4\ \Omega$) follows the same trend, achieving remarkable bandwidth extension of up to 300% relative to the raw LED bandwidth, yet again for case $C_c =$ 500 pF, excessive peaking amplitude is observed. The reason for this consistent



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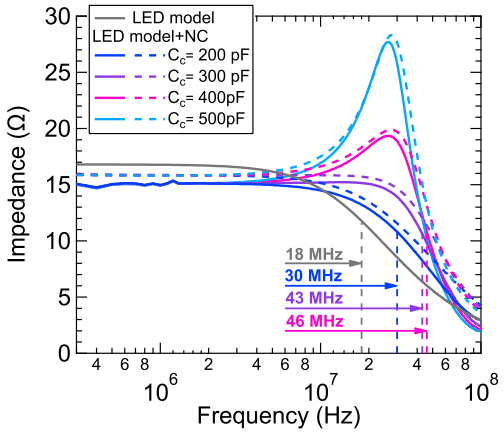

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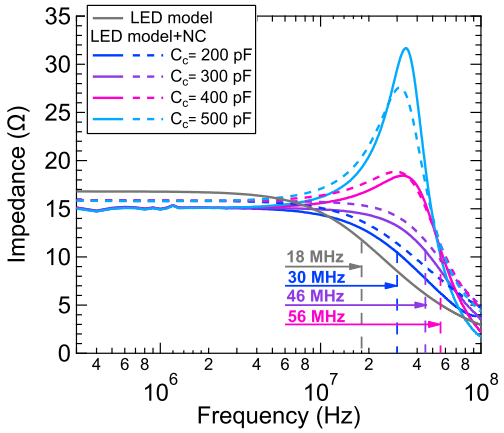


(c)

Figure 4.9: Measured (solid) and simulated (dashed) impedance of the LED equivalent circuit model when connected to the negative capacitance circuit for different values of C_c under (a) $I_C = 6$ mA (b) $I_C = 12$ mA (c) $I_C = 24$ mA

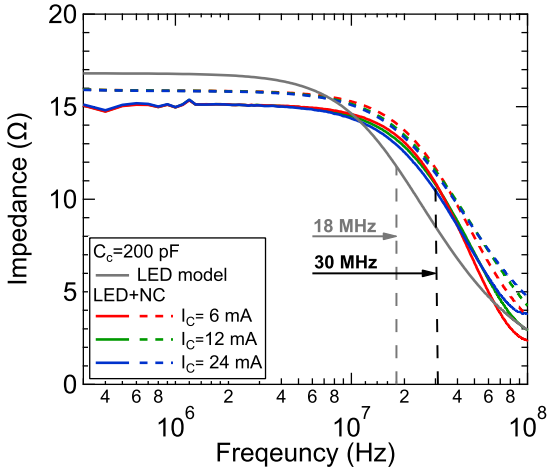
peaking behaviour is the increase in the Q-factor of the complex pole $p_{1,2}$, which is a function of both C_c and $-R_c$ as given by (4.16). Hence, the combined effect of increasing both C_c and $-R_c$ leads to the consequential increase in peaking amplitude, which is most prominent in Figure 4.9c where $I_C = 24$ mA and $C_c = 500$ pF that is the highest values of the two parameters.

Therefore, it can be inferred that increasing C_c provides a significant bandwidth extension of approximately 200% for the lowest current $I_C = 6$ mA and up to 300% for the highest current $I_C = 24$ mA yet, at the expense of enhanced peaking. Moreover, looking at the DC resistance value for all I_C cases, it can be seen that the negative capacitance circuit results in a very slight reduction in the LED resistance; less than 2 Ω (10%). This slight reduction is due to the resistive loading caused by R_b.

The previous chapter concluded that increasing $-R_c$ is advantageous in generating a less frequency-dependent $-C_c$ and, therefore, improving the quality of neutralising any given capacitance. In contrast, in applying the negative capacitance circuit to extend the LED bandwidth, the effect of increasing $-R_c$ is dependent on the value of C_c. For example, when $C_c = 200$ pF for $I_C = 6$, 12 and 24 mA in Figures 4.9a, 4.9b and 4.9c, no improvement in bandwidth between the different I_C cases. Although, all cases yield significant bandwidth extension compared to the raw LED bandwidth. Such observation was appreciated in simulating both the impedance response and pole-zero action of the passive equivalent LED and negative capacitance models in Section 4.4.2. Where, it was shown for $C_c = 200$ pF in Figure 4.8a, the system has two real poles and that increasing $-R_c$ has a limited effect on the dominant real pole frequency location and, in turn, the bandwidth. Therefore, in this specific case, there is no advantage in increasing $-R_c$, and it's better to operate at lower bias currents to consume less power. Whereas, in cases where $C_c = 400$ pF and 500 pF in Figures 4.9a, 4.9b and 4.9c, the effect of increasing $-R_c$ results in significant bandwidth extension. Similarly, such behaviour was evident from the pole-zero action of the passive equivalent model in Figures 4.8c and 4.8d, in both cases, the system bandwidth is determined by a complex conjugate pole $p_{1,2}$ and increasing $-R_c$ has the effect of increasing both the natural frequency f_n

and the quality factor Q, resulting in a notable increase in bandwidth and peak amplitude. Such observations suggest that the interplay between the values of C_c and $-R_c$ dictates both the bandwidth extension and the frequency behaviour in terms of peaking. Hence, it is important to evaluate the values of C_c and I_C of the negative capacitance circuit, based on a study of the pole behaviour to realise the utmost bandwidth gains for each distinct LED model.

Figures 4.10a and 4.10b strongly support the aforementioned conclusions by looking at the compensated LED impedance for a fixed C_c and $I_C = 6$ mA, 12 mA



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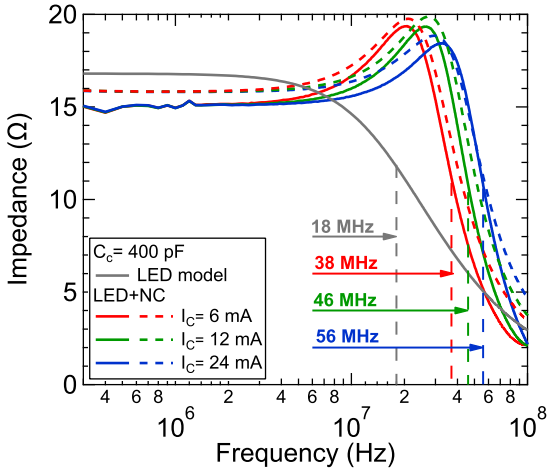


(b)

Figure 4.10: Measured (solid) and simulated (dashed) impedance of the LED equivalent model when connected to the negative capacitance circuit for different I_C at (a) $C_c = 200$ pF (b) $C_c = 400$ pF

and 24 mA. In Figure 4.10a, $C_c = 200$ pF, no improvement in the cut-off-frequency as I_C is increased. Whereas, in Figure 4.10b, $C_c = 400$ pF, clearly increasing I_C results in significant bandwidth enhancement. Therefore, it is clear that below certain level of C_c there is limited bandwidth extension as a result of increasing $-R_c$, which is only notable in cases with higher C_c values.

Conclusively, it is evident that the application of the negative capacitance circuit to offset the bandwidth-limiting effect of the LED junction capacitance results in a significant bandwidth enhancement with almost negligible loss in the DC resistance, which in theory can be avoided by employing a current mirror instead of the bias resistor R_b, to present a higher AC resistance. This suggests that the proposed LED bandwidth extension technique enhances the LED bandwidth without compromising its optical power intensity, as will become evident from the application of the proposed technique to commercially available LEDs described in the next section. Nevertheless, it is worth noting that despite being optically lossless, the proposed LED bandwidth extension technique will lead to increase in power consumption of the LED driver circuit. However, such an increase in power consumption is relatively lower than the power consumed by the LED, since the negative capacitance circuit operates at a fraction of the LED forward current.

4.5 Optical Measurements based on LEDs

In this section, first, the procedure for a simple LED passive equivalent circuit model extraction is described to aid in designing the appropriate negative capacitance equalisation circuit to extend the LED modulation bandwidth. Then, following the LED parameter extraction, a bespoke design of the negative capacitance circuit is described according to the extracted LED parameters.

4.5.1 LED Model Extraction

The LED parameter extraction is carried out for two LEDs, shown in Figure 4.11, which are of different colours and manufacturers. First, the electrical DC current-voltage characteristics are measured, which is used to derive r_d by calculating the local gradient for each current. Second, the LED return loss (S_{11}) is measured using VNA for a range of bias voltages generated by an external bias-T. The S_{11} responses is then converted to the corresponding Z_{11} to obtain the LED impedance response. The values of R_s and C_j are then extracted by curve-fitting simulations of the simplified LED equivalent model in Figure 4.1a to the measured S_{11} and Z_{11} responses of each LED at different LED forward currents I_f. Moreover, the Z_{11} responses is used to predict the LED cut-off-frequency using (4.9).

The VNA output power was set to -15 dBm to ensure the LED is operating in the linear region and avoid any distortion. The LED cut-off-frequencies obtained from the Z_{11} curves is compared to that obtained from the S_{21} measurements to verify the reliability of using the LED passive equivalent circuit model as the basis for designing the negative capacitance circuit. The LED S_{21} measurements are

(a) (b)

Figure 4.11: LEDs under test (a) Blue (b) Red

carried out using a simple VLC experimental set-up shown in Figure 4.16. For the S_{21} measurements, the VNA output power was increased to 3 dBm to provide sufficient optical power at the receiver. The LED modelling and parameter extraction procedure are similar for the two LEDs. Nevertheless, the LED model extraction is limited to 100 MHz for the blue LED in Figure 4.11a and 200 MHz for the red LED Figure 4.11b, which was chosen in relation to their nominal operating frequencies.

It is worth noting that in VLC links, it is common to operate the LED at currents higher than the midpoint of its linear region to benefit from the higher modulation bandwidth. Nevertheless, this could introduce some non-linear distortion and might reduce the signal swing and, as such, the SNR. Hence, the choice of the LED bias point often requires optimisation between parameters like bandwidth and SNR to achieve the highest attainable capacity as studied in [113]. However, in this experiment, optimisation of the LED bias point is not addressed, yet each LED is measured at various currents to check the model validity and give a wide range of capacitances for validation of the efficacy of the negative capacitance compensation circuit under different operating conditions.

Blue LED Model Extraction

The LED parameter extraction is carried out for a blue (455 nm) Osram Opto Golden Dragon, LD W5SM LED. Figure 4.12a shows the measured LED DC current-voltage characteristics, which is used to derive r_d by calculating the local gradient for each current. Noting that the curve starts at 2.5 V, which is the turn on voltage of the LED as indicated by the manufacturer. Whereas, Figures 4.12b and 4.12c, respectively show the measured S_{11} and derived Z_{11} for the LED at $I_f =$

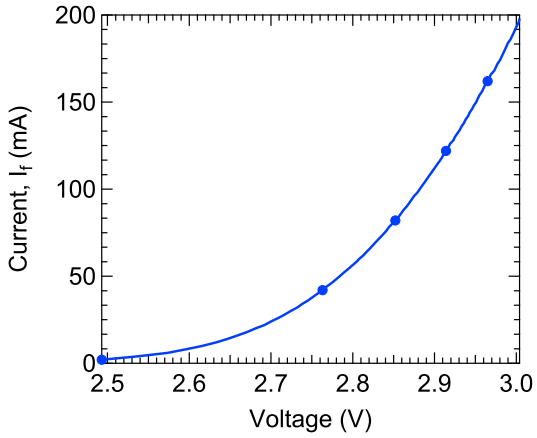
Table 4.1: Blue LED extracted model parameters at various currents

Bias (V, mA)	R_s (Ω)	r_d (Ω)	C_j (nF)	BW (MHz)
(2.72, 20)	0.7	4.3	6.3	5.9
(2.87, 60)	0.7	1.65	8.5	11.3
(2.96, 100)	0.7	1	9.8	16

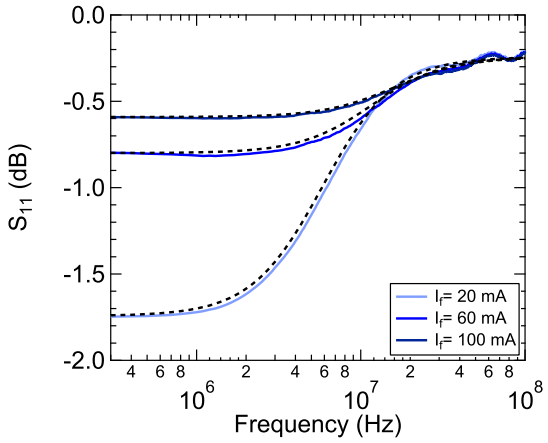
20 mA, 60 mA and 100 mA. Table 4.1 presents the extracted parameters of the LED equivalent model at each current.

By inspecting the LED impedance curves in Figure 4.12c, it can be seen that for all I_f cases, the LED passive equivalent model curves (dashed) deviates from the measured responses at high frequencies (beyond 50 MHz), where the measured LED impedance response exhibits an impedance increase that the equivalent model does not depict. At such frequencies, the effect of the inductance of the LED packaging becomes more significant, and as such, it presents a rise in the impedance that is not reflected by the basic LED passive equivalent circuit model of Figure 4.1a, which is adopted in the LED parameter extraction. Therefore, to achieve better matching between the measured LED impedance Z_{11} and the equivalent model at such frequencies, then the high frequency model of Figure 4.1b would present a better match since it considers the effects of the LED packaging parasitics. Nevertheless, adopting the high frequency LED model as the basis of the negative capacitance circuit design would result in a more complex impedance equations compared to (4.8) and (4.11), which would make the design and performance predictions of the negative capacitance circuit with the LED more challenging. Moreover, for this particular LED, the effect of the LED packaging parasitics are at frequencies beyond the LED cut-off-frequency, so it does not affect the accuracy of the LED model parameter extraction and, in turn, the associated negative capacitance circuit design. Hence, in such a case, it is sufficient to use the basic LED passive equivalent circuit model of Figure 4.1a.

As for the LED impedance behaviour, it is clear from Figure 4.12c and extracted parameters in Table 4.1 that increasing the LED forward current I_f reduces r_d, as given by (4.3), which in turn increases the LED modulation bandwidth as predicted by (4.9). Yet, such reduction in r_d is also accompanied by an increase in C_j, as a result of reducing the width of the depletion region W_D in (4.4). As such, increasing I_f would initially increase the LED bandwidth, until the associated increase in C_j becomes dominant over the reduction in r_d, reaching a saturation point beyond which increasing I_f will not increase the bandwidth further and would result



(a)



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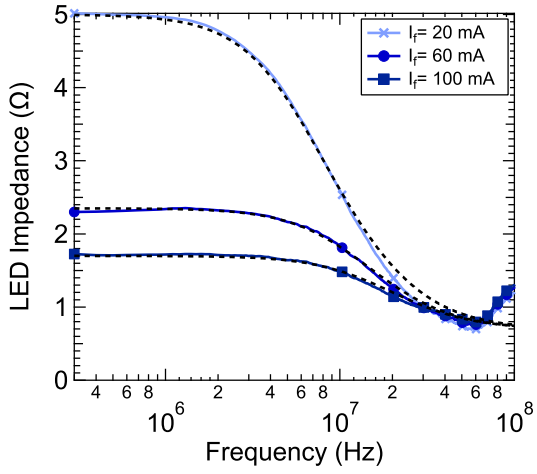


(c)

Figure 4.12: Measured (solid) and fitted model (dashed) blue LED responses (a) IV characteristics (b) S_{11} (c) Z_{11}

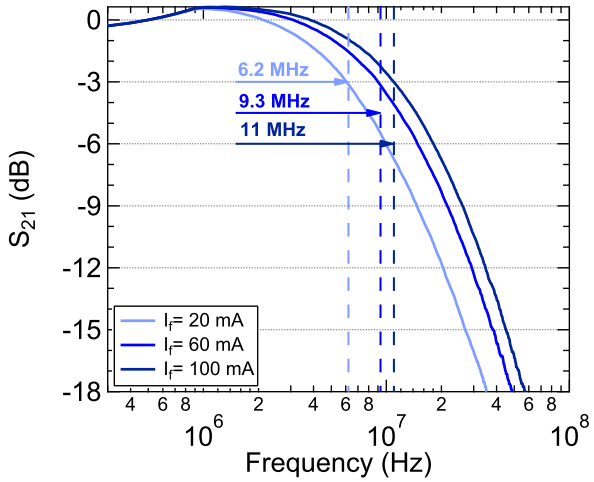


Figure 4.13: Measured S_{21} of the blue LED at different I_f

in reduction in the LED optical power.

The extracted LED model parameters are used to predict the LED cut-off-frequency using (4.9) as presented by Table 4.1, which are then compared to cut-off-frequencies obtained from measurements of the LED S_{21} responses. Figure 4.13 shows the normalised LED S_{21} response for $I_f = 20$ mA, 60 mA and 100 mA, where clearly increasing I_f increases the LED cut-off-frequency. Moreover, the S_{21} cut-off-frequencies show a reasonably good agreement with the predictions based on the basic LED equivalent circuit model of Table 4.1. Hence, verifying the accuracy of the basic LED passive equivalent circuit model and the parameter extraction in predicting the LED behaviour, as such, provides a reliable basis for further negative capacitance circuit design.

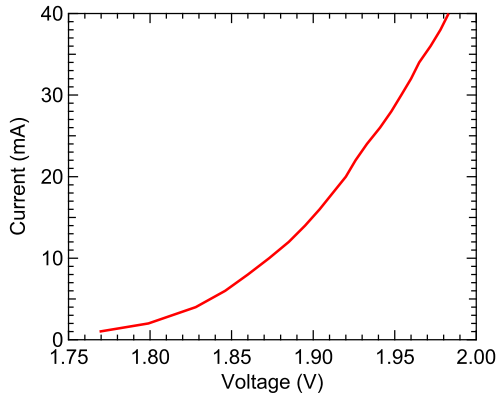
It is worth noting that a similar parameter extraction procedure was experimentally conducted for red and green colour LEDs from the same manufacturers, where the simplified LED passive equivalent circuit model also showed to fit accurately the measured S_{11} and Z_{11} of each LED. Nevertheless, such measurements are not shown to avoid redundancy, since the LEDs exhibit similar trends yet at slightly different bandwidths.

Red LED Model Extraction

The LED parameter extraction is carried out for a red (660 nm) Hamamatsu, LED L10762, with relatively higher bandwidth than the blue Osram Opto Golden Dragon, LD W5SM LED. This is attributed to both the smaller size and internal resonant cavity structure. The intention of modelling and performing parameter extraction for such an LED is to examine the behaviour of different types of LEDs. Moreover, investigate the utility and efficiency of the negative capacitance circuit in extending the bandwidth of LEDs of different sizes, types and bandwidths.

The parameter extraction for the red LED was found to be more challenging, especially when adopting the basic LED passive equivalent circuit model of Figure 4.1a, which showed to be insufficient to model the measured LED S_{11} and Z_{11} responses. This is because, for this particular LED, the interaction between the LED packaging parasitic elements, the different internal elements (r_d and C_j) and their dependence on the bias makes the LED behaviour more intricate to predict. Nevertheless, empirically, the measured S_{11}, Z_{11} and the S_{21} can be all used to obtain a reasonable prediction of the parameter values of the basic LED equivalent circuit of Figure 4.1a, which is for the design of the negative capacitance circuit.

Figure 4.14a shows the DC current-voltage characteristics, from which the values for r_d is estimated based on the local gradient at each current value. Noting that the curve starts at 1.75 V, which is the turn on voltage of the LED as indicated by the manufacturer. Figures 4.14b and 4.14c, respectively show the measured S_{11} and Z_{11} for the LED at currents of 5 mA, 10 mA and 20 mA and 30 mA. Whereas, Figure 4.15 shows the normalised S_{21} responses at each current. It is clear from the impedance response in Figure 4.14c, that the basic LED passive equivalent circuit model shows significant deviation from the LED measured responses, especially at high frequencies and high currents, where the measured impedance responses do not exhibit the typical RC first-order filter roll-off, yet shows a significant impedance rise, especially at high LED forward currents ($I_f = 20$ mA and 30 mA). Nevertheless, considering Figure 4.14c and 4.15, it is noted that at low current values ($I_f = 5$ mA), where the dynamic resistance is high, the RC response is evident in



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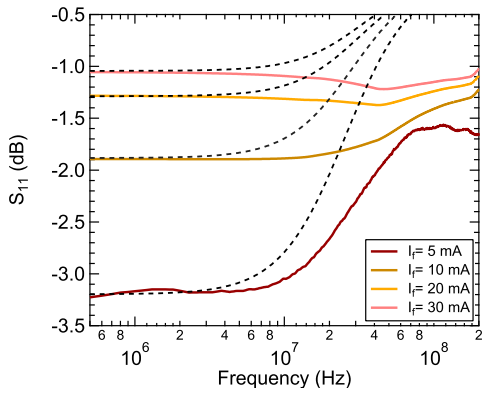

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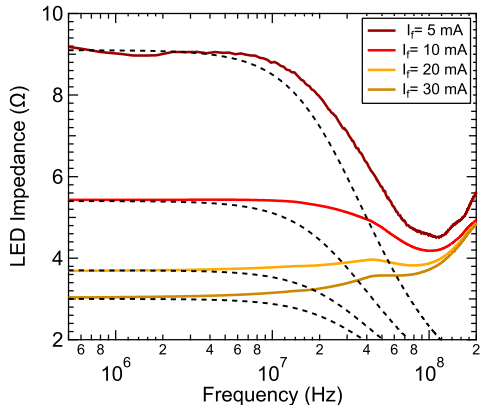


(c)

Figure 4.14: Measured (solid) and fitted model (dashed) red LED responses (a) IV characteristics (b) S_{11} (c) Z_{11}

both the LED impedance Z_{11} and the corresponding S_{21} response. From this and knowing the dynamic resistance variation with current, in addition to the S_{21} cut-off-frequencies, the LED capacitance can be estimated for different current values and as a function of current if required. Such technique is utilised to predict capacitance

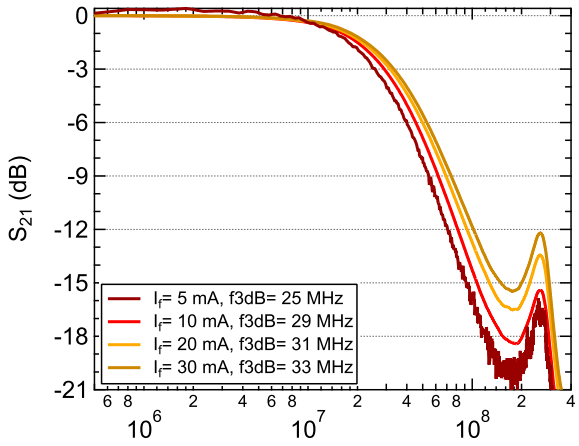


Figure 4.15: Measured S_{21} of the red LED at different I_f

values at high LED forward current I_f, where there is little frequency variation of the diode impedance as the packaging inductance becomes the dominant frequency effect. Table 4.2 presents the LED model parameter values at the different I_f.

Another interesting observation to note from the S_{21} responses in Figure 4.15 is high frequency peaking behaviour, which is seen to be at a fixed frequency for all I_f cases, yet with different magnitude. When applying the negative capacitance circuit in the next section, this peak will be seen to shift to lower frequencies and, as a result, will extend the LED bandwidth. Furthermore, the values of $-C_c$ and $-R_c$ of the negative capacitance circuit will also influence the frequency of such peak, as will be further discussed in Section 4.5.2.

Table 4.2: Red LED extracted model parameters at various currents

Bias (V, mA)	R_s (Ω)	r_d (Ω)	C_j (nF)
(1.79, 5)	0.4	8.7	0.7
(1.87, 10)	0.4	5	1.1
(1.91, 20)	0.4	3.3	1.51
(1.95, 30)	0.4	2.6	1.83

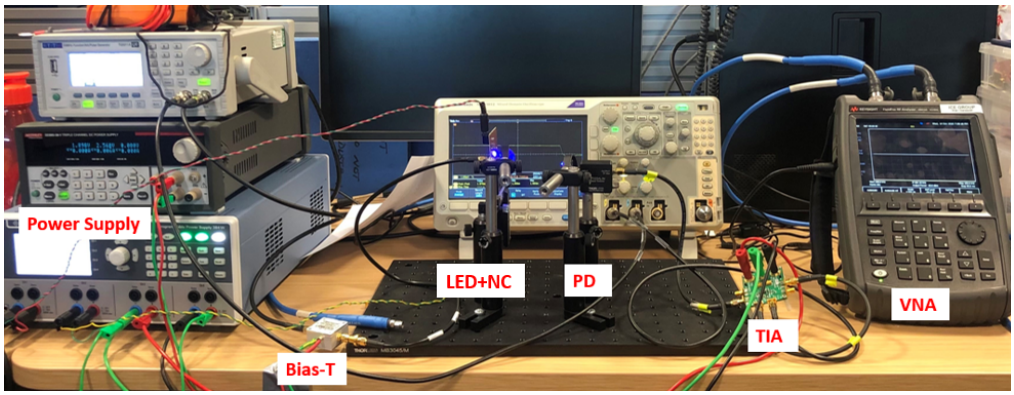


Figure 4.16: Test set-up to measure LED+NC impedance and S_{21}

Table 4.3: Key System Parameters

Element	Value
LED	OSRAM, LD W5SM-424T Blue LED, Hamatsu, L10762, Red LED
Bias-T	Mini-Circuits ZFBT-4R2GW-FT+, 0.1- 4.2 GHz
Photodiode	Thorlabs DET025ALM, bandwidth 2 GHz
Lens	Convex, focal length
TIA	HMC799, bandwidth 600 MHz, gain 10 kΩ

4.5.2 Negative Capacitance for LED Bandwidth Extension

First, the negative capacitance circuit utility was verified by measuring the quality of its negative capacitance generation. The circuit is then applied to two commercially available LEDs, independently, and its bandwidth extension advantage is examined using a simple experimental test set-up shown in Figure 4.16. The set-up consists of each of the LEDs and the negative capacitance circuit PCB, a Thorlab high-speed photodiode (DET025AL/M) and a 600 MHz Analog Devices transimpedance amplifier (HMC799LP3E). The LED is biased using a Mini-Circuit (ZFBT-4R2GW-FT+) bias-T and is driven using port 1 of the VNA. A short free-space optical channel of a fixed distance connects the output of the LED to the optical receiver assembly; port 2 of VNA is used to monitor the output of the receiver. In addition to using culminating lens at the transmitter and receiver sides. Noting that the bandwidth of the optical receiver is well above that of each LED and associated circuitry, S_{21} mea-

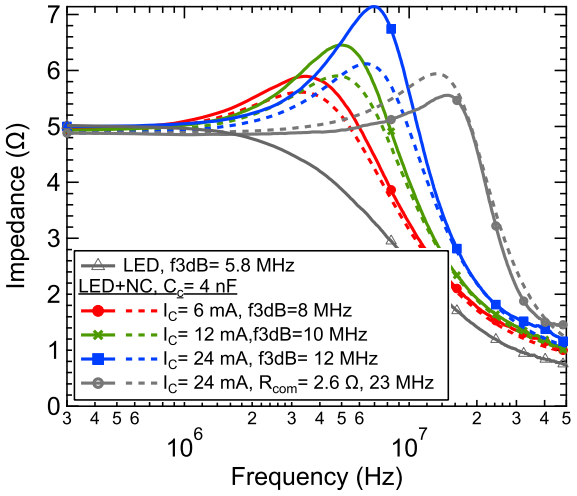
surement of the VNA would describe the frequency behaviour of each LED and can be used to demonstrate and study the effect of negative capacitance compensation.

The effect of compensating for the bandwidth-limiting LED junction capacitance by utilising the negative capacitance circuit is investigated by first, examining the effectiveness of increasing C_c in extending the LED cut-off-frequency. Moreover, the influence of $-R_c$ on the achievable bandwidth extension by varying I_C of the negative capacitance circuit. The electro-optical response of each LED is measured independently and with the application of the negative capacitance circuit, based on S_{21} measurements of the optical link shown in Figure 4.16.

Compensated Blue LED Measurements

Figures 4.17a and 4.17b show the measured LED impedance and S_{21}, respectively, at $I_f = 20$ mA for a fixed $C_c = 4$ nF and I_C is varied to 6 mA, 12 mA and 24 mA. For $I_C = 24$ mA, an additional case is introduced, where a series compensating resistance R_{com} is placed at the input of the negative capacitance circuit, where $R_{com} = 2.6\ \Omega$, this is done to offset $-R_c$ without having to increase I_C further.

From Figure 4.17a, it can be seen that measurements of the LED impedance closely agree with the simulation of the transistor circuit. Moreover, it is clear that increasing I_C progressively enhances the bandwidth with a gradual increase in the peaking amplitude. Similar behaviour was predicted in the simulation of the impedance response of the passive equivalent circuit model in Section 4.4.2. Moreover, in the case where a series resistance R_{com} is added, a remarkable bandwidth extension of almost 400% compared to the raw LED bandwidth is achieved. Hence, it can be inferred that mitigating the effect $-R_c$ either by increasing transistor currents I_C or by the introduction of the series compensating resistance R_{com} results in the generation of a less frequency-dependent negative capacitance $-C_c$ and hence more effective LED bandwidth extension. Moreover, looking at the DC resistance value, it can be seen that the negative capacitance circuit does not result in any reduction of the LED resistance, which suggests that no optical power loss is incurred, as is verified by the experimental S_{21} results below. It is important to recall that the negative capacitance circuit does not cause any loading to the LED, when



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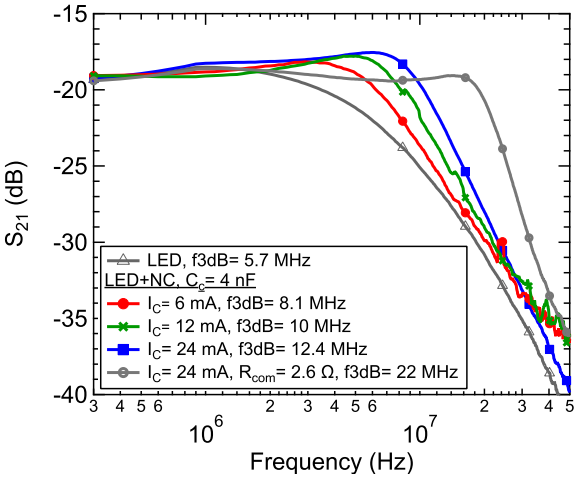


(b)

Figure 4.17: Measured blue LED responses at $I_f = 20$ mA and $C_c = 4$ nF for different negative capacitance circuit bias currents I_C (a) Z_{11} (b) S_{21}

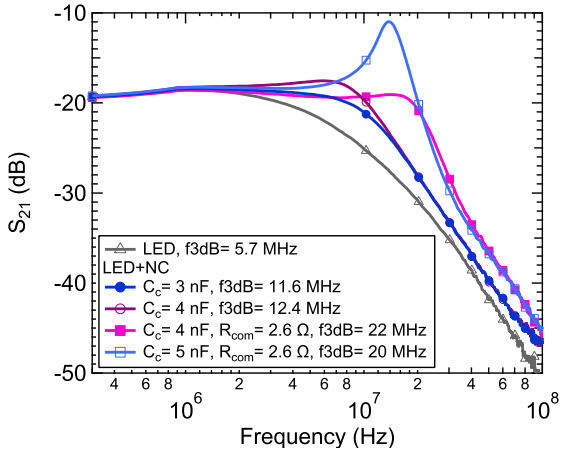
$R_b >> (R_s + r_d)$ in Figure 3.1. Notably, the application of negative capacitance circuit to extend LED bandwidth does not trade-off bandwidth for optical power.

All subsequent S_{21} measurements are taken with VNA port 2 being the output of the optical receiver and port 1 being the input to the LED transmitter circuit. As such, the exact value of the S_{21} parameter is of little importance; however, the relative variation within each figure and across the different figures are used to illustrate the behaviour of the LED transmitter. For example, from Figure 4.17b, it is clear that S_{21} follows a similar trend to that predicted by the LED impedance in

Figure 4.17a, where the bandwidth gradually increases as I_C is increased, accompanied by a slight peaking. Moreover, the received optical power remains constant in all four cases as was reflected by the impedance measurement in Figure 4.17a. Therefore, it can be deduced that the application of negative capacitance circuit to the LED results in effective bandwidth extension without compromising optical power. Note that the S_{21} response is intentionally unnormalised to highlight the advantage of the negative capacitance equaliser versus other lossy equalisers that are abundantly used in numerous VLC reports as [15, 20]. Furthermore, it is deduced that increasing I_C of the negative capacitance circuit is desirable to mitigate the constraint imposed by its negative resistance $-R_c$ on the LED bandwidth extension. Nevertheless, this would result in increased power consumption. However, it is also possible to offset the negative resistance by placing a series compensating resistor R_{com} at the circuit input without having to increase I_C further. Therefore, to obtain optimal bandwidth performance, the undesirable effect of $-R_c$ is minimised by either opting to bias the circuit at $I_C = 24$ mA or by the addition of $R_{com} = 2.6\ \Omega$ for all the subsequent measurements.

Figures 4.18a, 4.18b and 4.18c illustrate the measured S_{21} for $I_f = 20$ mA, 60 mA and 100 mA, respectively and for different C_c values. In Figure 4.18a, $C_c =$ 3 nF results in significant increase in bandwidth of more than 200% compared to the bandwidth with only the LED. Whereas, in the case where $C_c = 4$ nF, it has minimal effect on the bandwidth, yet results in enhanced peaking. Such behaviour is explained due to the limitation imposed by $-R_c$ on the LED bandwidth extension, which was highlighted by simulations of the impedance responses and pole-zero action of the passive equivalent circuit model of the LED and the negative capacitance circuit in Section 4.4.2. However, this limit is counteracted by the introduction of R_{com} at the input of the negative capacitance circuit, while keeping $C_c = 4$ nF, which results in a substantial bandwidth extension of almost 200% compared to the case $C_c = 4$ nF without R_{com}. Nevertheless, $C_c = 5$ nF and $R_{com} = 2.6\ \Omega$ case results in substantial increase in peaking and slight bandwidth reduction.

In Figures 4.18b and 4.18c, similar behaviour is observed, where increasing C_c



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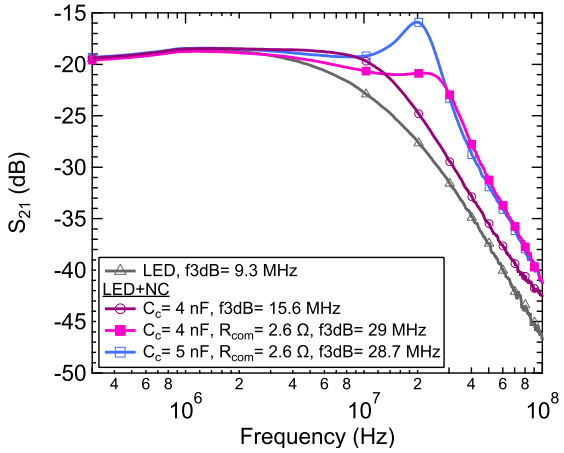

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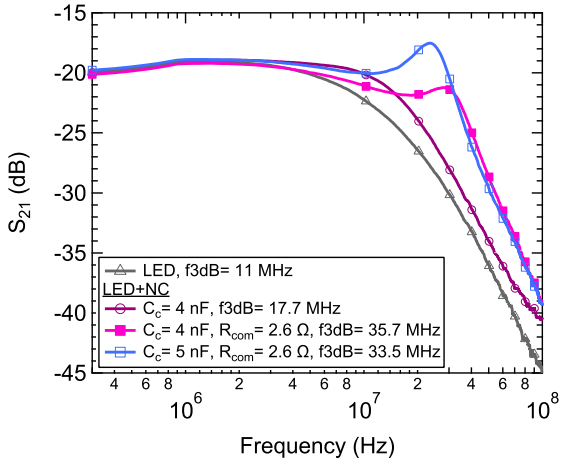


(c)

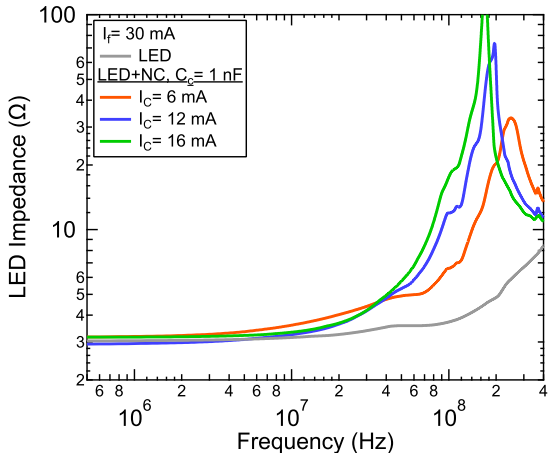
Figure 4.18: Blue LED S_{21} magnitude measurements at $I_C = 24$ mA for different LED forward current I_f (a) 20 mA (b) 60 mA (c) 100 mA

leads to substantial bandwidth extension at a constant received optical power. In the best case, in Figure 4.18c, where $C_c = 4$ nF and $R_{com} = 2.6\ \Omega$, bandwidth of almost 36 MHz is achieved as opposed to 11 MHz uncompensated LED bandwidth, which is a substantial improvement of approximately 360%. Moreover, it is clear that in all curves shown in Figures 4.18a, 4.18b and 4.18c, the signal power is maintained and the application of the negative capacitance circuit, regardless of its bias conditions and capacitance values, is always optically lossless. This can be contrasted with alternative equalisation techniques, for example RC-based equalisers, such as described in [112], where bandwidth was extended by factors slightly higher than what is reported in this work but at the cost of 15 dB loss in received signal power. On the other hand, the negative capacitance circuit will have different degrees of bandwidth neutralisation and frequency peaking amplitudes for different LED currents I_f, as a result of the dependence of LED parameter (r_d and C_j) on current (see Table 4.1). For example, increasing C_c to 5 nF, high frequency peaking appears and it is most prominent for lower diode bias currents as Figure 4.18a, as these will result in lower values of C_j. As such, high peaking may affect the pulse response of such systems and care must be taken when designing the negative capacitance as the design must take into consideration the equivalent circuit of the LED and its operating parameters.

Conclusively, it is evident that using a negative capacitance circuit in parallel with an LED results in significant enhancement of the latter's bandwidth, without compromising the transmitted optical power. Moreover, measured S_{21} of the overall optical link exhibits similar behaviour to that predicted based on the LED impedance model, which means that studies of effects of negative capacitance circuit on the LED impedance are useful as a base to predict the LED electro-optical response versus frequency.

Compensated Red LED Measurements

Figures 4.19a and 4.19b show the measured LED impedance and S_{21} responses, respectively, at $I_f = 30$ mA, $C_c = 1$ nF and I_C of the negative capacitance circuit is varied to 6 mA, 12 mA and 16 mA. From Figure 4.19a, it can be seen that increasing I_C shifts the LED impedance peak to lower frequencies, while also increasing its amplitude. Such behaviour is clearly reflected in the corresponding S_{21} response for each I_f case in Figure 4.19b, where for $I_C = 6$ mA, the LED bandwidth is extended by 155% compared to its uncompensated bandwidth (from 34 MHz to 53 MHz) and the high frequency peak is seen to shift to lower frequencies. Increasing I_C to 12 mA and 24 mA lowers the peak frequency further, which results in a substan-



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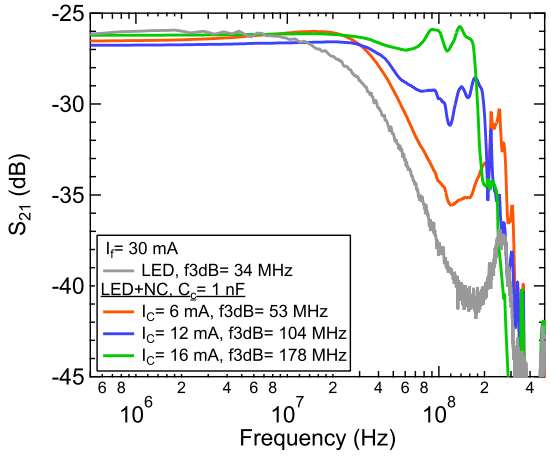


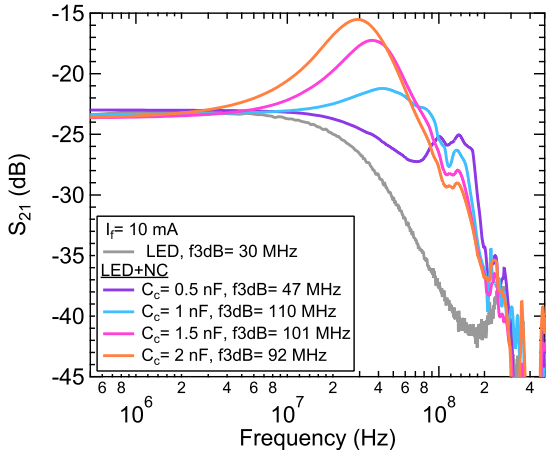
(b)

Figure 4.19: Measured red LED responses at $I_f = 30$ mA and $C_c = 1$ nF for different I_C (a) Z_{11} (b) S_{21}

tial bandwidth extension of 300% and 520% compared to the uncompensated LED bandwidth, respectively, with no loss in optical power. Increasing I_C of the negative capacitance circuit reduces its $-R_c$ component, which was previously shown to improve the quality of the generated negative capacitance as discussed in Section 4.4.2, and in turn enhances LED bandwidth extension. Yet, in the case of this particular LED, the bandwidth extension is also achieved by the interplay of the $-C_c$ and $-R_c$ and the frequency peak inherent to the LED S_{21} responses.

Since, it is established that biasing the negative capacitance circuit at $I_C =$ 24 mA achieves the highest bandwidth extension of the LED. The S_{21} of the compensated LED is measured at $I_C = 24$ mA for different C_c values at LED forward currents $I_f = 10$ mA, 20 mA and 30 mA. Figures 4.20a, 4.20b and 4.20c illustrate the measured S_{21} for $I_f = 10$ mA, 20 mA and 30 mA, respectively, at different C_c values. Clearly, that for all I_f cases, increasing C_c leads to substantial bandwidth extension at a constant received optical power. Yet again it is evident that the negative capacitance circuit results in different degrees of bandwidth extension and frequency peaking amplitudes for the different LED currents I_f, which as previously explained is a result of the dependence of LED parameter (r_d and C_d) on I_f. For instance, for $C_c = 2$ nF, frequency peaking appears and is most prominent for lower values of I_f (10 mA and 20 mA) as shown by Figures 4.20a and 4.20b, as these will result in lower values of C_j. Whereas, in the case of $I_f = 30$ mA, the $C_c =$ 2 nF results in relatively lower peaking, yet the highest bandwidth with a reasonably flat response at $C_c = 1$ nF.

Hence, based on the S_{21} behaviour of the compensated LED, it can be concluded that the negative capacitance circuit is effective in extending the LED bandwidth with no loss in optical power, yet careful selection of the values of $-C_c$ and the bias conditions is necessary to obtain optimal bandwidth performance with reasonable peaking levels.



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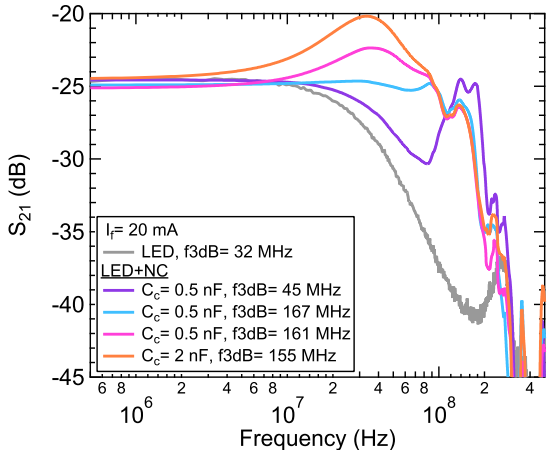

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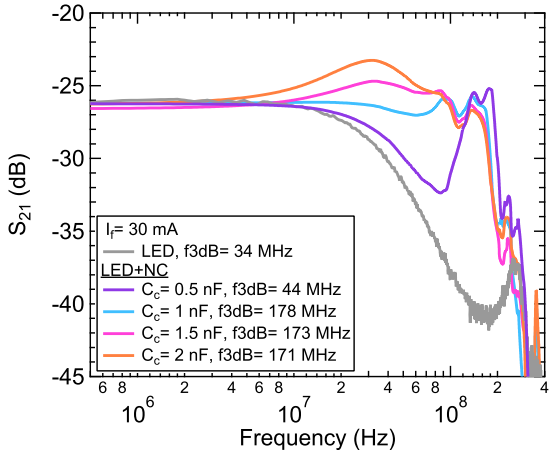


(c)

Figure 4.20: Measured S_{21} responses of the red LED for different C_c for (a) $I_f = 10$ mA (b) $I_f = 10$ mA (c) $I_f = 30$ mA

4.6 Discussion & Conclusions

This chapter described a new optically lossless LED bandwidth extension technique based on the application of a purpose-designed negative capacitance circuit. The chapter commenced with a brief survey of existing LED passive equivalent circuit models and their accuracy in predicting the LED behaviour, from which it was identified that the LED can be modelled by a simple parallel RC network in series with a series contact resistance. The parallel RC network is associated with the LED dynamic resistance and junction capacitance and are the factors that set the ultimate limit of the LED modulation bandwidth. The chapter also discussed some of the notable circuit-based LED bandwidth extension techniques reported for VLC systems. It was concluded that most of the reports are based on resistive lossy passive equalisers, resulting in substantial loss of the LEDs optical power. Moreover, the design of such equalisers is often based on trial and error, and as such, does not provide a holistic solution for enhancing the bandwidth of different LEDs.

Motivated by the limitations of such passive equalisers, a new optically lossless bandwidth extension circuit technique is proposed. The technique is based on introducing a negative capacitance circuit in parallel with the LED junction capacitance, hence, alleviating its bandwidth-limiting effect. One of the key advantages of the proposed circuit is that it does not result in resistive loading of the LED, therefore, the resultant bandwidth extension is at zero optical power loss. The design principle and optimisation of the proposed bandwidth extension technique were detailed, based on mathematical derivations, simulation-based analysis of the LED impedance responses and pole-zero behaviour. The bandwidth advantage of the negative capacitance circuit was verified through measurements in conjunction with two commercially available LEDs of different colours (blue and red) with a simple VLC link. Measurements demonstrated a bandwidth extension of more than 300% for a blue LED and more than 500% for a red LED, without any loss in optical power. Such bandwidth enhancement is substantial compared to currently reported LED bandwidth extension circuits as in [15, 20, 27, 112], which provide similar bandwidth enhancement yet with power penalties up to 25 dB. Furthermore,

measurements showed that careful optimisation of the operating conditions of the negative capacitance circuit in relation to each LED is required to achieve the highest bandwidth at well-behaved frequency behaviour.

Chapter 5

Low Input Impedance Configurations of TIAs

5.1 Introduction

In this chapter, a review of transimpedance amplifiers (TIAs) reported to date is presented, highlighting the key configurations and techniques adopted to achieve high gain and wide-band operation. It is identified that it is advantageous to employ low input impedance TIAs in applications with large photodiode capacitance to achieve wide-band operation. Therefore, key low input impedance TIA configurations; the common base (CB), the regulated cascode (RGC) designs are described, including their operation, main advantages and drawbacks. Modifications of the conventional CB and RGC stages are also discussed, based on circuit techniques that treat some of the inherent limitations of the conventional designs. The suitability of each low input impedance TIA configuration to VLC receiver's applications is also discussed, which identified the RGC configuration as a good balance between the key TIA design parameters, namely bandwidth, transimpedance gain and stability.

5.2 Design Techniques of Optical Pre-amplifiers

In optical receivers, the TIA is a crucial block since it is the first gain stage following the photodiode. Hence, it is a primary determinant dictating the performance of the overall optical receiver. In the application of optical fibre communication, the junction capacitance associated with photodiodes is commonly in the range of 0.2 pF to 1 pF, depending on the photodiode surface area [114]. Typically, it is desirable to employ large-area photodiodes to boost the amount of captured light at the receiver; this increases the received signal power to cater for longer transmission spans. Nevertheless, the large junction capacitance associated with such large-area photodiodes severely restricts the optical receiver bandwidth, which makes the design of a wide-band high gain TIAs significantly challenging.

Classically, TIAs employing shunt feedback (SFB) were employed for their advantage of achieving high gain and acceptable noise performance. Nevertheless, such gain and noise advantage comes at the expense of reduced bandwidth especially, in the presence of high photodiode junction capacitance (C_{pd}). Therefore, SFB TIAs are usually combined with additional bandwidth techniques such as inductive [115, 116] and capacitive peaking [117]. Alternatively, designs have been reported that utilise key bandwidth extension techniques, such as low input impedance amplifiers featuring CB input configuration [118, 119], which offer much improved isolation of C_{pd} from the bandwidth determination of the optical receiver in comparison to the SFB TIA counterpart. For extremely low input impedance, the RGC was first reported in 2000 in [120, 121], mainly to boost the transconductance (g_m) of the common gate (CG) configuration in TIAs employing field effect transistors (FETs).

The necessity of boosting the g_m of the CG stage stems from the fact that at a given current, the g_m offered by FETs are significantly lower than bipolar junction transistors (BJTs), which can limit the achievable bandwidth [122]. Therefore, for FETs to match the bandwidth performance of BJTs, it would require operation at a significantly high current, which is not practical in terms of power consumption. To overcome the trade-off between bandwidth and power consumption en-

countered in designs employing FETs, g_m-boosting techniques were proposed. One of the earliest derivatives of the CG stage used for g_m-boosting is the RGC, achieving reasonable balance between key TIA requirements such as large bandwidth, gain and acceptable power consumption [21, 120, 121]. Despite its contemporary record performance, the trend of down-scaling CMOS technology to obtain higher f_T continued incessantly to drive design modifications to obtain higher bandwidth and gain at lower powers. Low power operation is required mainly to prevent destructive breakdown in CMOS transistors and to satisfy the low power operation in very large scale integration (VLSI). Yet, low power operation limits the amplifier currents and, in turn, the achievable g_m, resulting in lower gains and bandwidths. Subsequently, different g_m-boosting configurations based on modifications of the CG and the RGC stage were reported, which combine techniques such as negative feedback [123, 124], dual negative feedback [125, 126], current reuse techniques [127, 128] to obtain extremely low input resistance and hence, alleviate a major culprit of bandwidth limitation, namely, the large C_{pd}.

On the other hand, for the application of VLC systems, standard TIA design techniques are applicable; however, some characteristics of such systems introduce additional design constraints. Firstly, the nature of the free-space channel mainly relies on line-of-sight, with received power being inversely proportional to the square of the distance. Secondly, most photodiodes operating in the visible range are silicon-based with relatively poor responsivity, thus, limiting the converted photocurrent. To alleviate these issues, usually, a high gain amplifier is required, or large photoactive area detectors [103, 129]. At best, a combination of both, especially for scenarios demanding large transmission distances between the transmitter and receiver. Nevertheless, the bandwidth limitation associated with large-area detectors is severe; hence careful optimisation of the TIA design is essential to enhance the receiver's bandwidth.

Despite the significance of the role of the TIA in a VLC link, limited research efforts have been committed to reporting specially designed TIAs to satisfy the requirements for practical VLC links. In fact, in conducting the literature review,

it was evident that there is a notable gap between the number of reports dedicated to the design of system-level aspects of VLC versus reports on circuits specifically TIAs. In this research effort, [23, 24, 130–135] were found to be the only notable reports of TIAs for VLC application in the literature.

Roger *et al.* (2005) reports an optical receiver front-end TIA suitable for optical wireless communication (OWC) applications, using 0.35 μm CMOS technology [130]. The structure of the receiver is based on a variable-gain TIA employing a low input resistance stage followed by a voltage amplifier, in addition to an ambient light rejection circuit. The low input resistance stage is implemented via a modified RGC stage, where the auxiliary RGC feedback amplifier based on a CS stage is replaced with a folded cascode stage. The advantage of using a folded cascode is to reduce the minimum voltage level requirement at the input node otherwise imposed by the CS stage and hence, make the RGC more suitable for low voltage designs. The modified RGC is followed by a CS stage for further gain. The achieved input resistance equals 40 Ω, providing an almost constant bandwidth of 114 MHz at C_{pd} of 5 pF and a variable gain of 0.3 kΩ to 1 kΩ. Meanwhile, this TIA achieves an insensitive bandwidth performance for more than triple the variation in transimpdance gain (from 0.3 kΩ to 1 kΩ). Yet, it falls behind in comparison to the comparable bandwidth reported in [24] also utilising the RGC as an input stage yet at C_{pd} two orders of magnitude higher (500 pF) and a transimpedane gain of approximately 5.5 kΩ. Such monumental difference in performance is attributed to the much lower input resistance achieved in [24] and possibly due to process variations.

An extension of the work in [130] is reported in [131], demonstrating the same TIA configuration yet with a more detailed study of the effect of the transimpedance gain variations on the TIA bandwidth. The TIA offers a maximum transimpedance gain of 24 kΩ at a bandwidth of 98 MHz and a minimum of 1.5 kΩ at 104 MHz. Despite the remarkably consistent bandwidth performance with such substantial variations in gain, this is achieved at an input capacitance of less than 0.5 pF, which simply bypasses a crucial bandwidth limitation, hence failing to reflect a practical design scenario. Similarly, work reported by Roger *et al.* (2016) demonstrates a

variable gain fully differential TIA using 0.18 μm CMOS process. The TIA utilises a low input resistance stage based on a modification of the CG employing a cross-coupled transistor pair for g_m-boosting, hence, achieving similar input resistance to the RGC configuration in [132]. The TIA offers transimpedance gain ranging from 55.8 dBΩ to 69.3 dBΩ at invariable bandwidth of 1 GHz with a C_{pd} of 1 pF. Such low C_{pd} would correspond to a significantly small area photodiode, which is again inadequate for free-space applications.

Works reported by Bassem *et al.* (2016) and Brandl *et al.* (2016) demonstrate free-space optical links consisting of a laser transmitter and a photodiode connected to a specially designed TIA, in addition to focal lens used at the transmitter and receiver to focus the laser beam on a small area photodiode at distances no more than 3 meters [133, 134]. At the receiver, the photodiodes used are of areas 100 μm x 100 μm [133] and 177 μm x 177 μm [134], which is equivalent to a C_{pd} of 650 fF and 700 fF, respectively. The TIA demonstrated in [133] is based on a dual-stage SFB TIA implemented using 0.35 μm CMOS technology. The individual amplifier stages are based on a differential pair configured in a cherry hopper structure to benefit from the immunity to common-mode noise and enhanced bandwidth performance. The TIA offers a bandwidth of 600 MHz, while the achieved gain is unclear. Whereas, the TIA demonstrated in [134] is based on a folded cascode amplifier with SFB implemented using 0.35 μm CMOS process. The choice of the folded cascode configuration is mainly to relax the voltage headroom limitation, while the use of feedback enhances the bandwidth. The TIA offers a bandwidth of 731 MHz at transimpedance gain equals 3 kΩ. In both links, the adopted TIA configurations tend to have higher input impedances in comparison to the low input impedance configurations such as the CG and the RGC. Hence, the recorded bandwidth is primarily a result of using very small area photodiodes; and hence, avoid creating a dominant input pole, which, with such high impedance TIA configurations would significantly reduce the bandwidth. Moreover, the use of such small area photodiodes severely limits the light collection and the receiver's field of view; therefore, the reported transmission distance ($<$3 meters) is achieved mainly

due to the high gain TIA and the use of a focused laser beam. Whereas, if the beam were to be diffused or worse, a LED was employed, then the distance would have been restricted to a few cm.

Most recently, Ehsan *et al.* (2020) reports a fully differential TIA utilising a RGC input using 0.18 μm CMOS process [23]. The RGC is followed by a voltage amplifier with current feedback from its output to the RGC input to obtain further reduction in the input resistance. The TIA offers a transimpedance gain of 68.8 dBΩ and bandwidth of 5.5 GHz at C_{pd} equals 650 fF. Adopting a combination of the RGC input stage and current feedback would offer significantly low input resistance, hence, decoupling C_{pd} from limiting the TIA bandwidth. Yet again, designing the TIA based on the assumption of such low C_{pd} (only 650 fF) is not pragmatic, since it does not sufficiently emulate the capacitance of a large-area photodiode.

A more practical VLC link is demonstrated by Hunag *et al.* (2012) reporting a monolithic optical receiver using 0.18 μm CMOS process, the integrated circuit consists of both the photodiode array and the TIA [24]. The TIA is based on a RGC followed by a SFB voltage amplifier. Whereas, the photodiode array is 850 μm x 850 μm equivalent to C_{pd} equals 500 pF. Note that this area is almost ten times bigger than the photodiodes area reported in [133, 134]. The TIA offers a considerable bandwidth of 100 MHz at a gain of 75 dBΩ. This remarkable bandwidth performance with such exceptionally high C_{pd} is attributed to the significantly low input resistance of the RGC (estimated to be approximately 3 Ω). A traditional 50 Ω input impedance amplifier would offer a bandwidth of approximately 6 MHz, hence, the use of the RGC results in bandwidth improvement of more than an order of magnitude. It is worth noting that the reported RGC is based on p-channel metal oxide semiconductor (PMOS) devices. Utilising a PMOS input stage boosts the photodiode cathode voltage in comparison to an n-channel metal oxide semiconductor (NMOS) RGC input stage, hence, reverse biasing the voltage of photodiode to reduce C_{pd} for a better optical response. Nevertheless, as will be described later in the RGC section, employing a PMOS devices limits the reduction in the input resistance in comparison to the NMOS counterparts.

Another well-designed example of a TIA for VLC applications is reported by Cura *et al.* (2013), which demonstrates a TIA consisting of a differential input stage followed by a voltage gain stage and an output buffer, where SFB is applied from the output buffer to the differential input to reduce the input resistance, hence, enhancing the bandwidth in the presence of large C_{pd} [135]. In contrast to all the aforementioned reports, the TIA is fabricated using 0.35 μm silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) process. Cura argues that increasing the gain of the open-loop amplifier extends the bandwidth of the closed-loop amplifier without reducing its transimpedance gain. The TIA demonstrates a bandwidth of 50 MHz and 10 kΩ at C_{pd} equals 50 pF. Since increasing the open-loop gain is of paramount importance for such feedback configuration as it dictates its bandwidth and transimpedance gain, it is rational to favour HBT over CMOS, since g_m of HBT devices does not depend on the device area and is proportional to the bias current. Unlike FETs where their g_m is a function of the device area and is proportional to the square root of the bias current. Hence, using FETs leads to higher area devices with reduced bandwidth capabilities and higher power consumption.

Table 5.1 presents a performance summary of the discussed TIAs designed for VLC application. While such efforts to have a specially designed TIA for VLC applications are appreciable and are based on carefully chosen design techniques whether in the form of the RGC, modifications to the RGC and the use of negative feedback. Nevertheless, except for work reported in [24, 135], the reported bandwidths are based on the use of relatively small area photodiodes [133, 134], hence small equivalent C_{pd} or by assuming a significantly small photodiode equivalent capacitance, few picoFarads in [130] and less than 1 pF in [23, 131–134]. Such capacitances are simply insufficient to mimic a practical large-area photodiode that is suitable for a realistic VLC link. Despite the shortcomings of the above reports in modelling a sufficiently large C_{pd}, yet based on their performance, three key observations can be made: i) The suitability and advantage of adopting low input impedance TIAs, especially the RGC configuration, in VLC receivers. ii) Evidently from [130, 131] that the use of the RGC configurations offers bandwidth insensitiv-

ity to transimpedance variations. Such an attractive feature is valuable in enhancing the flexibility of VLC receiver, since employing automatic gain control (AGC) is desirable due to the variety of received signal powers dictated by the distance. iii) The unexplored potential of employing HBT devices instead of CMOS for its advantage of higher g_m at any given bias current, therefore, can easily achieve low input resistance in designs like the CB and RGC configurations without resorting to additional bandwidth extension techniques.

Hence, based on the above discussion of different optical pre-amplifier design techniques, the following sections of this chapter survey a significant number of designs of TIAs reported up to date, which was found to be relevant to the design of TIAs for the application of VLC. First, the classical SFB configuration is described to highlight the advantage of employing low input resistance TIA configurations. Subsequently, low input resistance TIA configurations featuring the CB and the RGC together with some of their interesting derivatives are described.

Table 5.1: Performance summary of TIAs for OWC applications

Ref	**Topology**	**BW (MHz)**	**Gain (dBΩ)**	C_{pd} **(pF)**	**Tech. (μm)**
[130]	Folded cascode-RGC	114	60	5	0.35
[131]	Folded cascode-RGC	104-98	63.5-87.6*	0.5	0.35
[132]	Cross coupled CG (Fig.5.5d)	1000	55.8-69.3*	1	0.18
[133]	Diff. stage + shunt feedback	600-1200	-	0.65	0.35
[134]	Folded Cascode	731	69.5	0.7	0.35
[23]	RGC (Fig.5.5a)	5500	68.8	0.65	0.18
[24]	RGC	100	75	500	0.18
[135]	Diff. stage + shunt feedback	50	80	50	0.35

*Tunable transimpedance gain

5.3 Shunt Feedback TIAs

SFB TIAs are a well-acknowledged TIA topology that is customarily used for its high gain and satisfactory noise performance. Moreover, the use of feedback ensures flat transimpedance gain in the bandwidth of interest while reducing sensitivity to process and measurement variations [136]. Figure 5.1 shows a basic SFB TIA, where the output voltage of a voltage amplifier is sampled and current is fedback to the input through the feedback resistor (R_F).

The voltage amplifier can be implemented in various ways, where the simplest is a common emitter/common source (CE/CS) configuration. The choice of the voltage amplifier configuration is often dictated by the requirements for gain and noise performance. To minimise noise, a single-stage voltage amplifier can be used, provided sufficient gain is obtained. Nevertheless, this is seldom the case, especially in CMOS designs, which are limited by their voltage headroom, hence restricting the achievable gain of individual stages and a cascaded number of gain stages are usually required to boost the amplifier gain. Hence, it is difficult to ensure a sufficient phase margin and often requires extra compensation components to achieve stability. Therefore, it imposes a trade-off between the achievable noise, gain and stability.

The performance of the SFB TIA is analysed as in [122, 137] by assuming that the voltage amplifier has a finite gain equals $-A$ and a high input impedance, hence it is reasonable to assume a purely capacitive input impedance $1/j\omega C_a$. Moreover, the voltage amplifier output impedance is taken to be zero, and the bandwidth is infinite. Where C_{pd} appears to be in parallel with the voltage amplifier input capacitance so can be written as $C_T = C_{pd} + C_a$. The SFB TIA transimpedance can be expressed as:

$$A_T(s) = -R_T . \frac{1}{1 + s/\omega_p} \tag{5.1}$$

where

$$R_T = \frac{A}{A+1} R_F \tag{5.2}$$

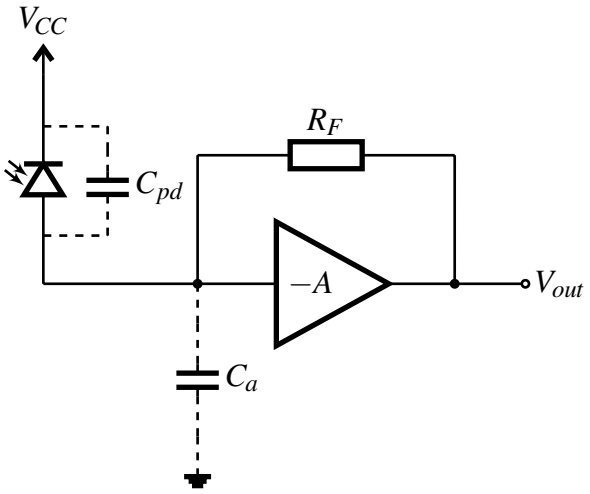


Figure 5.1: Basic shunt-feedback amplifier configuration

$$\omega_p = \frac{A+1}{R_F C_T} \tag{5.3}$$

For sufficiently large open loop gain, where $A \gg 1$ then the DC transimpedance gain is approximately equals R_F. Whereas, the bandwidth is set by the real pole ω_p given by the product of $R_{in}\, C_T$, where R_{in} is the input resistance equals $R_F/1+A$. Clearly, it can be seen from (5.3) that C_{pd} significantly limits the bandwidth of the SFB TIAs.

Furthermore, to model the behaviour of the SFB amplifier accurately, the infinite voltage amplifier bandwidth is replaced by a more realistic single pole amplifier model. The voltage amplifier can be modelled by $A(s) = A/1+s\tau_A$, where A is the voltage amplifier DC gain and τ_A is the pole time constant. The amplifier input impedance remains purely capacitive equals $1/j\omega C_a$, and the output impedance is zero. Now the closed loop response of the TIA is given by a second order transfer function with two poles, where the high frequency pole is due to the finite bandwidth of the voltage amplifier, and the low frequency pole is due to the low pass filter formed by C_T and R_F. Hence, the closed loop transimpedance gain is given by:

$$A_T(s) = \frac{R_T}{1+s/(\omega_n Q)+s^2/{\omega_n}^2} \tag{5.4}$$

where the DC transimpedace gain R_T remains same as given by (5.9), whereas, the natural frequency (ω_n) and the quality factor of the pole pair (Q) are given by:

$$\omega_n = \sqrt{\frac{A+1}{R_F C_t \tau_A}} \tag{5.5}$$

$$Q = \frac{\sqrt{(A+1)R_F C_t \tau_A}}{R_F C_t + \tau_A} \tag{5.6}$$

The low-frequency input referred noise current for the SFB TIA is given by:

$$I_{n,TIA}^2 = I_{n,R_F}^2 + \frac{v_{n,amp}^2}{R_F^2} \tag{5.7}$$

Assuming a peaking free response, which includes either a Butterworth, Bessel and critically damped designs, then $Q \leq 1/\sqrt{2}$, hence, the bandwidth of the SFB TIA is bounded by:

$$BW \leq \omega_n / 2\pi \tag{5.8}$$

Clearly, the achievable bandwidth of the SFB TIA is challenged by both the noise and transimpedance gain performance. According to (5.5) and (5.7), increasing R_F results in higher transimpedance gain and lower input-referred noise current. Since the input referred noise current is passed to the input while scaling it with R_F^2 and since R_F does not carry a large bias current, hence its value can be increased to reduce the noise. Nevertheless, such an advantage comes at the cost of reduced bandwidth. Since increasing R_F reduces the frequency of ω_n and, in turn, the TIA bandwidth. Apart from the trade-off imposed by R_F, another bandwidth-limiting factor is C_{pd}, where it is clear from (5.5) and (5.6) that the SFB TIA bandwidth and stability heavily rely on C_{pd}. Meaning, in the case where C_{pd} is high, then the open loop input pole frequency is reduced, which in turn reduces the amplifier bandwidth. Whereas, in the case of low C_{pd}, the input pole frequency is increased, which reduces the pole spacing between the input pole and the high frequency pole of the voltage amplifier, potentially compromising the amplifier stability.

These conclusions were also gathered in a study by Sackinger (2010) defining an operating limit known as the transimpedance limit for different TIA configurations, among these configurations is the SFB TIA [137]. The transimpedance limit

is a quality used to describe the maximum transimpedance that a TIA can achieve for a given bandwidth and technology. According to derivations in [137], based on the assumption of a peaking free response, while expressing R_F in terms of R_T with (5.9) and substituting into in (5.5), results in the SFB TIA transimpedance limit given by:

$$R_T \leq \frac{Af_A}{2\pi C_t BW^2} \tag{5.9}$$

where the product Af_A is the voltage amplifier gain-bandwidth product, which is roughly proportional to the technology f_T. In summary, (5.9) defines the maximum achievable DC transimpedance gain by the SFB TIA for a given 3dB-bandwidth and technology Af_A/C_t. Two key conclusions can be made: First, the transimpedance gain reduces with the square root of the bandwidth and not linearly. This is a consequence of the finite gain-bandwidth product of the voltage amplifier. Second, the trade-off between transimpedance gain and bandwidth is solely dictated by the single parameter Af_A/C_t, which is mostly dictated by C_{pd}.

This dependence of the SFB TIA bandwidth and stability on C_{pd} can be reduced by incorporating a feedback capacitor C_f in parallel with R_F, this capacitor can be in the form of a physical capacitor added to improve the amplifier stability as in [138] or the parasitic capacitance of R_F. Alternatively, a noiseless capacitive feedback can be employed, which can improve both the stability and noise performance of the TIA as proposed in [136, 139]. Furthermore, the SFB TIA can be combined with other bandwidth extension techniques such as inductive peaking as in [115, 117], to enhance the bandwidth while maintaining the noise advantage. Alternatively, a low input resistance voltage amplifier can be utilised that acts as a current buffer stage between the photodiode and the SFB voltage amplifier to isolate C_{pd} from determining the bandwidth. An illustrative example is a circuit reported by Mohan *et al.* (2000), where a CG amplifier stage preceded the SFB amplifier to decouple C_{pd} from the bandwidth determination of the SFB TIA [140].

5.4 Low Input Impedance TIAs

5.4.1 Common Base/Gate TIA Configuration

Since it is concluded that TIAs employing a low input resistance stage are less sensitive to C_{pd} therefore, it is useful to understand and analyse the key low input resistance configurations. A low input resistance TIA stage can be in the form of a traditional CB/CG configuration. The CB was first utilised as an optical preamplifier input stage in 1988 by Darwazeh *et al.*, which demonstrated a TIA with CB input stage and current SFB [118, 119]. The seminal work reported in [118, 119], inspired further work by Vansiri *et al.* in 1995 to exploit the low input resistance advantage of the CB configuration with modifications to the bias and feedback to obtain improved noise performance, while maintaining the bandwidth advantage [141]. From these reports have ensued a flow of reports on the so called "current mode" optical transimpedance preamplifier based either on the CB/CG stage [123, 140, 142–145] or modifications of the CB/CG stage [120, 121, 124, 146, 147].

First we consider the feedforward CB (open-loop) configuration, shown in Figure 5.2, by analysing the CB equivalent model, the input resistance (R_{in}) can be expressed as:

$$R_{in} = \frac{1}{g_{m1}} \tag{5.10}$$

where g_{m1} is the transconductance of transistor Q_1. To derive the feedforward CB TIA tansimpedance gain, we make some simplifying assumptions: transistor output resistance $r_o \gg R_1$, $R_s \gg 1/g_{m1}$ and $\beta \gg 1$. Hence, the CB transimpedance gain (A_T) can be presented by a transfer function composed of a real input pole ω_{p1} and a real output pole ω_{p2} as given by A_T;

$$A_T = \frac{R_T}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{5.11}$$

and

$$R_T = R_1 \tag{5.12}$$

$$\omega_{p1} = \frac{1}{R_{in}C_{pd}} \tag{5.13}$$

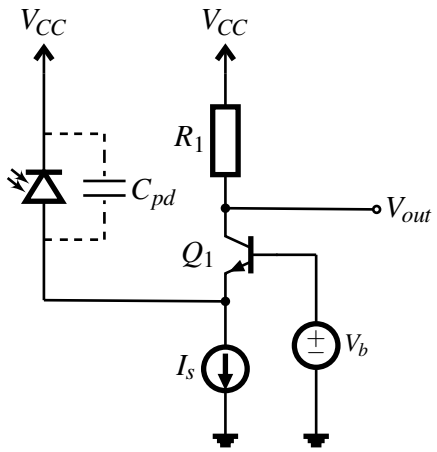


Figure 5.2: The feedforward CB transimpedance amplifier

$$\omega_{p2} = \frac{1}{R_1 C_{\mu 1}} \tag{5.14}$$

where $C_{\mu 1}$ is the base collector capacitance of Q_1. The input referred noise current can be derived as:

$$I_{n,in}^2 = \frac{4kT}{R_1} + I_{n,Is}^2 \tag{5.15}$$

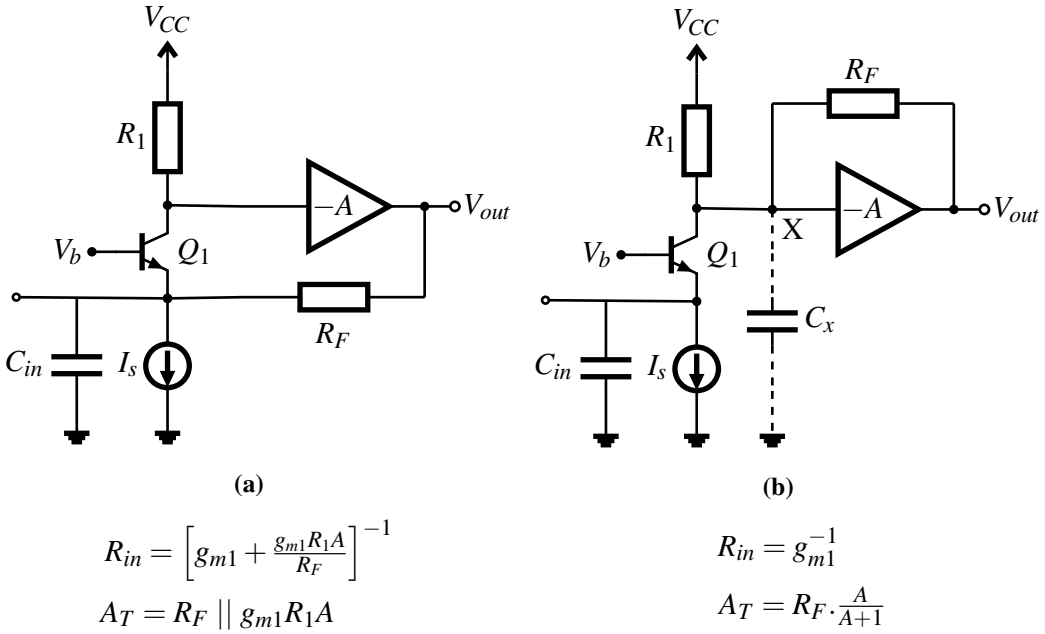
where $I_{n,Is}^2$ denotes the noise current from the current source I_s. According to (5.10), the input resistance is inversely proportional to g_{m1}. To obtain low input resistance, the bias current should be large to maximise g_{m1}. This in turn should provide better isolation of relatively large C_{pd}, alleviating its bandwidth-limting effect when compared to traditional CE and CC [148] inputs. Moreover, the photodiode current passes unattenuated through Q_1 into the collector resistor R_1, since the CB is a current buffer with unity gain. Therefore, the input AC current is then converted to AC voltage $V_{out} = I_{in} R_1$. Hence, the transimpedance gain of the CB TIA approximately equals R_1.

However, maximising g_{m1} to reduce the input resistance not only raises the current consumption but, according to (5.15), this raises the input-referred noise current from the current source I_s. Moreover, increasing g_{m1} can also have the downside of lower transimpedance gain, since it is dictated by R_1, where the maximum value is limited by the voltage headroom. Therefore, increasing the transimpedance gain

mandates employing high supply voltage to accommodate the voltage drop across R_1 to maintain the bias condition of Q_1.

Furthermore, increasing the transimpedance gain (i.e increasing R_1) also reduces the frequency of the output pole ω_{p2}, which can impose a gain bandwidth trade-off in cases where ω_{p2} is the dominant pole. The dominant pole dictating the bandwidth of the CB is generally reported to be the output pole and it is insensitive to the input pole ω_{p1} associated with C_{pd} and its input resistance [118, 119, 122]. While this is true for such cases, yet this is largely dependent on the C_{pd} value. In cases where C_{pd} is significantly high, in the range of tens to hundreds picoFarads, the dominant pole shifts to the input pole ω_{p1}. Hence, it can be inferred that there is a trade-off between bandwidth, transimpedance gain, noise and voltage headroom of CB TIAs. The feedforward CB stage can be used as a stand-alone TIA, yet there are hardly any reports adopting the CB without the use of additional feedback to alleviate the formerly described trade-offs. An example of a feedforward CB TIA, where the bandwidth is insensitive to C_{pd} is reported by Mesgari *et al.* (2020). The work demonstrates a feedforward CB TIA followed by a capacitive degeneration limiting amplifier, achieving a 27 GHz bandwidth at 49 dBΩ differential transimpedance gain at C_{pd} equals 90 fF using 130 nm SiGe process to be employed as radio over fiber transceiver for 5G remote radio head application [145]. Despite the considerable bandwidth, yet the transimpedance gain is relatively low. Such bandwidth is primarily achieved by reducing the CB transimpedance gain (reducing R_1) to ensure that the CB dominant output pole ω_{p2} dictating the bandwidth is pushed to higher frequencies. Hence, the reported receiver relies mainly on the following limiting amplifier stage to boost the gain. Moreover, it is also worth noting that the authors opt to use the CB topology in particular since it provides better stability performance especially at higher frequencies due to the absence of large number of parasitic paths with a positive phase shift as with the RGC TIA as studied in [149].

To alleviate the trade-off between bandwidth, transimpedance gain, noise and voltage headroom in the feedforward CB TIA, the use of feedback was proposed. Current shunt feedback is employed by applying a feedback resistor connected to



$$R_{in} = \left[g_{m1} + \frac{g_{m1} R_1 A}{R_F} \right]^{-1}$$

$$A_T = R_F \,||\, g_{m1} R_1 A$$

$$R_{in} = g_{m1}^{-1}$$

$$A_T = R_F \cdot \frac{A}{A+1}$$

Figure 5.3: (a) Shunt feedback TIA with CB input stage (b) CB TIA with current feedback

the input of the CB TIA as shown in Figure 5.3a. Such arrangement has the effect of both reducing the CB input resistance and increasing the transimpedance gain, yet at the cost of degraded noise performance because of the additional noise components.

The reduction in the input resistance via current shunt feedback renders an additional degree of freedom by varying the amount of feedback, hence, allowing for operation at smaller g_{m1}, while still achieving low input resistance. This in turn eases the voltage headroom limitation, making room for higher R_1 (transimpedance gain). Therefore, mitigating the trade-off between bandwidth and transimpdance gain. The current shunt feedback arrangement was first reported by Darwazeh *et al.* (1988). The work has demonstrated a TIA employing a low input impedance CB stage followed by a buffer, a voltage gain stage and an output buffer with shunt feedback resistance from the gain stage to the input of the CB stage. It was demonstrated that the CB based TIA bandwidth is insensitive to C_{pd} up to 7 pF, which is attributed to its low input resistance rendered by the combination of the CB input stage and the use of current shunt feedback [118, 119]. However, this comes at the expense of an increase in noise current spectral density in comparison to the CE

and CC configurations. In [141], the CB based TIA demonstrated in [118, 119] was modified by changing were the feedback is placed and how the CB is biased to reduce the noise spectral density, while maintaining the same bandwidth advantage. Similar circuit was also reported by Fan *et al.* (2008), the work reported a 40 G/bs receiver consisting of a AGC-TIA followed by a clock and data recovery (CDR) circuit [123]. The TIA features a low input resistance CG stage followed by a differential stage and output buffer with negative feedback from the buffer to the input of the CG stage. The work reports optimisation techniques for noise reduction while exploiting the current feedback arrangement, by raising R_1 with a factor m and reducing the bias current with the same factor to offset for the added noise sources from the additional current feedback path (amplifier and feedback resistor), hence, match the noise performance to a stand-alone CG stage.

Alternatively, the CB TIA can be combined with SFB amplifier as shown in Figure 5.3b. Here, the CB is loaded by the input impedance of the SFB amplifier, which is approximately $R_F/1+A$ at low frequencies. The value of R_1 is usually higher than that, especially at high values of open loop voltage gain A. Ideally, the expression of the transimpedance gain given in (5.9) of SFB amplifiers is not affected by the addition of the CB stage. Whereas, the input resistance remains to be $1/g_{m1}$. In contrast to the current shunt feedback arrangement in Figure 5.3a, which results in further reduction of the input resistance. Noting that if the additional input node ω_{p1}, introduced by the CB to the basic SFB arrangement is placed sufficiently high, such that it does not interfere with the SFB TIA frequency response, then the overall TIA bandwidth is dictated by the SFB TIA.

For a SFB amplifier, such arrangement circumvents the transimpedance limit encountered in (5.9). This is because C_{pd} is now isolated from the transimpedance stage by the low input resistance of the CB stage. Therefore, the total capacitance C_x at the critical node X, seen by the SFB amplifier is reduced, allowing for larger values of R_F while maintaining the same bandwidth. Alternatively, at similar transimpedance gain, the CB with SFB amplifier can achieve higher bandwidth in comparison to the basic SFB amplifier. Hence, compared to SFB TIA, C_{pd} is now

isolated from the node X making the TIA bandwidth and stability less dependent on C_{pd}. Compared to a feedforward CB, the small noisy resistor R_1 is replaced by a larger and quieter feedback resistor R_F. Moreover, to some extent it relaxes the trade-off between the CB transimpedance gain and bandwidth, since the transimpedance gain is now mainly dictated by the SFB TIA stage. The main drawback of such arrangement is the poor noise performance in comparison to a stand-alone SFB amplifier, mainly due to the added noise sources by the CB stage and the commensurate increase in power consumption. Whereas, in comparison to the current shunt feedback arrangement in Figure 5.3a, this arrangement fails to match the reduction in input resistance rendered by the latter. Hence, the current shunt feedback arrangement would have superior performance in terms of the achievable bandwidth. An example of this arrangement is reported by Mohan *et al.* (2000) and Park *et al.* (2003) [140, 142]. Work in [140] featured a fully differential TIA that utilising a CG input stage followed by a SFB amplifier, achieving a 1.6 kΩ and 1.2 GHz at C_{pd} equals 0.6 pF. The bandwidth is realised due to the adoption of the CG in addition to shunt inductive peaking. Whereas, [142] reports four-channel photoreceiver array each channel achieving an overall a 3.2 kΩ and 4 GHz at C_{pd} equals 0.25 pF. Each channel featuring a TIA consisting of a CB stage followed by a buffer and SFB amplifier.

The feedforward CB TIA shown in Figure 5.2 is single-ended. In many applications, a differential TIA with its superior noise immunity against common mode noise is desirable. To this end, a fully differential CB consisting of two matched but single-ended CB can be used as shown in Figure 5.4a. An example of this approach is reported in [140, 143–145]. Work reported by Stavros *et al.* (2017), demonstrates a fully differential CB stage in 130 nm SiGe process that achieves a bandwidth of 45 GHz at 56 dBΩ transimpedance gain, the design has utilised a fully differential arrangement to minimise the common mode noise [144].

Another way of providing differential output is shown in Figure 5.4b by employing a combination of a CB stage accompanied by CE stage or equivalently CG-CS stages as reported in [150–154]. In such case, in order for the outputs to

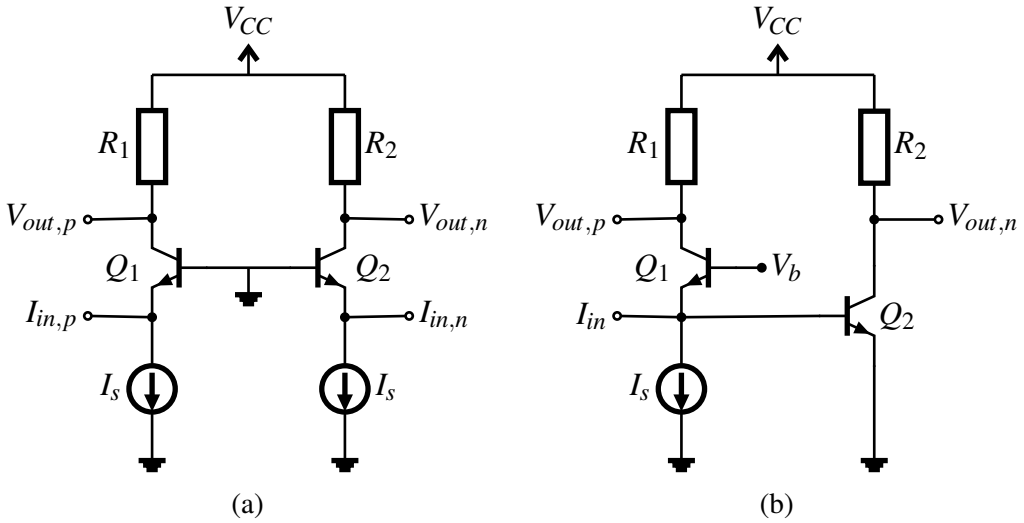


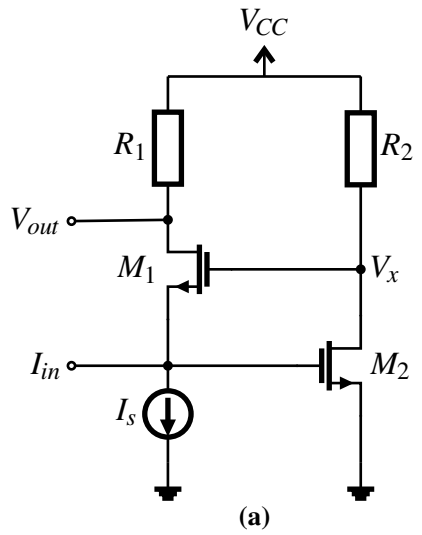
Figure 5.4: (a) Feedforward CB TIA with differential input and differential output (b) Feedforward CB TIA with single-ended input and differential output

be matched then $R_1 = g_{m1}/g_{m2}.R_2$ has to be satisfied. This arrangement is reported by Blaakmeer *et al.* (2008), yet with admittance scaling of the CS stage and replica biasing to achieve balanced output operation while simultaneously cancelling the CG stage noise and distortion [150]. Whereas work reported by Kalogerakis *et al.* (2013) and Sang *et al.* exploits the enhanced noise performance of the CG-CS configuration, yet the CE stage is replaced with a cascode stage to provide improved frequency behaviour by ameliorating the Miller capacitance encountered in CE stages [151, 152]. Work reported by Mesgari *et al.* (2018) builds on the CG-CS configuration reported in [150] to provide single to differential output yet with an additional modification to the input impedance path to reduce the input resistance [153]. The modification is based on the addition of an inverting amplifier following the CS stage, where the output of the CS stage is fed to the input of the additional amplifier. The amplifier output is then fed to the input of the CG. This feedback mechanism results in a significant reduction in the input resistance of the CG-CS TIA by a factor equals the gain product of the CS and the additional inverting amplifier stage. A different feedback mechanism is applied to the CG-CS arrangement in work reported by Firouz *et al.* (2021), where local feedback is applied to each of the CG and CS stages independently [154]. In the case of the CG stage, the local

feedback contributes in the reduction of the TIA input resistance, whereas, for the CS stage, the local feedback grants noise cancellation of the CS stage.

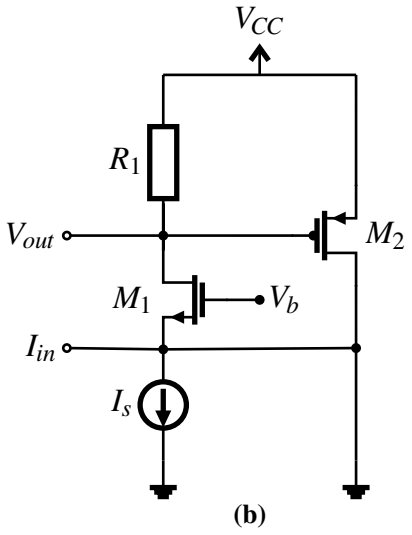
Having established some of the merits and shortcomings of the CB/CG TIA in terms of bandwidth, transimpedance gain, power consumption and noise, another important aspect is stability. While the CB has two poles that are real, so the amplifier is stable for any values of the photodiode capacitance. Hence, the CB TIA guarantees stability overall values of C_{pd} in comparison to other input impedance reduction configurations such as the RGC, owing to its real poles. However, other potential causes of instability could arise due to the inductive nature of its input impedance caused by the non-zero base resistance of the transistors. An inductive input can potentially speed up the TIA, yet could cause significantly large peaking, which could degrade its stability [119, 155]. Work reported by Green *et al.* (2013) presents a thorough study on the stability of CB amplifiers, detailing the necessary conditions to achieve a stable operation and outlining methods to improve stability in terms of both the optimum design parameters and layout techniques [155].

In contrast to TIAs employing CB input stage, circuits based on FETs, featuring CG come short in matching the performance of CB TIAs optical front-ends. Analysis in [122] explains that there is a preference of the CB input stages over CG, the reason for this is that the BJT achieves significantly higher g_m in comparison to FETs for a given bias current. Where, for a BJT $g_m \approx I_C/V_T$, at which I_C is the collector current and V_T is the thermal voltage approximately equals 25 mA , and for FET $g_m = 2I_D/(V_{GS} - V_{th})$, where I_D is the drain current and $(V_{GS} - V_{th})$ is the overdrive voltage with typical values of 0.3 V. Hence, the BJT g_m is approximately six times higher than FETs for the same bias current. Therefore, for a FET to achieve the same g_m, it would require six times the bias current which in most cases would not be supported by the transistor or would significantly increase the noise as well as the power consumption. To boost g_m of the CG input stage, numerous novel circuit modifications based on g_m-boosting techniques of the traditional CG stage were reported. Hence, alleviating the stringent trade-off between the achievable transimpedance gain, bandwidth and power consumption [78, 121, 124, 147, 153, 154].



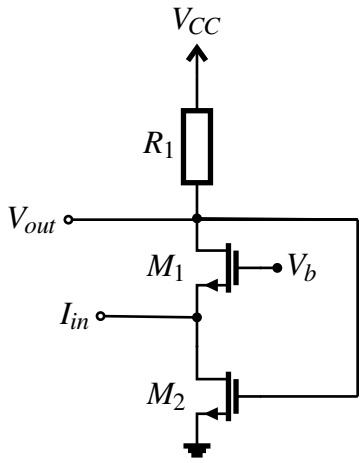
(a)

$$R_{in} = [g_{m1}(1+g_{m2}R_2)]^{-1}$$
$$A_T = R_1$$



(b)

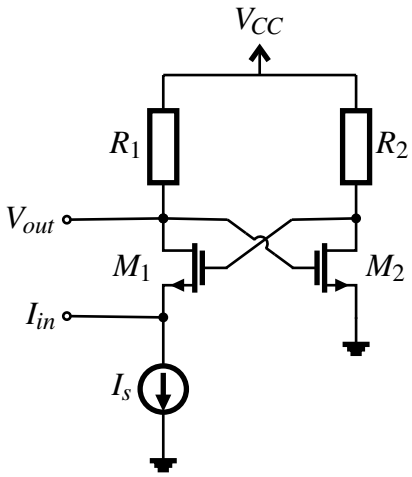
$$R_{in} = [g_{m1}(1+g_{m2}R_1)]^{-1}$$
$$A_T = R_1 \,||\, g_{m2}^{-1}$$



(c)

$$R_{in} = [g_{m1}(1+g_{m2}R_1)]^{-1}$$
$$A_T = R_1/(1+g_{m2}R_1)$$

(a)



(d)

$$R_{in} = [g_{m1} - g_{m2}R_1R_2]^{-1}$$
$$A_T = R_1$$

(b)

Figure 5.5: a) RGC TIA (b) CG TIA with active feedback (c) CG TIA with direct feedback (d) cross-coupled CG TIA

Some of these circuits are presented in Figure 5.5.

The first report of a circuit based modification to boost g_m of the traditional

CG, known as the RGC, was reported by Park *et al.* (2000) in [120, 121]. Figure 5.5a, shows the reported RGC TIA input stage, in this circuit the g_m-boosting of the CG is achieved by means of an auxiliary amplifier based on a CS stage acting as booster amplifier resulting in a significant reduction in the input resistance by a factor equals $A_{v2}+1$ where A_{v2} is the CS voltage gain and hence, providing high amplifier bandwidth. Whereas the transimpedance gain is still determined by the collector resistor R_1. Hence, the RGC configuration provides a significant reduction in input resistance without affecting the transimpedance gain of the traditional CG stage. The reported TIA consisted of a RGC input stage followed by a voltage amplifier to achieve further gain, using 0.6 μm CMOS process. However, the voltage amplifier limited the bandwidth of the RGC TIA; therefore, negative feedback from the output buffer to the input of the voltage amplifier was incorporated to shift the dominant pole resulting from the voltage amplifier to a higher frequency. The TIA offered bandwidth of 300 MHz at 57.7 dBΩ, which is a 120% improvement over the CG counterpart at a similar transimpedance gain yet, improved noise performance. The bandwidth enhancement is attributed to the significant reduction in the input resistance from 250 Ω in the CG case to 50 Ω in the RGC case.

One of the main motivations of the RGC configuration is to boost the g_m of the CG input stage, hence, reducing the input impedance without the need to increase the bias current significantly. Yet by inspecting Figure 5.5a, it can be seen that the voltage at node V_x is equal the sum of the gate-source voltages of transistors M_1 and M_2. This limitation does not permit increase in M_1 current (g_{m1}) and the R_1 value. Therefore, the input resistance can not be reduced considerably at low voltage design. In addition to, placing a limit on the achievable transimpedance gain. Such limitations were studied and treated in multiple derivatives of the conventional RGC as in [156–158]. More detailed explanations of these designs are presented in the following section.

Another variety of the CG employing g_m-boosting technique based on active feedback is reported by Zhenghao *et al.* (2010) in [124]. The active feedback is implemented by means of a PMOS stage M_2 as shown in Figure 5.5b. The TIA offered

bandwidth of 7 GHz at 54.6 dBΩ with C_{pd} equals 0.3 pF, using 0.18 μm CMOS process. Although, this arrangement succeeds in reducing the input resistance of the traditional CG yet its benefits are questionable in comparison to the conventional RGC circuit. First, the reduction in the input resistance of the CG is by the gain of the PMOS transistor M_2, such reduction is not as much as the reduction achieved by the NMOS CS amplifier in the RGC circuit, because the transconductance of PMOS is lower than the NMOS counterpart. Moreover, to achieve low input resistance and high transimpedance gain, it is imperative to minimise the value of g_{m2} and maximise the value of R_1. This is because, in contrast to the RGC, the input resistance becomes a function of the resistor R_1, which also dictates the transimpedance gain. Moreover, the transimpedance gain is not determined by just R_1 but by the parallel combination of R_1 and $1/g_{m2}$. The dependencies introduced by this arrangement could be problematic, especially in low power consumption designs, since it imposes a more acute trade-off between bandwidth and gain. This implied that attempting to minimise g_{m2} to avoid a reduction in the transimpedance gain will, in turn, lead to an increase in the input resistance. Alternatively, increasing R_1 to both increase the transimpedance gain and counteract the increase the input resistance resulting from minimising g_{m2} is still constrained by the voltage headroom limitation.

Similarly, the g_m-boosting technique of the CG TIA by the feedback arrangement shown in Figure 5.5c suffers from the aforementioned dependency of both the transimpedance gain and input resistance on R_1 and g_{m2} as seen in Figure 5.5b. It is manifested that such dependency inflicts a severe compromise between bandwidth and transimpedance gain. This arrangement was proposed by Abdollahi *et al.* (2015) to relax the voltage headroom limitation encountered in conventional RGC, since it increases the available DC headroom at node V_x [147]. Furthermore, the input resistance is reduced by utilising the concept of current reuse, which is based on using g_m from the tail current source, normally used for only biasing to provide negative feedback. Hence, enhancing the bandwidth with no additional cost in terms of current consumption and noise performance. This configuration was also utilised by Samart *et al.* (2018), reporting a fully differential arrangement in the

application of positron emission tomography (PET) scanning, the modified CG is interfaced with a silicon photomultiplier (SiPM) array, achieving a bandwidth of 150 MHz at an input resistance of 14 Ω [159]. In the application of PET scanning, the low input resistance is desirable to prevent current sharing and bandwidth extension. In comparison to [124], this arrangement achieves similar input resistance to the RGC, since the feedback is achieved using an NMOS transistor M_2 instead of a PMOS transistor. Yet again, the transimpedance gain becomes a function of g_{m2}, which can potentially limit the achievable bandwidth. Work reported by Roya *et al.* (2016) utilises the same configuration, yet in a differential arrangement with the combination of capacitive cross-coupling between the CG differential pair, the use capacitive cross-coupling CG pair doubles g_{m1} in comparison to [147], so that the input resistance becomes $[2g_{m1} + g_{m2}R_1]^{-1}$, while also benefiting from the enhanced noise immunity offered by a differential arrangement [160].

Another g_m-boosting technique of the CG stage is based on a cross-coupled transistor arrangement, also known as immittance converter as shown in Figure 5.5d. This configuration was utilised as a single-ended low input resistance TIA by Taghvani *et al.* (2015) and in differential arrangement by Chen *et al.* (2013) [78, 132, 146]. Such arrangement dramatically reduces the input resistance by employing feedback implemented by M_2 and R_2 to be set almost to zero. This is evident by inspecting the expression of R_{in}; the presence of the negative term allows for almost zero input resistance. Hence, this breaks the trade-off between achieving low input resistance and power consumption encountered in previous designs. Despite having the desirable input resistance to achieve wide-band performance, yet this configuration can exhibit unsatisfactory stability performance. As explained in [161], the input impedance of the immittance converter circuit can be mimicked by a combination of series resistance and a negative inductance ($R_{in} - L_{in}$). Where L_{in} is a function of the resistor R_1 (i.e transimpedance gain). Therefore, if $R_{in} \approx 0$, then the circuit input impedance is now formed by a lossless resonant network consisting of the input negative inductance in parallel with C_{pd}. Hence, to avoid oscillations, then L_{in} should be designed to be small, which suggest small R_1. Hence, imposing

a trade-off between transimpedance gain and stability.

Based on the above discussion, it becomes clear that out of all the CG TIA modifications presented, the RGC offers the best balance of all key parameters in terms of bandwidth, gain and stability. Therefore, the following section, presents more details about the basic concept of the RGC, together with some interesting derivatives of the conventional RGC TIA that treat some of its inherent limitations.

5.4.2 Regulated Cascode TIA Configuration

The RGC configuration was first reported by Sackinger as a superior alternative to the simple cascode that features higher output impedance yet is not limited by the usable output voltage swing as with the simple cascode [162]. Sackinger demonstrated that the RGC offers improved output impedance and enlarged output voltage swing in comparison to the simple cascode, which endorse the RGC to be used in the design of different analogue building blocks such as current mirrors. Another signature feature of the RGC is its extremely low input resistance, which is advantageous in the application of front-end optical pre-amplifiers with high capacitive inputs. As mentioned earlier, work in [120] and [121] are the first to exploit the low input impedance characteristic of the RGC to employ it as the input stage of optical receiver pre-amplifiers. An extension of the work in [120, 121] was later reported in [21], presenting a TIA using a 0.6 μm CMOS process, the TIA exploited the RGC as an input stage, thus achieving a large effective g_m, as that of the BJTs. For further gain, the RGC was followed with a shunt feedback voltage amplifier, where the feedback was applied to the voltage amplifier and not the RGC input, since the dominant pole dictating the TIA bandwidth is a result of the voltage amplifier. The TIA offered a bandwidth of 950 MHz at 58 dB with C_{pd} equals 0.5 pF.

Following the proposal of the RGC TIA, a myriad of reports studying and utilising the RGC circuit as a high-speed TIA itself or as an input stage to a SFB amplifier. Some of which also aimed to improve its performance even further by addressing some inherent RGC limitations of the RGC, such as the voltage headroom limitation [156, 157] and stability [149] or by proposing RGC varieties that improve the frequency behaviour even further [161, 163–165].

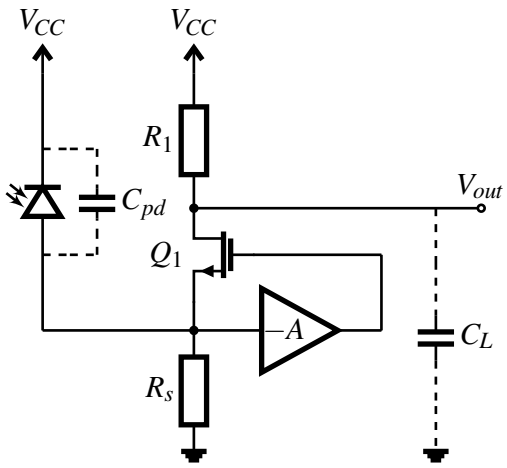


Figure 5.6: Block diagram of the RGC TIA

First we consider the conventional RGC configuration. Study by Sackinger (2018) describes the RGC as a CG stage with a local feedback booster amplifier as shown in Figure 5.6 [122]. The role of the booster amplifier is to sense any voltage changes at the CG input node and control its gate voltage to counteract it. Hence, the resulting input resistance is reduced by a factor equals $(1+A_o)$ in comparison to the CG stage. Where, A_o is the DC voltage gain of the booster amplifier. Therefore, the RGC input resistance is given by:

$$R_{in} = \frac{1}{g_{m1}(1+A_o)} \tag{5.16}$$

The booster amplifier can be implemented by a CS stage as originally proposed in [120, 121] or possibly using either a cascode or an inverter stage as in [163, 166, 167]. Sackinger showed that the booster amplifier can be modelled as having a single pole $A(s) = A_o/(1+sT_A)$, infinite input resistance, and zero output resistance. Hence, with the simplifying assumptions of $R_s = \infty$, the substrate transconductance $g_{mb1} = 0$, output conductance $g_{o1} = 0$ and the gate drain capacitance $C_{gd} = 0$, the transimpedance gain A_T of the RGC can be expressed by:

$$A_T = R_T \frac{1+s/\omega_z}{[1+s/\omega_n Q + s^2/\omega_n^2][1+\omega_{p3}]} \tag{5.17}$$

where

$$R_T = R_1 \tag{5.18}$$

$$\omega_z = \frac{A_o + 1}{T_A} \tag{5.19}$$

$$\omega_n = \sqrt{\frac{(A_o + 1) g_{m1}}{C_T T_A}} \tag{5.20}$$

$$Q = \frac{\sqrt{(1 + A_o) C_T g_{m1} T_A}}{C_T + A_o C_M + g_{m1} T_A} \tag{5.21}$$

$$\omega_{p3} = \frac{1}{R_1 C_L} \tag{5.22}$$

where C_L is the load capacitance at the output node and C_T is the total capacitance at the input node equals $C_{pd} + C_I + C_M$, where C_I is the input capacitance of the booster amplifier and C_M is the sum of the gate-source capacitance C_{gs1} and other parallel capacitance such as C_{gdB}. Clearly, the expression for the DC transimpedance gain and the real output pole ω_{p3} are the same as with the CB/CG TIA. Yet, the real input pole is replaced by a complex pole $\omega_{p(1,2)}$ defined by ω_n and quality factor of the complex pole (Q) and a zero ω_z. To elucidate, the fairly complex equation in (5.17), Sackinger makes the simplifying assumptions that $C_M = 0$ and $T_A = 0$, hence, ω_n and Q will go to infinity, leaving single real input pole $\omega_n Q = (A_o + 1).g_{m1}/C_T$. This is equivalent to the real input pole of the basic CB/CG given in (5.13), yet scaled with a factor $(A_o + 1)$. Hence, the booster amplifier increases the transconductance of the input FET and thus the frequency of the input pole by $(A_o + 1)$.

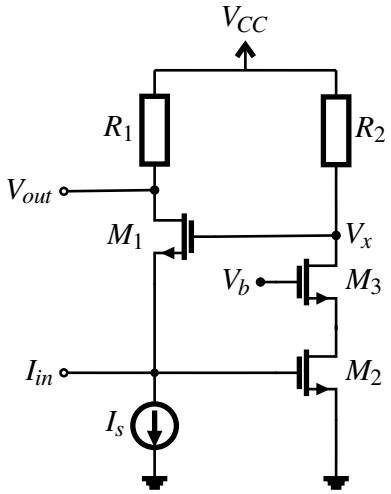
Sackinger explains that the presence of ω_z and $\omega_{(1,2)}$ could potentially result in peaked frequency response or even instability. From (5.19), it is clear that $\omega_z > A_o/T_A$, hence, ω_z frequency is larger than the gain-bandwidth product $A_o f_A$ of the booster amplifier. Being located at such a high frequency, ω_z has negligible influence on the frequency response. On the other hand, a large value for Q is of higher concern, since it can reduce the amplifier phase margin, potentially leading to instability. A lower value of Q can be obtained by reducing A_o and simultaneously increasing f_A, thus keeping the gain-bandwidth product fixed; this modification reduces the feedback loop gain, hence improving the phase margin.

The analysis provided by Sackinger gives a good overall understanding of the RGC behaviour. Yet, the assumption of $C_{gd1} = 0$ limits the accuracy of the RGC modelling for the sake of simpler equations. This assumption would have been fairly reasonable in the case of the CG stage, since the gate of Q_1 would have been grounded, and it has only one input feed, which is the source. Nevertheless, for the RGC, Q_1 has two input feeds, where most of the signal is fed to the source of Q_1 and a small part is fed to the gate of Q_1 through the booster amplifier, which, what provides the regulation mechanism. In this feedback path, the signal flowing into the gate of Q_1, sees Q_1 as a CS, hence, experiencing the capacitance C_{gd1} as a Miller capacitance at both the drain of Q_1 and more significantly at the gate. Such capacitance is a function of both the TIA transimpedance gain and Q_1 voltage gain. Such observation about the RGC behaviour seems counter-intuitive, yet it will become evident in Chapter 6 that such capacitance C_{gd1}, besides C_{pd}, is a major contributor in determining the value of both ω_n and Q. Hence, dictating both the bandwidth and stability of the RGC. Such capacitance was utilised by Bashiri *et al.*, where an RGC TIA is reported yet with the addition of an inductor added in the feedback, which is designed to resonate with the Miller capacitance of C_{gd1} to increase the bandwidth of the TIA [168].

In general, careful optimisation of the RGC design parameters is necessary to ensure stability. Abdollahi *et al.* (2017) studies the stability and bandwidth compromise associated with a low voltage RGC derivative employing a level shifter configuration [149], originally proposed in [156]. The RGC employs a level shifter to alleviate the voltage headroom problem. In this work, the criterion for a well behaved time and frequency response of the low voltage RGC design has been derived, where it is suggested that increasing the RGC g_m to obtain higher bandwidth may compromise the amplifier stability and results in ringing in the time response. Moreover, a compensating technique that employs some passive components (a capacitor in series with a resistor) between the gate and drain of the RGC CS stage is proposed that results in reduced frequency response peaking and at the same time allow for the g_m to be increased to obtain higher bandwidth.

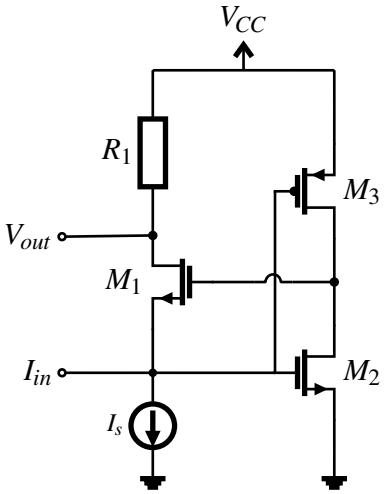
Other reports treating the RGC voltage headroom limitation was proposed in [157] and [158]. Work in [157], demonstrates a single to differential output low power TIA that achieves a bandwidth of 26 GHz at 53 dB single-ended transimpedance gain with C_{pd} equals 150 fF, the amplifier is based on a modified RGC-based transformer configuration. In the transformer-based RGC, the reduction in the RGC input impedance via feedback is achieved by an inverting transformer instead of a CE/CS stage. The advantage of this configuration lies in alleviating the voltage headroom requirement of the conventional RGC design. In other words, the headroom of conventional RGC has to be at least two gate-source voltages to accommodate for the CB and the feedback CE stage, this requirement leads to relatively high power consumption. However, this configuration treats this limitation by eliminating the CE stage. Alternatively, in [158] the voltage headroom problem associated with RGC is treated by inserting an intermediate PMOS source follower stage between the CG and the CS of the RGC, which was termed as source follower based RGC. The additional PMOS source follower stage has two advantages: first, it lowers the DC output voltage, and second, it acts as additional isolation from C_{pd}. This work also employed a shunt feedback resistor between the gate and the drain of the CG of RGC stage to construct a Cherry-Hooper like-structure to achieve a bandwidth of 7.7 GHz and 60 dB single-ended transimpedance gain with C_{pd} equals 300 fF.

More importantly to the scope of this work, other reports of the RGC TIA were concerned with improving its frequency behaviour even further. This was mainly achieved by modifications of the booster amplifier based on the CS stage so that it is replaced by either a cascode stage or with an inverter stage as shown in Figures 5.7a and 5.7b, respectively. Such modifications have the advantage of enhancing g_m of the booster amplifier with the additional transistor (M_s) so that the input resistance of the RGC is reduced further. Therefore, the voltage of gain of booster amplifier will be increased to $A_{cas} = g_{m2}g_{m3}r_{o2}r_{o3}||R_2$ and $A_{inv} = (g_{m,n2} + g_{m,p3}).r_{ds,n2}||r_{ds,p3}$ in the case of the cascode/inverter RGC TIA, respectively. Other than increasing g_m, another intuitive advantage of replacing the CS stage with a cascode stage is to



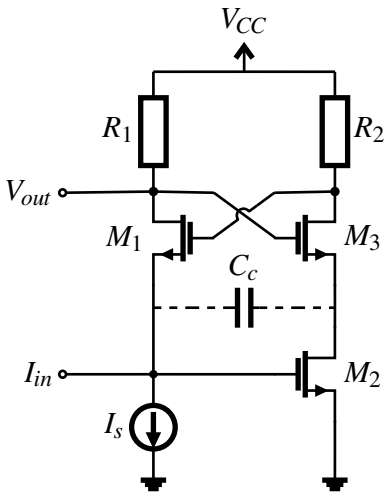
(a)

$$R_{in} = [g_{m1}(1 + g_{m2}g_{m3}r_{o2}r_{o3}||R_2)]^{-1}$$
$$A_T = R_1$$



(c)

$$R_{in} = [g_{m1}(1 + A_{inv})]^{-1}$$
$$A_T = R_1$$



(b)

$$R_{in} = [g_{m2}(g_{m1}R_1 - R_2/r_{o3})]^{-1}$$
$$A_T = R_1$$

Figure 5.7: (a) RGC TIA with auxiliary cascode feedback stage (b) RGC with inverter auxiliary amplifier stage (c) RGC with cross coupled pair feedback stage

ameliorate the Miller effect of the bandwidth-limiting gate-drain capacitance of the CS (M_2) stage. An example of the RGC with a cascode feedback arrangement is reported in [163, 164, 169]. Work in [163, 164] reports TIAs featuring RGC with a

cascode feedback arrangement, while work in [169] utilises a similar arrangement combined with the use of inductors to achieve peaking. The aforementioned reports emphasise the advantage of using the cascode stage to enhance g_m of the booster amplifier of the conventional. Another interesting observation deduced based on work by [163], the dominant pole of the conventional RGC with the CS stage is given by $(1+g_{m1}/g_{m2})(C_{gd2}+C_{gs1})$, where it is clear that the C_{gd2} of the CS does not multiply by the conventional Miller multiplier, which equals $(1+g_{m2}R_2)$, but by $(1+g_{m1}/g_{m2})$ factors so for example if $g_{m1}=g_{m2}$ then the sum of $C_{gd2}+C_{gs1}$ multiples by two. Furthermore, it is stated that adding a cascode stage would eliminate the g_{m1}/g_{m2} factor. This equation for the RGC dominant pole is originally based on analysis derived by Mohammadreza (2006) in [170]. This is mainly because such capacitance (C_{gd2}) is part of the feedback loop of the RGC, hence, in such case the Miller effect does not apply. According to analysis by Moura in [171], the Miller effect only applies in cases where the open loop gain is equal to the closed loop gain. Hence, the bandwidth-limiting effect of C_{gd2} within the RGC configuration is significantly lower in comparison to a traditional CS stage. Hence, based on analysis in [163, 170, 171], it can be deduced that the Miller effect does not apply to the CS stage of the RGC, where the gate drain capacitance does not multiply by the CS gain. Hence, the impact of such capacitance on the RGC bandwidth is minimal.

Work in [163] demonstrates a differential input-output stage based on the modified RGC and a buffer stage employing active feedback to achieve 4.5 GHz bandwidth at 64.8 dB with C_{pd} equals 0.2 pF. Although, the addition of the cascode stage instead of the CS improves the frequency behaviour of the RGC, yet it aggravates the inherent voltage headroom limitation of the conventional RGC even further. Another modification of the RGC is reported by Atef *et al.* (2015), at which the CS amplifier is replaced with a cascode inverter stage for gain boosting [166, 167]. Hence, achieving the performance of the conventional RGC TIA but with 30% reduction in the power consumption. The cascode inverter is a modification of the conventional inverter structure that provides higher output impedance. The inverter based RGC addresses the problem encountered with the conventional

RGC TIA, where the CS stage suffers from limited gain due to the limited supply voltage. Hence, the use of the inverter stage compensates for this gain reduction by enhancing both the output resistance and effective g_m of the booster amplifier so that the inverter gain is $A_{inv} = (g_{m,n2} + g_{m,p3}).r_{ds,n2}||r_{ds,p3}$. Work reported by Sheng *et al.* (2017) reports an inverter based RGC TIA with an additional CS feedback stage, where the additional CS input is fed from the gate of M_1 and its output feeds the source of M_1 (input) [172]. Hence, this arrangement achieves a dual feedback configuration for bandwidth enhancement, which results in further reduction of the conventional of the input resistance of the RGC as a result of the use of a combination of the inverter stage and the additional negative feedback from the extra CS stage.

Whereas work reported by Belostotski *et al.* (2012) and Taghavi *et al.* (2015) builds on the use of immitance converters as TIA input stage, yet combined with the RGC configuration as shown in Figure 5.7c [161, 165]. Recalling, from Section 5.4.1 discussing design derivative of the CG stage, the immitance converter stage exhibits a theoretically almost zero input impedance due to the presence of the negative term in its input impedance expression as illustrated in Figure 5.5d. Nevertheless, the stability of such an arrangement is of major concern. Thereby, Taghavi states that combining the immittance converter with the RGC can improve the TIA stability while maintaining the desirable input impedance characteristics. In [161], the immittance converter is configured either as a negative impedance converter that generates an active negative capacitance or as a positive impedance converter to generate positive inductance. In both cases, this configuration mitigates the effect of the large C_{pd}. On the other hand, work reported by Kari *et al.* (2020) utilises the cross-coupled input stage of the modified-RGC TIA as a negative capacitance converter without employing any additional active circuit, yet by only using an additional compensation capacitor C_c between the emitter nodes of M_1 and M_3 [84]. This C_c appears as a negative shunt capacitance in parallel with any load capacitor at the output at the collector of M_1, hence, offsetting the load capacitance and pushing the output pole to a higher frequency.

Table 5.2: Performance comparison for various low input impedance TIA configurations

Topology	R_{in}	A_T
CB/CG	g_{m1}^{-1}	R_1
RGC	$[g_{m1}(1+g_{m2}R_2)]^{-1}$	R_1
CG- PMOS active feedback	$[g_{m1}(1+g_{m2}R_1)]^{-1}$	$R_1 \| \| g_{m2}^{-1}$
CG-tail feedback	$[g_{m1}(1+g_{m2}R_1)]^{-1}$	$R_1/(1+g_{m2}R_1)$
Cross coupled pair	$[g_{m1}-g_{m2}R_1R_2]^{-1}$	R_1
Inverter-RGC	$[g_{m1}(1+A_{inv})]^{-1}$	R_1
Cross coupled toplogy RGC	$[g_{m2}(g_{m1}R_1-R_2/r_{o3})]^{-1}$	R_1

Table. 5.2 presents a performance summary of the different TIAs configurations discussed earlier. All of the aforementioned reports have largely achieved high gain and wide bandwidth operation. Although the techniques employed are interesting and applicable in the context of our study yet, the capacitances of the photodiodes in these reports are in the femtoFarad range, which is far less than the capacitances encountered in VLC. Therefore, it is important to independently study the performance of the RGC with large C_{pd} (hundreds of picoFarad range).

5.5 Discussion & Conclusions

The key specification requirements of a typical TIA are high bandwidth, high transimpedance gain, low noise and low power consumption; such specifications are often challenging and conflicting to achieve. Among these parameters, a large bandwidth is critical to achieving broadband data transmission. The major limitation on the bandwidth of conventional TIAs is usually due to the input node introduced by the large capacitive load associated with the preceding large-area photodiode.

The challenge imposed by large C_{pd} on the design of TIAs is particularly problematic in the VLC systems. Since using exceptionally large-area photodiodes are inevitable to the application of such systems, hence, bringing large C_{pd} (range in the 100s of pF). Techniques for TIA bandwidth enhancement are reported constantly; nevertheless, mostly designed at a fixed C_{pd} that is significantly low (femtoFarad range). In contrast to the scope of this work, where studying the TIA behaviour with a variety of ultra-high C_{pd} is necessary to optimise performance in terms of bandwidth, transimpedance gain and stability. The vast majority of reports tackling the bandwidth limitation associated with large C_{pd} used low input resistance stages featuring a CB/CG and RGC input stages, which establishes the suitability of low input resistance configurations to deal with high C_{pd}.

An obvious theme from the literature review is that most reports based on CMOS TIAs aim to boost the effective g_m of FETs transistors using design modifications of the CG and the RGC, without increasing the current consumption. The main drive for such modifications is to abide by the limitations imposed by the CMOS process in terms of voltage headroom, which results in a limited gain. While the use of such techniques successfully boosts g_m of these designs, yet in some cases, it gives rise to too many conflicting parameters.

A particular topology that has been identified from this review, for its remarkable utility in designing low input impedance TIAs with ultra-wide bandwidth performance, is the RGC TIA. Since, it achieves a good balance of all key TIA parameters. Nevertheless, due to the significance of boosting g_m to achieve low input resistance, which is to some extent limited in the conventional RGC design due to

its inherent voltage headroom limitation, the use of BJTs instead of FETs seems more favourable in the application of VLC. Since, sufficient g_m can be achieved in the RGC BJT implementation without having to resort to additional modifications of the RGC to achieve g_m-boosting.

Since most of the RGC reports are based on the use of very small C_{pd}, there is a lack of sufficient study on the RGC behaviour with ultra-high C_{pd}. Furthermore, due to the nature of the RGC incorporating feedback, it is necessary to conduct detailed studies of the RGC behaviour, especially in the presence of high C_{pd} to avoid any potential instability and to optimise the bandwidth performance.

From the preceding discussion, it can be inferred that the use of BJTs is more suitable in dealing with large C_{pd}. Moreover, an independent study of the RGC behaviour in the presence of large C_{pd} is essential. In the latter chapters, efforts to study the behaviour of the RGC with large C_{pd} and to treat its inherent bandwidth limitations are presented. Modifications of the conventional RGC, with the intent of optimising its utility, particularly in terms of transimpedance gain and bandwidth performance in the application of VLC systems.

Chapter 6

A New High Bandwidth Modified Regulated Cascode Amplifier

6.1 Introduction

This chapter describes the design of the low input impedance RGC TIA with ultra-high photodiode capacitance C_{pd}. Analysis of the RGC at high C_{pd} showed that the complex nature of its dominant input pole necessitates careful design optimisation to achieve optimal bandwidth performance. Furthermore, mathematical and analytical studies of the RGC led to the identification of internal Miller capacitance presented by $C_{\mu 1}$ of the CB stage as a major limitation on bandwidth and transimpedance gain. Therefore, a modification of the RGC is proposed to eliminate the undesirable Miller capacitance effect. Mathematical analysis and full circuit simulations showed, that by introducing a cascode stage, substantial improvement in bandwidth and transimpedance gain are realised. Moreover, the newly proposed modified RGC has a key advantage in that its bandwidth is almost independent of transimpedance gain. The performance of the two TIAs is experimentally verified through measurements of the scattering parameters of two circuits constructed using discrete components on two PCBs. Experimental results show the advantage of the new design where the bandwidth is nearly doubled relative to the traditional RGC. Work in this chapter includes results presented in two conference papers [1].

[1] A.Kassem and I.Darwazeh, "A High Bandwidth Modified Regulated Cascode TIA for High Capacitance Photodiodes in VLC," IEEE International Symposium on Circuits and Systems (ISCAS), 2019
A.Kassem and I.Darwazeh, "Practical Demonstration of RGC and Modified RGC TIAs for VLC systems," IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2021

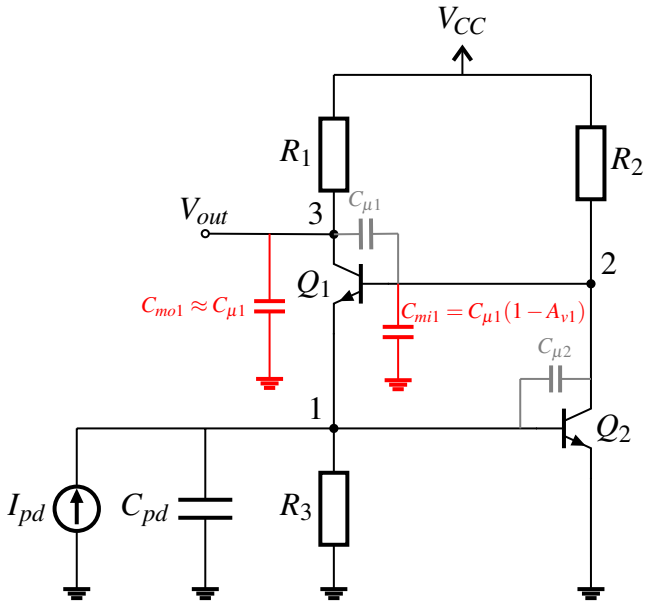


Figure 6.1: The conventional RGC TIA with photodiode input

As discussed in Chapter 5, some of the RGC modifications replace the CS/CE stage with a cascode to increase g_m of the booster amplifier, hence extending the RGC bandwidth by reducing its input resistance even further. In addition to improving the RGC frequency behaviour by eliminating the Miller effect associated with the C_μ of the CE stage. Nevertheless, this is not the only frequency limiting Miller capacitance encountered in the RGC configuration. Interestingly, when inspecting the signal flow Figure 6.1, it becomes clear (although counter-intuitive) that through the feedback path, the signal flowing from the collector of Q_2 into the base of Q_1, sees Q_1 as a CE instead of a CB stage, since Q_2 feeds the base of Q_1, which in turn outputs an amplified voltage signal at its collector. Hence, the feedback signal at the base of Q_1, experiences its $C_{\mu 1}$ as a Miller capacitance at the collector of Q_1 as C_{mo}, and more significantly at the base of Q_1 as C_{mi}.

In studies of the performance of the RGC TIA as in [122], the effect of $C_{\mu 1}$ is often omitted to simplify the analysis, since it is believed that $C_{\mu 1}$ has minimal effect on the RGC bandwidth performance. Nevertheless, such capacitance would be expected to affect the RGC bandwidth significantly, especially for it is part of the feedback loop. Hence, it would interplay with the large C_{pd} and, therefore, limit the RGC bandwidth, as will become evident by the subsequent studies of the RGC

behaviour. In this chapter, the RGC performance is examined extensively against different circuit parameters, including $C_{\mu 1}$ to identify its main bandwidth-limiting factors. The aim is to modify the design to obtain wide-band performance at high transimpedance gain, when large-area and high capacitance photodiodes are employed. The design studies in this chapter are limited to frequency behaviour and deliberately ignore the noise. Noise of the RGC amplifier is straightforward to calculate, and noise minimisation can be done in similar ways to CE or CB amplifiers, using established techniques and therefore not addressed here.

The chapter starts with the derivation and verification of the RGC TIA equivalent circuit model. The RGC TIA performance is then analysed through simulations of its equivalent circuit model, from which design optimisations are concluded. One section is then dedicated to the derivation and verification of the modified RGC TIA equivalent circuit model. The performance of the two TIAs is comparatively assessed through simulation studies of their frequency responses and pole action versus different design parameters. The advantage of the modified RGC is then demonstrated and verified through measurements of the two TIAs.

6.2 Design of the RGC TIA

6.2.1 RGC Equivalent Circuit Model Derivation

In deriving the simplified equivalent circuit model of the RGC, Miller's theorem is applied to split $C_{\mu 1}$ into its equivalent Miller capacitances at the base and collector of Q_1 as C_{mi} and C_{mo}, respectively. This aids in obtaining a compact and tractable RGC transfer function, where the key parameters governing its performance are explicit. The accuracy of the simplified model was compared to and verified against the model without applying Miller's theorem to ensure that the simplified model accurately mimics the RGC TIA behaviour.

Figure 6.2 shows the simplified equivalent model of the RGC TIA. The model is based on standard hybrid-π and T transistor models, for the CE and CB stages, respectively, similar to those in [97]. The model considers the effect of g_m of the two transistors g_{m1} and g_{m2}; input resistance r_{e1}, where $r_{e1} \approx r_{\pi 1}/\beta$; resistive loads R_1 and R_2; base emitter capacitances $C_{\pi 1}$ and $C_{\pi 2}$ and base collector capacitances $C_{\mu 1}$ and $C_{\mu 2}$. Whereas, $C_{\mu 1}$ is split into $C_{mi} = C_{\mu 1}(1 + g_{m1}R_1)$ and $C_{mo} = (1 + 1/g_{m1}R_1)$. The model makes some reasonable simplifying assumptions, such as ignoring the output resistance (r_o) of the BJTs, as its large value makes its effect on the accuracy of the model negligible. Moreover, ignoring the effects of the transistor base spreading resistances r_{bb} and emitter contact resistances R_e, since, they are generally small so their effect is insignificant. The photodiode at the RGC input is represented by an equivalent input current source I_{pd} in parallel with C_{pd}.

Applying nodal analysis to the simplified equivalent circuit model of the RGC shown in Figure 6.2 yields the following equations of summed currents at nodes 1, 2 and 3.

$$(g_{m1} + j\omega(C_{in} + C_t))v_1 - (g_{m1} + j\omega C_t)v_2 = I_{pd} \tag{6.1}$$

$$(g_{m2}R_2 - j\omega C_t R_2)v_1 + (1 + j\omega R_2(C_t + C_{mi}))v_2 = 0 \tag{6.2}$$

$$g_{m1}R_1 v_1 - g_{m1}R_1 v_2 - (1 + j\omega R_1 C_{mo})v_3 = 0 \tag{6.3}$$

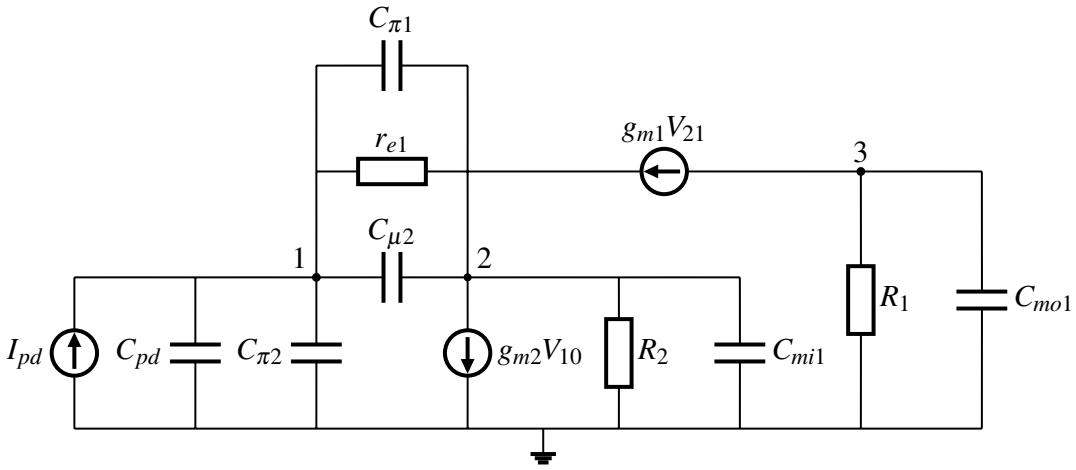


Figure 6.2: Simplified equivalent model of the RGC TIA with photodiode input

where $C_{in} = C_{pd} + C_{\pi 2}$ and $C_t = C_{\pi 1} + C_{\mu 2}$. The nodal equations yields the following equations for the input impedance Z_{in} and voltage gain A_v:

$$Z_{in} = \frac{1 + j\omega R_2(C_t + C_{mi})}{g_{m1}(1 + g_{m2}R_2) + j\omega(C_{in} + C_t(1 + g_{m2}R_2) + g_{m1}R_2C_{mi})) - \omega^2 R_2(C_{in}C_t + C_{in}C_{mi} + C_tC_{mi})} \tag{6.4}$$

The input impedance simplifies at DC to give an input resistance R_{in} as:

$$R_{in} \approx \frac{1}{g_{m1}(1 + g_{m2}R_2)} \tag{6.5}$$

The voltage gain is expressed by:

$$A_v = \frac{g_{m1}R_1(1 + g_{m2}R_2) + j\omega g_{m1}R_1R_2C_{mi}}{(1 + j\omega R_2(C_t + C_{mi}))(1 + j\omega C_{mo}R_1)} \tag{6.6}$$

The voltage gain simplifies at DC to give:

$$A_v(0) = g_{m1}R_1(1 + g_{m2}R_2) \tag{6.7}$$

The transimpedance gain A_T can be approximated by a transfer function composed of a zero z_1, a input complex conjugate pole $p_{(1,2)}$ and output real pole p_3.

$$A_T = R_T \frac{1 + s/\omega_z}{[1 + s/\omega_n Q + s^2/\omega_n^2][1 + s/\omega_{p3}]} \tag{6.8}$$

where

$$R_T = R_1 \tag{6.9}$$

$$\frac{\omega_n}{2\pi} = f_n = \frac{\sqrt{g_{m1}(1+g_{m2}R_2)}}{2\pi\sqrt{R_2(C_{in}C_t + C_{in}C_{mi} + C_tC_{mi})}} \tag{6.10}$$

$$Q = \frac{\sqrt{g_{m1}R_2(1+g_{m2}R_2)(C_{in}C_t + C_{in}C_{mi} + C_tC_{mi})}}{C_{in} + C_t(1+g_{m2}R_2) + g_{m1}R_2C_{mi}} \tag{6.11}$$

where f_n and Q are the natural frequency and the quality factor of $p_{(1,2)}$, respectively, given by:

$$p_{1,2} = -\frac{\pi f_n}{Q} \pm j2\pi f_n\sqrt{(1-Q^2)} \tag{6.12}$$

whereas, p_3 and z_1 are given by:

$$\frac{\omega_{p3}}{2\pi} = p_3 = \frac{1}{2\pi R_1 C_{mo}} \tag{6.13}$$

$$\frac{\omega_{z1}}{2\pi} = z_1 = \ frac1 + g_{m2}R_2 2\pi R_2 C_{mi} \tag{6.14}$$

Finally, to assess the stability of the RGC TIA, it is important to estimate the phase margin, which is related by the Q-factor. As such, according to [98], assuming a second-order system, the amplifier phase margin is given by:

$$pm = tan^{-1}\sqrt{\frac{1+\sqrt{1+4Q^2}}{2Q^2}} \tag{6.15}$$

The RGC DC transimpedance gain is dictated by R_1. Whereas the frequency behaviour of the transimpedance gain is determined by the interaction of $p_{(1,2)}$ and p_3 only, since Z_1 falls at much higher frequencies. Yet, $p_{(1,2)}$ is largely dominant due to the exceptionally large capacitances C_{in} and C_{mi}, except for high values of transimpedance gains (large values of R_1), which shifts the dominance to p_3. The bandwidth-limiting effect of the $C_{\mu 1}$ is made clear by (6.10), where the capacitances C_{in}, C_t and C_{mi} appear in the denominator of the fraction. Therefore, high values

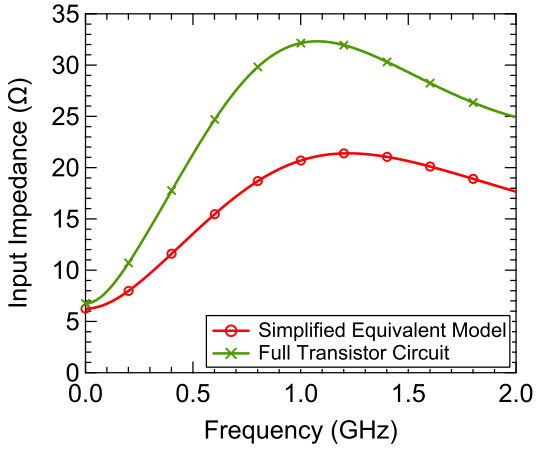
Table 6.1: RGC equivalent model circuit parameter

Parameter	Value
C_π	2.5 pF *
C_μ	0.3 pF *
g_m	40 mS$^+$
R_1	500 Ω$^+$
R_2	75 Ω$^+$

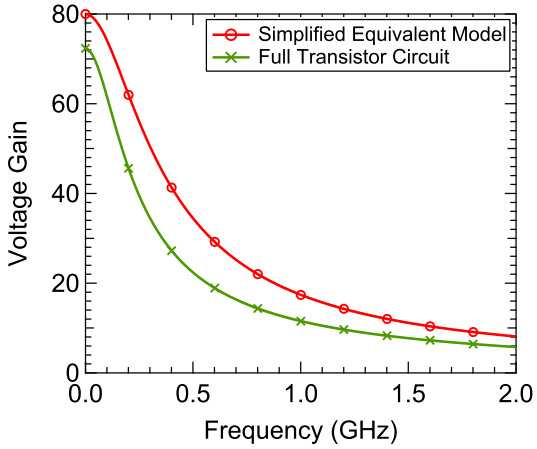
*Fitted values based on datasheets of similar f_T transistors such as the BFR93A.
$^+$Bias dependent parameters, shown to verify analytical equations in (6.4), (6.6) and (6.8).

of any of these capacitances would reduce the frequency of f_n and therefore the frequency of $p_{(1,2)}$. Recalling, $C_{in} = C_{pd} + C_{\pi 2}$, as such out of all the capacitances, C_{pd} and C_{mi} are the dominant capacitances and are therefore the root cause of the RGC bandwidth limitation. Therefore, high values of C_{mi} would clearly reduce the f_n and, in turn, the frequency of $p_{(1,2)}$ dictating the RGC bandwidth. As such, supporting the author's conjectures of the importance of including $C_{\mu 1}$ in the RGC analysis.

The accuracy of the RGC equivalent circuit model is verified by simulating the RGC transistor circuit using NPN silicon transistors, BFU520AR, with $f_T =$ 10 GHz. The transistor circuit simulations are compared to simulations of the equivalent circuit model of Figure 6.2 and to results obtained from the analytical model in (6.4), (6.6) and (6.8). Figures 6.3a-c illustrates the input impedance, voltage gain and transimpedance gain of the RGC transistor circuit and the simplified RGC equivalent circuit model simulations, respectively. In Figure 6.3a, the discrepancy in both the DC input impedance and the peak amplitude between the simplified model and the transistor circuit is because the model does not account for the intrinsic transistor emitter resistances R_{e1} and R_{e2} therefore, tends to underestimate the input resistance and the peak amplitude. Whereas, in Figure 6.3b, the discrepancy in the DC voltage gain between the simplified model and the transistor circuit is because the model does not account for the R_{e1} and R_{e2} and the output resistances r_o of the transistors, which results in a drop in the voltage gain.



(a)



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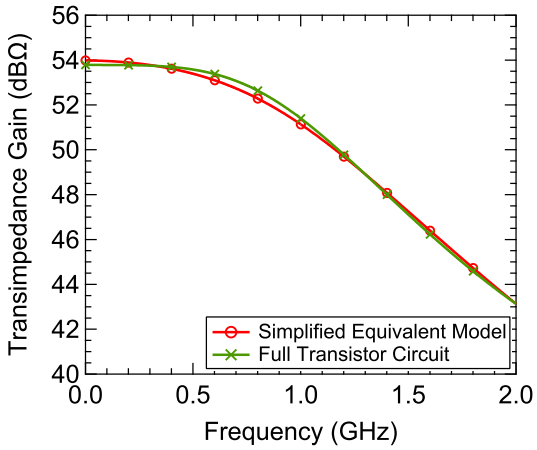


(c)

Figure 6.3: Simulations of the RGC simplified equivalent model vs. full transistor model simulation (a) Input impedance (b) Voltage gain (c) Transimpedance gain

However, despite these small variations in the voltage gain and input resistance between the simplified RGC equivalent circuit model and the transistor circuit, yet the transimpedance gain response provides a fairly accurate estimation of the DC transimpedance gain and the frequency response. Conclusively, the RGC simplified equivalent circuit model reasonably mimics the RGC transistor circuit and can be fairly reliable for further design and optimisation. Noting that including intrinsic transistor resistances R_{e1}, R_{e2} and r_{o1}, r_{o2} will result in much more complex mathematical model and equations. The parameter values of the RGC simplified equivalent circuit model obtained by curve-fitting the RGC model in Figure 6.2 to the full transistor RGC circuit are presented in Table 6.1.

6.3 Performance Assessment of the RGC TIA

In this section, the effects of various RGC design parameters are studied to gain insight into its key bandwidth-limiting factors. The effect of the RGC low input resistance and the Miller effect of $C_{\mu 1}$ are investigated based on simulations of the frequency responses, and pole action of the RGC simplified equivalent circuit model in Figure 6.2. All simulation is based on fitted parameter values of the simplified RGC model presented in Table 6.1, and $C_{pd} = 300$ pF, unless otherwise stated.

6.3.1 Effect of RGC R_{in} on the Bandwidth Performance

This section aims to study the behaviour of the RGC input resistance (R_{in}) and its effect on its bandwidth performance by varying the CE voltage gain (A_{v2}). Where A_{v2} equals the product of g_{m2} and R_2, each parameter is varied independently to assess its effect on the RGC bandwidth, hence, aid in determining the optimum values of g_{m2} and R_2 to enhance the achievable bandwidth. This study is conducted at a fixed transimpedance gain of 500 Ω and $g_{m1} = 40$ mS. Noting that more emphasis is given to study the effects of varying g_{m2} and R_2 on the RGC bandwidth rather than g_{m1}, since variations of g_{m1} have the compound effect of also varying the Miller capacitance of $C_{\mu 1}$, which is independently studied in the following section.

With such exceptionally high C_{pd}, the dominant pole dictating the RGC bandwidth is $p_{(1,2)}$, which is defined by both f_n and the Q-factor. Intuitively, reducing R_{in} should increase the frequency of $p_{(1,2)}$, hence, boosting the RGC bandwidth. By inspecting (6.10) and (6.11), it can be seen that increasing R_2 to reduce R_{in} limits the frequency of f_n, since R_2 appears in the denominator of f_n. In addition to enhancing the peaking amplitudes, since R_2 multiplies twice in the numerator of the Q-factor. Moreover, according to (6.6), increasing R_2 also reduces the cut-off-frequency of A_v, which, as will become evident, significantly limits the achievable bandwidth extension as a result of reducing R_{in} of the RGC. In contrast, increasing g_{m2} does not limit either (6.6) or (6.10), as such can be more effective mean of reducing R_{in} to enhance the RGC bandwidth.

The impact of reducing R_{in} by increasing either g_{m2} or R_2 is examined independently. Initially, the input impedance response is simulated at fixed R_2, while

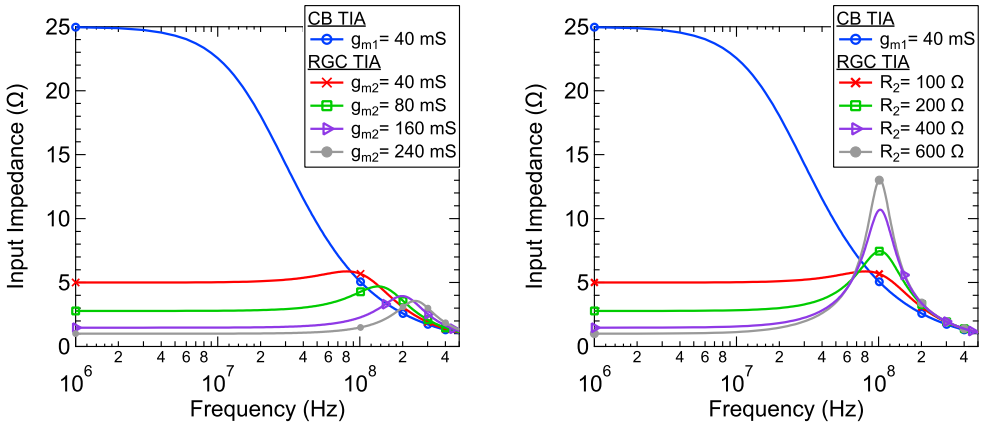


Figure 6.4: Simulations of the RGC input impedance versus the CB at $g_{m1} = 40$ mS (a) variable g_{m2} at constant $R_2 = 100\ \Omega$ (b) variable R_2 at constant $g_{m2} = 40$ mS

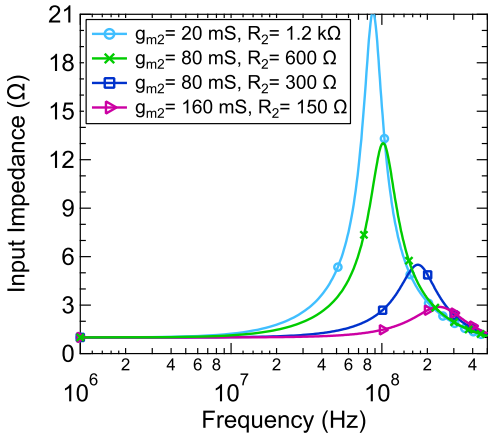
increasing g_{m2}. These impedance responses are also compared to the response of a CB stage running at $g_{m1} = 40$ mS. Similarly, the RGC input impedance response is also simulated at fixed g_{m2}, while increasing and R_2, yet maintaining similar A_{v2} for each respective $g_{m2}R_2$ combination. Figure 6.4a shows the input impedance responses of the CB and the RGC, for the RGC, for $R_2 = 100\ \Omega$ and g_{m2} is varied. Whereas, Figure 6.4b also shows the input impedance responses of the CB and the RGC, yet for the RGC, each of the plots is for $g_{m2} = 40$ mS and R_2 is varied while maintaining similar A_{v2} for each R_2 case as with Figure 6.4a.

From Figure 6.4a, the advantage of the RGC in reducing the CB input resistance is clearly seen, where the CB input resistance is reduced by five times, from 25 Ω to 5 Ω, which is equivalent to the $(1 + g_{m2}R_2)$ factor as given by (6.5). As such, advantageously, the RGC has a much higher tolerance to ultra-high C_{pd}. On the other hand, increasing g_{m2} reduces the RGC input resistance significantly, reaching an extremely low input resistance of approximately 1 Ω at $g_{m2} = 240$ mS, with slight frequency peaking that is gradually suppressed and pushed to higher frequencies. In contrast, Figure 6.4b, shows similar input resistances by increasing R_2 at fixed g_{m2} for each respective case. Nevertheless, reducing the input resistance by increasing R_2 results in significantly different frequency behaviour, where a peak is observed with almost fixed frequency and increasing amplitude. Such behaviour is due to the sensitivity of f_n and the Q-factor to increasing R_2 as indicated earlier

by (6.10) and (6.11), respectively. As such, the frequency of f_n becomes limited, therefore, limiting the bandwidth extension. Whereas the Q-factor increases, hence, the apparent peaking.

The impedance behaviour observed in Figure 6.4b is generally undesirable since it reflects in the transimpedance gain frequency response. Therefore, such behaviour is studied further by simulating the input impedance, voltage gain and transimpedance gain responses of the RGC for a fixed A_{v2} yet, variable values of g_{m2} and R_2 as shown by Figures 6.5a-6.5c, respectively. The results shows that the highest-peaking with the lowest bandwidth is recorded for the lowest value of g_{m2} and the highest value of R_2. On the other hand, significant bandwidth extension is obtained with maximally flat frequency response for the lowest value of R_2 and highest value of g_{m2}.

Hence, it can be concluded that reducing R_{in} is not sufficient to achieve optimum bandwidth performance, the optimisation of g_{m2} and R_2 values is necessary. This is due to the complex nature of the RGC dominant pole $p_{(1,2)}$. As such, despite having a fixed low R_{in} for all the g_{m2} and R_2 combinations investigated in Figures 6.5a-6.5c, yet the product of high g_{m2} and low R_2 gives significantly better bandwidth and frequency behaviour than the product of high R_2 and low g_{m2}.



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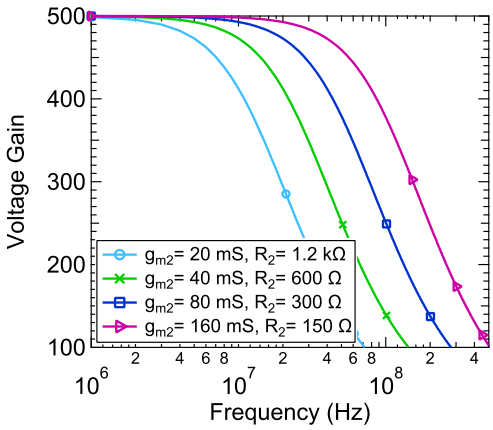

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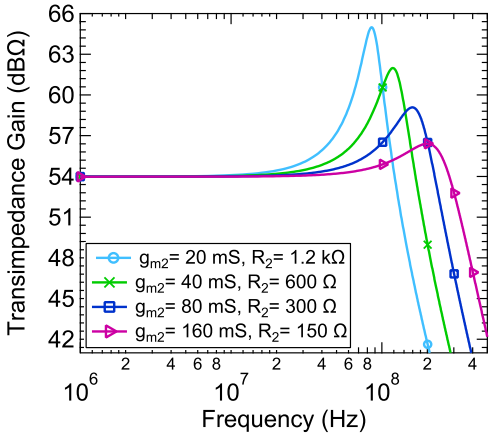


(c)

Figure 6.5: Simulations of the effect of varying g_{m2} and R_2 on the RGC at $R_1 = 500\ \Omega$ and $g_{m1} = 40$ mS (a) Input impednace (b) Voltage gain (c) Transimpedance gain

6.3.2 Miller Effect of $C_{\mu 1}$

The aim of this section is to investigate the effect of the Miller capacitance imposed by $C_{\mu 1}$, in particular C_{mi}, as indicated by (6.10)-(6.12), by means of varying the Miller multiplier equals $(1+A_{v1})$, where A_{v1} is the product of g_{m1} and R_1. Initially, the effect of varying R_1 is examined for different values of $C_{\mu 1}$, while fixing $g_{m1} =$ 40 mS, $g_{m2} = 240$ mS and $R_2 = 100\ \Omega$. The value of R_1 is sequentially increased, while recording the bandwidth and the Q-factor for each case. Figure 6.6a shows the recorded RGC bandwidths as R_1 is increased from 100 Ω to 3.1 kΩ for different values of $C_{\mu 1}$. Ideally, for $C_{\mu 1} = 0$, the RGC bandwidth is independent of R_1. This is because, in such a case, the Miller effect associated with $C_{\mu 1}$ is eliminated. Hence the C_{mi} term in f_n is omitted; as such, the bandwidth becomes insensitive to increasing transimpedance gain. However, in cases where $C_{\mu 1}$ is a non-zero value starting from $C_{\mu 1}$ equals 0.1 pF to 0.5 pF, increasing R_1 results in substantial reduction in the RGC bandwidth. Such bandwidth reduction is due to the increase in C_{mi} as a result of increasing A_{v1}, which in turn reduces the frequencies of f_n and $p_{(1,2)}$.

Increasing R_1 also have the downside of increasing the Q-factor of $p_{(1,2)}$ as given by (6.11), which is a consequence of the increase in C_{mi}. High Q-factor results in high peaking and, therefore, reduce the phase margin of the TIA. Hence, it is important to examine variations in the Q-factor and in turn the phase margin as given by (6.15), as the value of R_1 increases to achieve high transimpedance gain, especially in cases where $C_{\mu 1}$ is high. Figure 6.6b shows the variation in the Q-factor of the RGC for different values of $C_{\mu 1}$ as R_1 is increased. Ideally, for $C_{\mu 1} = 0$, the Q-factor is independent of R_1, since the Miller effect is eliminated and therefore, $p_{(1,2)}$ becomes independent of of R_1. For relatively low R_1, it is clear that the variation in the Q-factor for the different $C_{\mu 1}$ is not substantial. However, as R_1 increases and in turn, A_{v1}, the value of the Q-factor varies significantly with higher values corresponding to cases with higher $C_{\mu 1}$, which presents higher Miller capacitance C_{mi}.

A high Q-factor directly translate into a reduced amplifier phase margin as observed in Figure 6.6c. It is evident that as the Q-factor increases, the phase margin

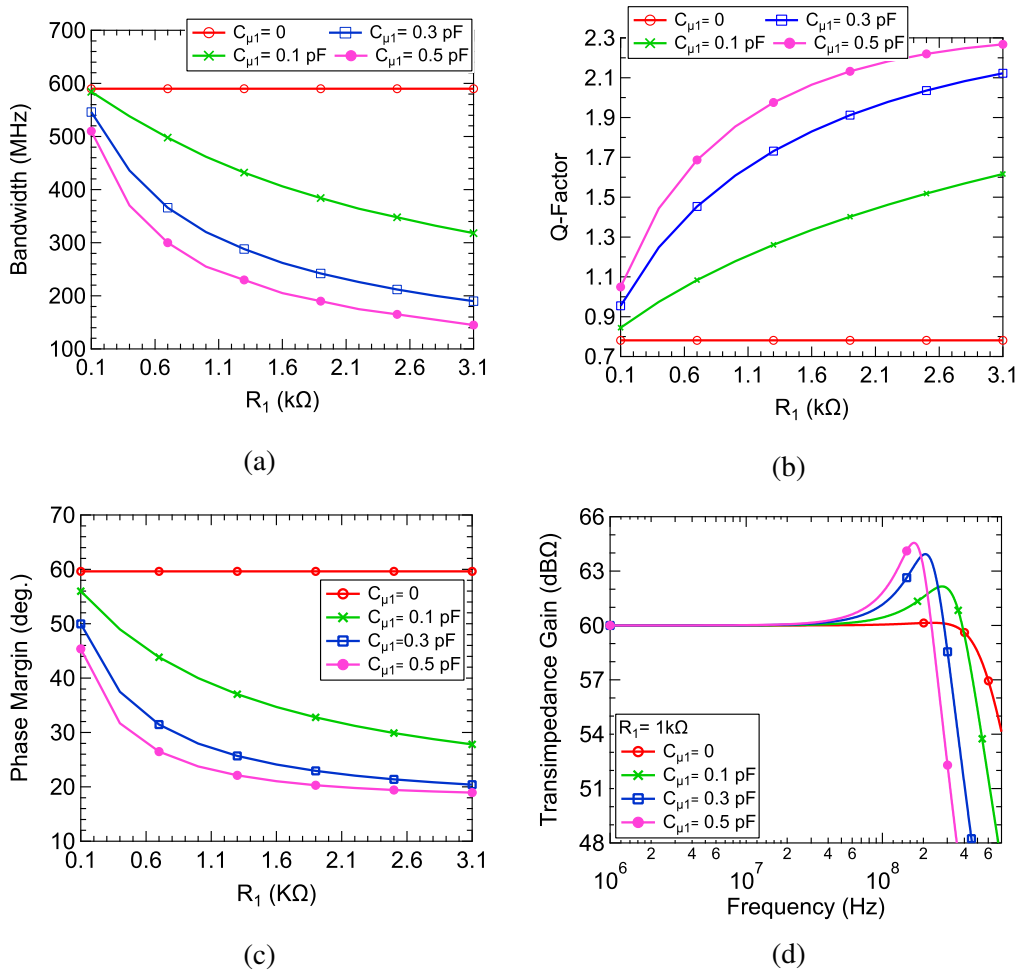


Figure 6.6: The effect of varying R_1 for different $C_{\mu 1}$ on the RGC at $g_{m1} = 40$ mS, $g_{m2} = 240$ mS and $R_2 = 100$ Ω (a) Bandwidth (b) Q-factor (c) Phase margin (d) Transimpedance gain

is reduced. While amplifiers with such phase margin are theoretically stable, in practice, amplifiers must be designed with a phase margin substantially in excess of 0° to ensure stability. The reason is that many practical factors can reduce the phase margin below the theoretical minimum. Conventionally, amplifiers are designed to achieve a typical phase margin of at least 45° which, is a common compromise between wide-band possibly unstable operation and narrow-band stable operation. Therefore, if $C_{\mu 1}$ is high, then the designer will have to lower R_1 to ensure moderate peaking and sufficient phase margin yet, this comes at the cost of reduced transimpedance gain. Figure 6.6d shows the RGC transimpedance gain response at 1 kΩ to illustrate its bandwidth and frequency peaking behaviour for the different

$C_{\mu 1}$ cases, where it is clear that higher $C_{\mu 1}$ values result in reduced bandwidth and high peaking amplitude.

Therefore, based on the bandwidth, Q-factor and phase margin variations of the RGC for the different values of $C_{\mu 1}$ and R_1. It is concluded that the significance of $C_{\mu 1}$ on the RGC bandwidth and frequency peaking relies on the Miller multiplier $(1 + A_{v1})$. For relatively low R_1 and in turn low A_{v1}, the effect of C_{mi} is low, as such large values of $C_{\mu 1}$ has minimal effect on the RGC bandwidth and frequency peaking. Where the RGC maintained a fairly constant bandwidth and a reasonable Q-factor, irrespective of the $C_{\mu 1}$ value. Nevertheless, for higher values of R_1 and in turn A_{v1}, the effect of $C_{\mu 1}$ became more critical, since its associated Miller capacitances are higher. Consequently, the high $C_{\mu 1}$ coupled with the high R_1 results in substantial bandwidth reduction and an increase in the Q-factor, which leads to a significant reduction in the phase margin.

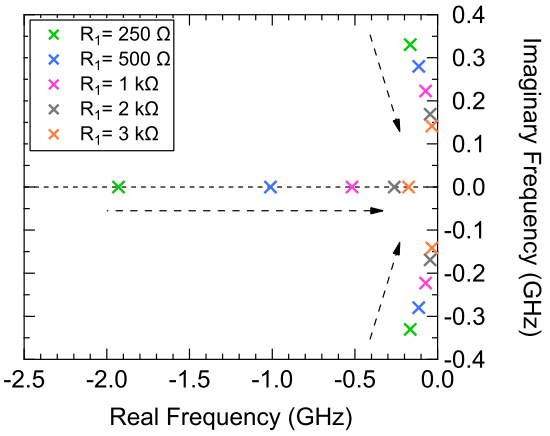
To illustrate these conclusions, the RGC behaviour is examined by plotting its pole action, on the s-plane, as R_1 is increased from 250 Ω to 3 kΩ as shown by Figure 6.7a, while simultaneously examining its corresponding transimpedance gain responses for each respective R_1 value. Figure 6.7a shows the RGC pole action including both the input complex pole $p_{(1,2)}$ and the output real pole p_3, as R_1 increases. Clearly, increasing R_1 results in a reduction in the frequencies of both $p_{(1,2)}$ and p_3 as indicated by (6.12) and (6.13), respectively, yet for all cases of R_1, $p_{(1,2)}$ comes at lower frequencies than p_3. As such, the RGC bandwidth is mostly dictated by $p_{(1,2)}$, especially for $R_1 = 250$ Ω, 500 Ω and 1 kΩ cases, where p_3 is nearly 10 times higher than $p_{(1,2)}$. Hence, for such cases, the effect of p_3 on the RGC bandwidth is negligible. Even for $R_1 = 2$ kΩ and 3 kΩ, although p_3 becomes closer to $p_{(1,2)}$, so its effect on the RGC bandwidth becomes slightly more significant as indicated by the faster roll-off of the transimpedance gain responses for $R_1 = 2$ kΩ and 3 kΩ, in comparison to the lower R_1 cases shown by Figure 6.7c, yet even then, the bandwidth-limitation resulting from p_3 is relatively insignificant, as such, can be also ignored.

Therefore, since the dominant bandwidth-limiting effect of $p_{(1,2)}$ has been

established, Figure 6.7b plots only its corresponding pole action as R_1 increases. Clearly, increasing R_1 pushes $p_{(1,2)}$ towards the unstable region of the s-plane as indicated by the arrow. This is because increasing R_1 increases C_{mi}, which in turn increases the Q-factor of $p_{(1,2)}$, hence, reducing the RGC phase margin as illustrated in Figures 6.6b and 6.6c, respectively, which again highlights the trade-off between the RGC transimpedance gain and stability. Moreover, the reduction in bandwidth as R_1 increases is demonstrated via the reduction in the distance between each of the $p_{(1,2)}$ from the real axis, which is equivalent to the value of f_n. Hence, also highlighting the trade-off between the bandwidth and transimpedance gain of the RGC TIA.

The effect of increasing R_1 on the RGC performance observed by its pole action can be appreciated by its corresponding transimpedance gain responses shown in Figure 6.7c, where increasing R_1 (transimpedance gain) results in a substantial drop in the RGC bandwidth by approximately 240%. Such bandwidth reduction is mainly because $p_{(1,2)}$ is a function of R_1 as imposed by the C_{mi} in (6.10). In other words, increasing R_1 has the effect of increasing the Miller multiplier $(1+g_{m1}R_1)$ of $C_{\mu 1}$, hence reducing the frequency of f_n and in turn the frequency of the dominant $p_{(1,2)}$, as such reducing the RGC bandwidth. Moreover, the increased peak amplitude, which reduces the RGC phase margin, can potentially jeopardise the amplifier stability. Hence, the Miller effect imposes a trade-off between the amplifier bandwidth and a well-behaved stable operation.

Similar bandwidth limitations are imposed by C_{mi}, when attempting to enhance the RGC bandwidth by reducing its input resistance via increasing g_{m1}, which in turn increases the Miller multiplier (A_{v1}) of $C_{\mu 1}$. Hence, limiting the RGC achievable bandwidth extension. As discussed in Chapter 5, generally, increasing g_{m1} of the RGC TIA is not desirable, particularly in low power designs or designs with limited voltage headroom. Since increasing g_{m1} would increase the voltage drop across R_1, hence, requiring higher voltage supplies V_{CC} to maintain the bias conditions for the CB stage Q_1, which is not efficient in terms of power consumption. Alternatively, the value of R_1 would be reduced, yet this limits the



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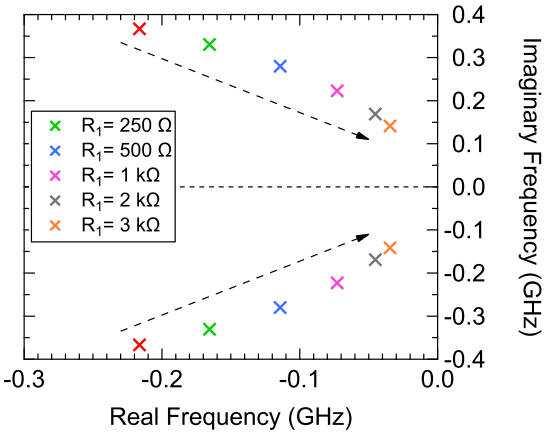

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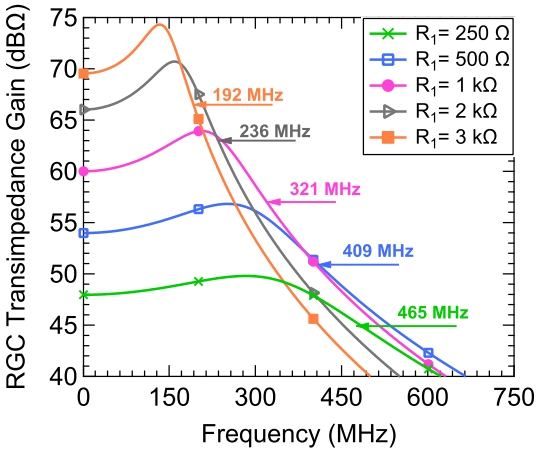
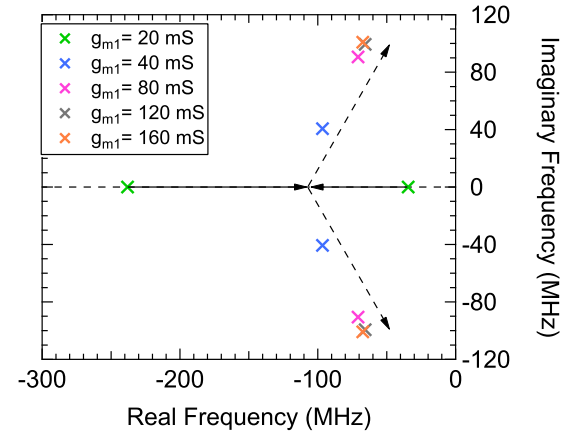


(c)

Figure 6.7: Simulations of the effect of increasing R_1 on the RGC TIA at $g_{m1} =$ 40 mS, $g_{m2} = 240$ mS and $R_2 = 100$ Ω (a) Pole action including $p_{(1,2)}$ and p_3 (b) Pole action including only $p_{(1,2)}$ (c) Transimpedance gain



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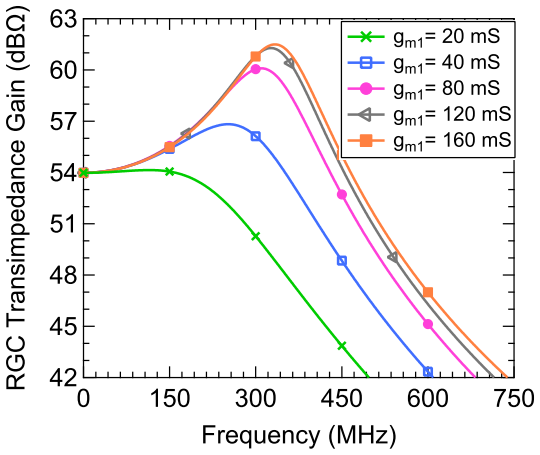


(b)

Figure 6.8: Simulations of the effect of increasing g_{m1} on the RGC TIA at $R_1 = 500\ \Omega$, $g_{m2} = 240$ mS and $R_2 = 100\ \Omega$ for $C_{\mu 1} = 0.3$ pF (a) Pole action including $p_{(1,2)}$ only (b) Transimpedance gain

RGC transimpedance gain. Even so, the effects of increasing g_{m1} are still studied to verify the bandwidth-limiting effect imposed by C_{mi}.

The effect of varying g_{m1} on the RGC is examined by plotting its pole action, on the s-plane, as g_{m1} increases from 20 mS to 160 mS as shown by Figure 6.8a, while simultaneously examining its corresponding transimpedance gain responses for each respective g_{m1} value as shown by Figure 6.8b. Figure 6.8a shows the pole action of $p_{(1,2)}$ only as g_{m1} increase, since it has been established that p_3 is generally at much higher frequency than $p_{(1,2)}$ so it has negligible effect on the bandwidth as illustrated in Figure 6.7a. Noting the p_3 is a function of g_{m1} as imposed by C_{mo} in

(6.13), yet the reduction in p_3 as result of increasing g_{m1} is minimal. In Figure 6.8a, starting with $g_{m1} = 20$ mS, it can be observed that $p_{(1,2)}$ is defined by a real pole pair before it breaks in the s-plane as g_{m1} is increased. This is because for such low g_{m1}, the Q-factor of $p_{(1,2)}$ is less than 0.5. Hence, the resulting RGC transimpedance gain response is over-damped, as illustrated by its corresponding curve in Figure 6.8b. Such low values of Q at $g_{m1} = 20$ mS, is a result of the low A_{v1} and in turn the effect of C_{mi} on the Q-factor as given by (6.11) is minimal. Increasing g_{m1} pushes $p_{(1,2)}$ towards the unstable region of the s-plane as indicated by the arrow. Such behaviour is due to the increase in C_{mi} as A_{v1} increases due to the increase in g_{m1}. As such, leading to a higher Q-factor as indicated by the increased peaking amplitudes for the corresponding transimpedance gain responses in Figure 6.8b. Moreover, the increase in bandwidth is indicated by the increased distance between $p_{(1,2)}$ and the real axis, as also reflected by the transimpedance gain responses in Figure 6.8b. Nevertheless, such bandwidth enhancement is offset by the significant increase in the peaking amplitude where for g_{m1} higher than 80 mS, the increase in the RGC bandwidth becomes minimal with a significantly high peak. Therefore, it is best to opt for lower values of g_{m1}, since on account of the RGC stability, the effect of C_{mi} is minimised, as such leading to a well-behaved frequency behaviour.

Hence, based on the above analysis of the RGC TIA, it can be concluded that the RGC TIA offers extremely low input resistance compared to other configurations such as the CB TIA. Such an advantage is a result of the negative feedback provided by the auxiliary CE stage, which reduces the RGC input resistance by almost equals the CE voltage gain $A_{v2} = (1 + g_{m2}\, R_2)$, in comparison to the CB stage, which provides the RGC with high-tolerance to exceptionally high C_{pd}. It was inferred that optimisation of A_{v2} by carefully choosing the values of g_{m2} and R_s is essential to enhance the achievable bandwidth, where employing higher g_{m2} and R_2 is more effective means of reducing R_{in} and extending the RGC bandwidth. Last but not least, critical analysis of the RGC equivalent circuit model in Figure 6.2, led to the identification of the Miller effect of $C_{\mu 1}$ of the CB stage of the RGC, as performance limiting, as it imposes a trade-off between the RGC bandwidth, tran-

simpedance gain and stability. Hence, if the undesirable Miller effect of $C_{\mu 1}$ is neutralised then the RGC performance can be significantly improved. As such, a modification of the conventional RGC TIA is proposed as described by the following section.

6.4 Design of a Modified RGC TIA

Studies of the RGC TIA in Section 6.3, indicated a major limitation on its bandwidth and transimpedance gain imposed by the Miller effect associated with $C_{\mu 1}$, in particular C_{mi}. Since increasing R_1 to boost the RGC transimpedance gain, has the undesirable effect of increasing C_{mi}, hence, significantly reducing the bandwidth and therefore imposing a stringent trade-off between transimpedance gain and bandwidth. Furthermore, increasing g_{m1} to extend the RGC bandwidth by reducing its input resistance also has the counteractive effect of increasing C_{mi}, hence, limiting the achievable bandwidth enhancement. Moreover, it was concluded that increasing either R_1 or g_{m1} leads to a significant increase in the Q-factor of the RGC, hence, reducing its phase margin, which may compromise the RGC stability.

Such undesirable characteristics can be simply eliminated by introducing an additional cascode stage that neutralises the Miller effect of $C_{\mu 1}$ as shown by Figure 6.9. In this circuit, the Miller capacitance resulting from $C_{\mu 1}$ of Q_1 is eliminated through a cascode configuration that adds a CB stage Q_3. Therefore, the signal flowing from the collector of Q_2 to the base of Q_1 is not limited by the Miller effect of $C_{\mu 1}$. In other words, the proposed RGC modification extends the bandwidth of the

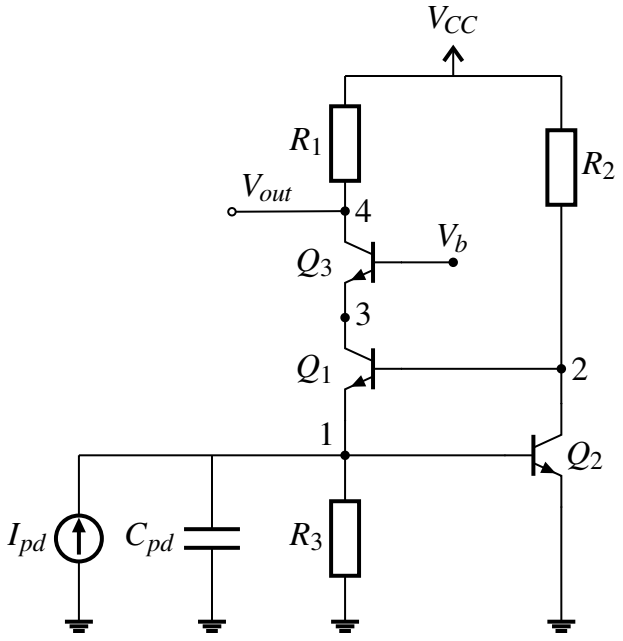


Figure 6.9: The modified RGC TIA circuit with photodiode input

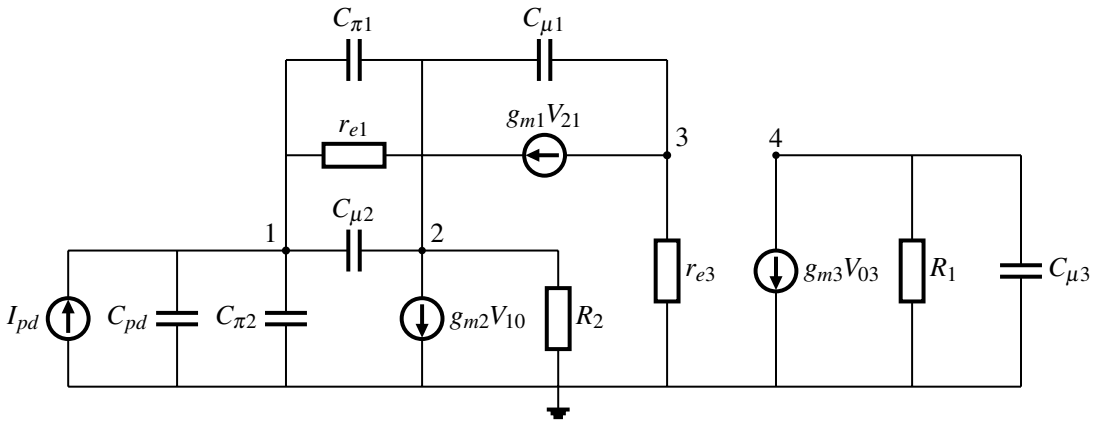


Figure 6.10: Simplified equivalent model of the modified RGC with photodiode input

RGC by neutralising the impact of the Miller effect of $C_{\mu 1}$ on the frequency of $p_{(1,2)}$, thus shifting the location of the $p_{(1,2)}$ to a higher frequency. Advantageously, the modified RGC also relaxes the trade-off between the RGC transimpedance gain and bandwidth, since the frequency of $p_{(1,2)}$ becomes independent of R_1, as such the gain can be increased, whilst largely maintaining the desirable high bandwidth.

6.4.1 Modified RGC Equivalent Model Derivation

Figure 6.10 shows the simplified equivalent circuit model of the modified RGC. Similar to the RGC model derivation, the modified RGC model is based on standard hybrid-π and T transistor models for the CE and CB stages. The model takes into account g_m of the three transistors g_{m1}, g_{m2} and g_{m3}. The input resistance of the transistors Q_1 and Q_3. Again, the simplifying assumption of negligible effects of r_o, r_{bb} and R_e of the BJT is made. The nodal analysis of the small-signal model yields the following equations of summed currents at nodes 1, 2, 3 and 4.

$$(g_{m1} + j\omega(C_{in} + C_t))v_1 - (g_{m1} + j\omega C_t)v_2 = I_{pd} \tag{6.16}$$

$$(g_{m2}R_2 - j\omega C_t R_2)v_1 + (1 + j\omega R_2(C_t + C_{\mu 1}))v_2 - j\omega C_{\mu 1}R_2 v_3 = 0 \tag{6.17}$$

$$-g_{m1}v_1 + (g_{m1} - j\omega C_{\mu 1})v_2 + (g_{m3} + j\omega C_{\mu 1})v_3 = 0 \tag{6.18}$$

$$-g_{m3}R_1 v_3 + (1 + j\omega C_{\mu 3}R_1)v_4 = 0 \tag{6.19}$$

Recalling that $C_{in} = C_{pd} + C_{\pi 2}$ and $C_t = C_{\pi 1} + C_{\mu 2}$. The nodal equations yields the following expressions for Z_{in} and A_v, under the simplifying assumption that $g_{m1} = g_{m3}$. Hence, Z_{in} is given by:

$$Z_{in} = \frac{1 + j\omega R_2(C_t + 2C_{\mu 1}) - \omega^2 \frac{R_2 C_t C_{\mu 1}}{g_{m3}}}{1/R_{in} + j\omega(C_{in} + (C_t + C_{\mu 1})(1 + A_{v2}) + C_{\mu 1} g_{m1} R_2)) - \omega^2 R_2(C_{in}(C_t + 2C_{\mu 1}) + C_t C_{\mu 1}(1 + \frac{g_{m2}}{g_{m3}}))} \tag{6.20}$$

which simplifies at DC to give:

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2} R_2)} \tag{6.21}$$

whereas, A_v is expressed by:

$$A_v = \frac{g_{m1} R_1(1 + g_{m2} R_2) + j\omega R_1 R_2 C_{\mu 1}(g_{m1} - g_{m2}) - \omega^2 C_t C_{\mu 1} R_1 R_2}{(1 + j\omega C_{\mu 3} R_1)(1 + j\omega R_2(C_t + 2C_{\mu 2}) - \omega^2 \frac{C_t C_{\mu 1} R_2}{g_{m3}})} \tag{6.22}$$

A_v simplifies at DC to give:

$$A_v(0) = g_{m1} R_1(1 + g_{m2} R_2) \tag{6.23}$$

The transimpedance gain A_T can be approximated by a transfer function composed of an input complex conjugate pole $p_{(1,2)}$ and an output real pole p_3. Noting that the zero of the modified RGC transfer function is at much higher frequencies than the system poles, so is neglected for simplicity.

$$A_T = R_T \frac{1}{[1 + s/\omega_n Q + s^2/\omega_n^2][1 + s/\omega_{p3}]} \tag{6.24}$$

where

$$R_T = R_1 \tag{6.25}$$

$$\frac{\omega_n}{2\pi} = f_n = \frac{\sqrt{g_{m1}(1 + g_{m2} R_2)}}{2\pi\sqrt{R_2(C_{in}(C_t + 2C_{\mu 1}) + C_t C_{\mu 1}(1 + g_{m2}/g_{m3}))}} \tag{6.26}$$

$$Q = \frac{\sqrt{g_{m1}(1 + g_{m2} R_2)(C_{in} R_2(C_t + 2C_{\mu 1}) + C_t C_{\mu 1}(1 + g_{m2}/g_{m3}))}}{C_{in} + (C_t + C_{\mu 1})(1 + g_{m2} R_2) + C_{\mu 1} g_{m1} R_2} \tag{6.27}$$

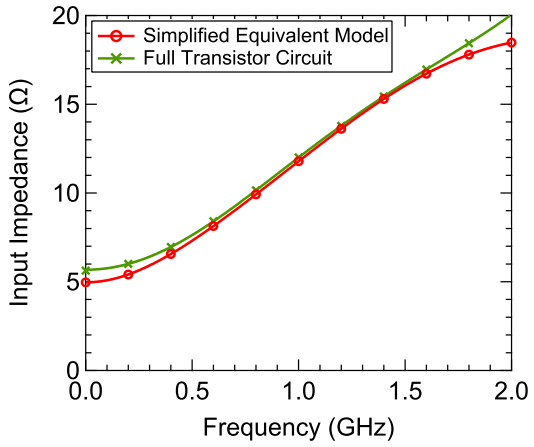
The input complex pole $p_{(1,2)}$ and the output pole p_3 is given by:

$$p_{1,2} = -\frac{\pi f_n}{Q} \pm j2\pi f_n \sqrt{(1-Q^2)} \tag{6.28}$$

$$\frac{\omega_{p3}}{2\pi} = p_3 = \frac{1}{2\pi R_1 C_{\mu 3}} \tag{6.29}$$

The DC behaviour of the modified RGC is similar to the conventional design, where the input resistance, DC transimpedance gain and the voltage gain are unchanged. Nevertheless, the frequency behaviour of the modified RGC is significantly improved, where it is clear from (6.26) and (6.27) that the C_{mi} term of (6.10) and (6.11) is now removed, therefore, the frequency of the dominant $p_{(1,2)}$ of the modified RGC is increased, resulting in a significant bandwidth enhancement. Furthermore, $p_{(1,2)}$ is no longer a function of R_1. Thereby, in theory, the bandwidth of this circuit is independent of its transimpedance gain when the frequency spacing between $p_{(1,2)}$ and p_3 is sufficiently large. Such characteristics are highly desirable for VLC receivers, since as discussed in Chapter 5, the free-space channel highly limits the received optical signal power. Therefore, employing high gain TIAs is crucial for the received signal recovery. As such, in the case of the modified RGC, the transimpedance gain can be increased while maintaining its high bandwidth advantage. The effects of neutralising the Miller effect of $C_{\mu 1}$ is further studied in the following section.

The accuracy of the modified RGC equivalent circuit model is verified by simulating the modified RGC transistor circuit using NPN silicon transistors, BFU520AR, with $f_T = 10$ GHz. The transistor circuit simulations are compared to simulations of the equivalent circuit model of Figure 6.10 and to results obtained from the analytical model in (6.20), (6.22) and (6.24). The fitted parameter values of the modified RGC simplified equivalent circuit model used in simulations are similar to those presented in Table 6.1, since the same transistors were used for the modified RGC transistor circuit. Figures 6.11a-6.11c illustrate the simulated input impedance, voltage gain and transimpedance gain of the modified RGC transistor circuit and its simplified equivalent circuit model, respectively. In Figures 6.11a and



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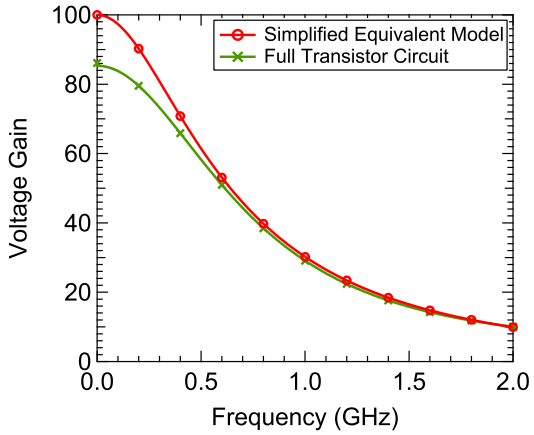

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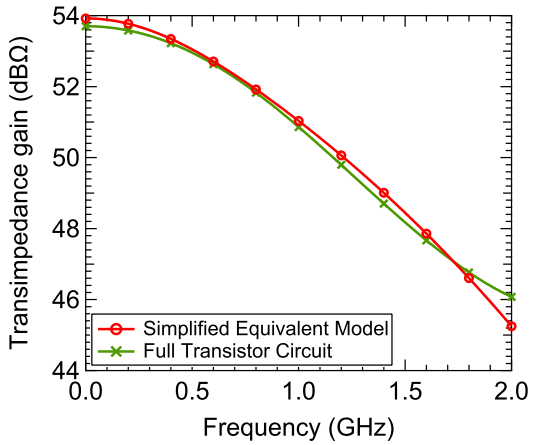


(c)

Figure 6.11: Simulations of the modified RGC simplified equivalent circuit model vs. full transistor circuit (a) Input impedance (b) Voltage gain (c) Transimpedance gain

6.11b the discrepancy in both the DC input impedance and the peak amplitude between the simplified equivalent model and the full transistor model is again because the simplified model does not account for the intrinsic transistor emitter resistances R_{e1} and R_{e2}. Therefore, it tends to underestimate the input resistance and the peak amplitude. Whereas, in Figure 6.11b, the discrepancy between the DC voltage gain between the transistor circuit and the simplified model is because the model does not account for emitter contact resistances R_e and output resistances r_o of the transistors, which results in a drop in the voltage gain value. However, despite these small variations in the voltage gain and input resistance between the simplified modified RGC equivalent circuit model and the transistor circuit, yet the transimpedance gain provides a reasonably accurate estimation of the DC transimpedance gain and the frequency response. Thus, conclusively, the modified RGC simplified equivalent circuit model reasonably mimics the full transistor circuit and can be fairly reliable for further design and optimisation.

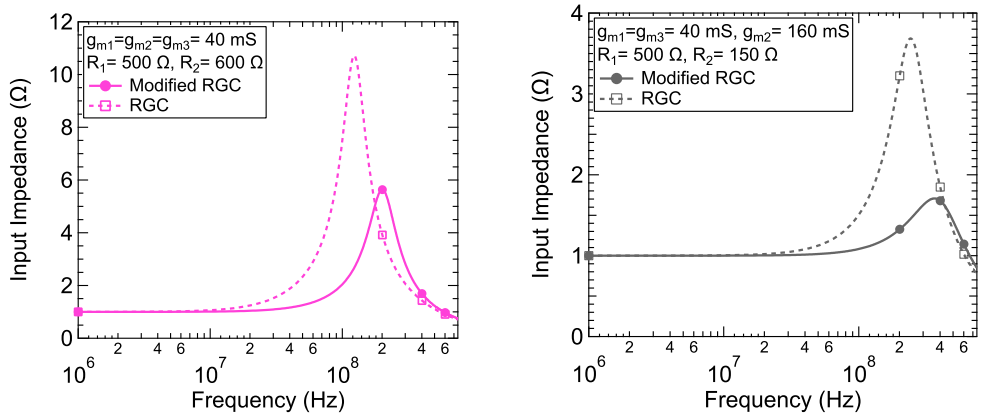
6.5 Comparative Assessment of the RGC & the Modified RGC TIAs

This section compares the performance of the proposed modified RGC in comparison to the conventional RGC. The effects of neutralising the Miller capacitance of $C_{\mu 1}$ are investigated based on simulations of the frequency responses and pole action of the simplified equivalent models in Figures 6.2 and 6.10.

6.5.1 Comparison of R_{in} of the RGC & Modified RGC

When a photodiode with a large C_{pd} is placed at the input of a TIA, the dominant pole location shifts to the input node, which reduces its bandwidth significantly. This is because the input pole is usually the product of C_{pd} and the TIA input resistance R_{in}. Thus, intuitively, reducing R_{in} shifts the frequency of the dominant input pole to higher frequencies and, as such, enhance the bandwidth of the TIA. Nevertheless, for the RGC, the complex nature of the input dominant pole $p_{(1,2)}$ dictate additional design optimisations, where reducing R_{in} is often not sufficient to obtain optimal bandwidth performance. Yet, the means of reducing R_{in} significantly impacts the achievable bandwidth as shown in Section 6.3.1. It was concluded that R_{in} is reduced by increasing the voltage gain A_{v2} of the feedback CE stage. Yet for a given A_{v2}, it is best to opt for a combination of high g_{m2} and low R_2 rather than low g_{m2} and high R_2. This is because high values of R_2 limits the frequency of f_n and in turn $p_{(1,2)}$ as illustrated in Figures 6.5a-6.5c. Therefore, to boost the achievable bandwidth, it is best to reduce R_{in} by increasing g_{m2} and reducing R_2.

In the case of the modified RGC, similar design optimisation prevails, where again high R_2 limits the frequency of f_n and in turn its dominant input pole $p_{(1,2)}$ as indicated by (6.26) and (6.28). Nevertheless, because of the neutralisation of the Miller effect of $C_{\mu 1}$, which in turn omits the C_{mi} term of $p_{(1,2)}$, it is predicted that the bandwidth of the modified RGC, for any given A_{v2}, irrespective of the choice of g_{m2} and R_2 is significantly higher in comparison to the conventional design. Such bandwidth behaviour is examined by simulating the input impedance, voltage gain and transimpedance gain responses of two TIAs for at $g_{m1} = 40$ mS and $R_1 = 500\ \Omega$



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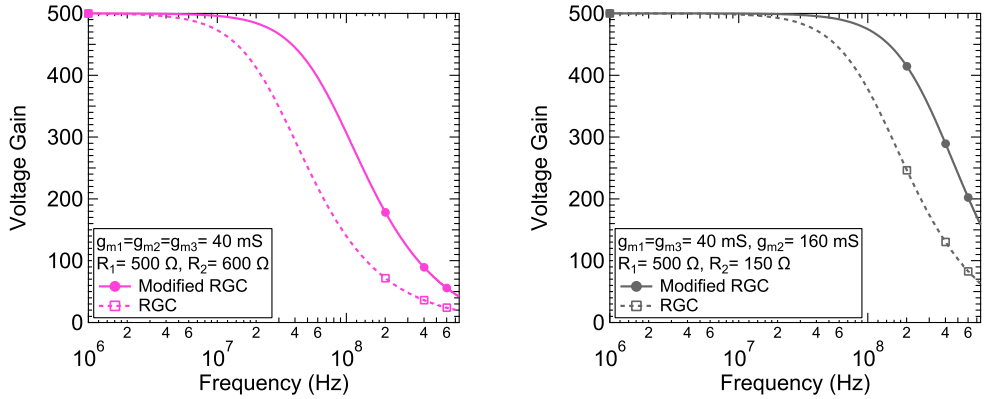

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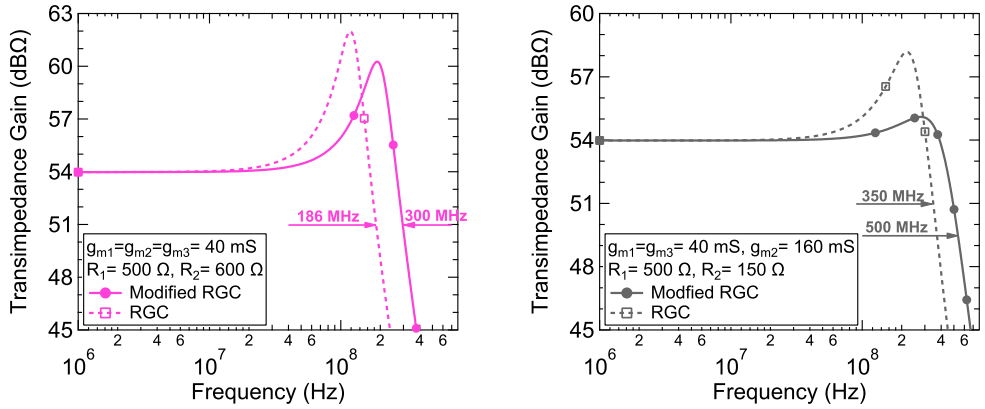

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Figure 6.12: The effect of different values of g_{m2} and R_2 on the RGC and modified RGC TIAs for Case 1 (left side) and Case 2 (right side) at $g_{m1} = 40$ mS and $R_1 = 500\ \Omega$ (a) Input impedance (b) Voltage gain (c) Transimepdance gain

at $A_{v2} = 24$ for 2 cases of g_{m2} and R_2, where Case 1: $g_{m2} = 40$ mS and $R_2 = 600\ \Omega$, whereas, Case 2: $g_{m2} = 160$ mS and $R_2 = 150\ \Omega$.

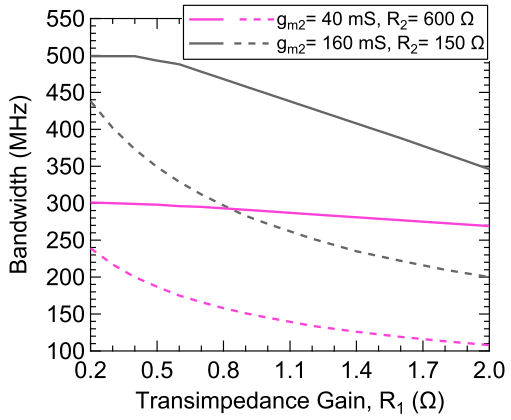
Figures 6.12a, 6.12b and 6.12c illustrates the input impedance, voltage gain and transimpedance gain responses of the two TIAs for the 2 cases of g_{m2} and R_2, respectively. From Figure 6.12a illustrating the TIAs input impedance responses, it shows that for Case 1 (top left), it is clear that the modified RGC has the same input resistance as the conventional RGC. Yet, it improves the impedance frequency behaviour by shifting the impedance peak of the RGC to higher frequencies while suppressing its amplitude. This improvement in the input impedance frequency behaviour is due to the neutralisation of the Miller effect of $C_{\mu 1}$ of the RGC. Whereas in Case 2 (top right), a similar trend is observed for the two TIAs, yet each impedance profile appears to be flatter compared to Case 1, which is a result of using optimised values of g_{m2} and R_2, since high values of R_2 increases the Q-factor as indicated by (6.11) and (6.27).

Figure 6.12b illustrating the TIAs voltage gains show that for Case 1 (middle left), the modified RGC voltage gain response has a higher cut-off-frequency than the conventional RGC, with a less frequency-dependent behaviour. In Case 2 (middle right), the TIAs show a similar trend, yet the voltage gain responses appear to be much less frequency-dependent than Case 1. The trends observed from the input impedance and voltage gain responses are directly reflected in the transimpedance gain responses of the two TIAs shown in Figure 6.12c, where the modified RGC results in substantial improvement in bandwidth and peaking behaviour over the conventional design, irrespective of the g_{m2} and R_2 values. Such bandwidth advantage is a result of ameliorating the bandwidth-limiting Miller capacitance associated with $C_{\mu 1}$, which increases the frequency of $p_{(1,2)}$. Nevertheless, it is clear that operating at a combination of low g_{m2} and high R_2 yields higher bandwidth enhancement with moderate peaking amplitudes when compared to operating at low g_{m2} and high R_2. Hence, it can be concluded that similar design optimisations of the values of g_{m2} and R_s also hold for the modified RGC TIA.

6.5.2 Effects of Neutralising the Miller Capacitance of $C_{\mu 1}$

As previously discussed in Section 6.4.1, neutralising the Miller capacitance of $C_{\mu 1}$ results in several advantages, as proposed by the modified RGC. First, it results in substantial bandwidth enhancement, which is due to the elimination of the bandwidth-limiting C_{mi} term of f_n in (6.10) as seen in (6.26), hence, increasing the frequency of the dominant $p_{(1,2)}$ of the modified RGC and in turn its bandwidth. Second, it relaxes the stringent trade-off between the transimpedance gain and bandwidth of the RGC TIA, since $p_{(1,2)}$ of the modified RGC is independent of R_1. Thereby, in theory, the bandwidth of the modified RGC is independent of its transimpedance gain, provided the frequency spacing between $p_{(1,2)}$ and p_3 is sufficiently large. Finally, on account of the TIAs stability, again, it eliminates the C_{mi} term of the RGC Q-factor in (6.11), as seen in (6.27); therefore, the Q-factor of the modified RGC is lower, which corresponds to a lower peaking amplitude and in turn improved phase margin. Such advantages of the modified RGC frequency behaviour is illustrated by recording its bandwidth, Q-factor and phase margin in comparison to the conventional RGC for increasing the transimpedance gain (R_1) as illustrated by Figures 6.13, 6.13b and 6.13c, respectively. The performance of the two TIAs is recorded at $g_{m1} = 40$ mS for 2 cases of g_{m2} and R_2, where Case 1: $g_{m2} = 40$ mS and $R_2 = 600\ \Omega$ and Case 2: $g_{m2} = 160$ mS and $R_2 = 150\ \Omega$, while R_1 is varied from 200 Ω to 2 kΩ.

Figure 6.13 shows the 3-dB bandwidths of the two TIAs versus transimpedance gain. Noticeably, for Case 1 ($g_{m2} = 40$ mS and $R_2 = 600\ \Omega$), the modified RGC exhibits almost constant bandwidth as R_1 (transimpedance gain) is increased, with only slight reduction at higher R_1 values, of approximately 10% (30 MHz) of its values at 200 Ω. This is because the dominant $p_{(1,2)}$ of the modified RGC is independent of R_1. Nevertheless, the slight reduction in the modified RGC bandwidth at higher R_1 is due to the reduction in the frequency of p_3, which reduces the pole spacing between $p_{(1,2)}$ and p_3, as such making the effect of p_3 on the modified RGC bandwidth slightly more significant. In contrast, for all R_1 values, the recorded RGC bandwidths are significantly lower than the modified RGC. Moreover, increasing



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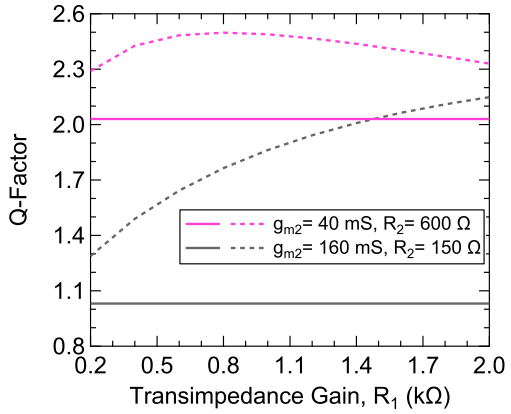

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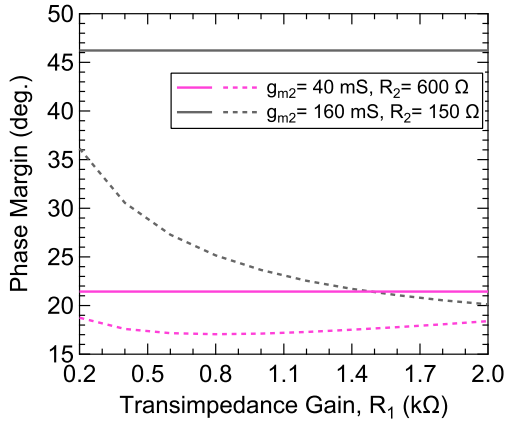


(c)

Figure 6.13: Performance comparison of RGC (dashed) versus the modified RGC (solid) as the transimpedance gain (R_1) increases at $A_{v2} = 24$ for different $g_{m2}R_2$ combinations (a) Bandwidth (b) Q-factor (c) Phase margin

R_1 results in a substantial reduction in the RGC bandwidth. Whereas, its bandwidth at 2 kΩ is approximately reduced by 220% compared to its value at 200 Ω. This substantial drop in the RGC bandwidth is mainly because its dominant $p_{(1,2)}$ is a function of R_1 as imposed by the Miller capacitance of $C_{\mu 1}$, as indicated by (6.10).

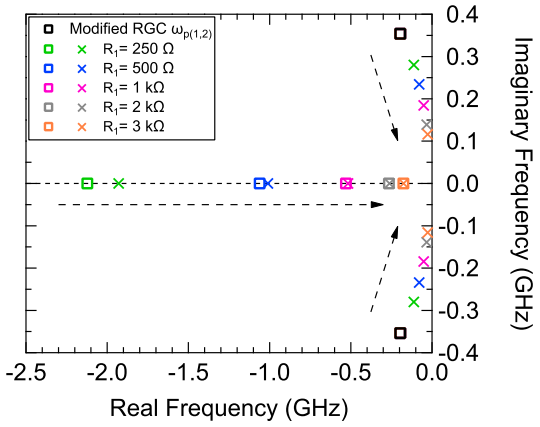
On the other hand, for Case 2 ($g_{m2} = 160$ mS and $R_2 = 150$ Ω), for all R_1 values, the bandwidth of the modified RGC is seen to be significantly higher than its bandwidth for Case 1. Such bandwidth improvement is a result of employing optimised values of g_{m2} and R_2 as discussed in Section 6.5.1. Nevertheless, despite the bandwidth enhancement, yet for Case 2, the bandwidth reduction of the modified RGC, as a result of increasing R_1, is relatively more significant when compared to Case 1. Such bandwidth behaviour is because the frequency of the dominant $p_{(1,2)}$ of the modified RGC is higher in comparison to Case 1, as indicated by the recorded higher bandwidths. Hence, the increased frequency of $p_{(1,2)}$ coupled with the simultaneous reduction in the frequency of p_3 results in narrower spacing between $p_{(1,2)}$ and p_3 in Case 2 Hence, making the effect of p_3 on the bandwidth of the modified RGC more obvious. Nevertheless, the bandwidth of the modified RGC in at 2 kΩ is only reduced 30% reduced from its value at 200 Ω, which is relatively small compared to the decade increase in gain. In contrast, increasing R_1 results in a substantial reduction in the bandwidth of the conventional RGC, of approximately 220%, which is again due to the bandwidth limitation imposed by the Miller capacitance of $C_{\mu 1}$. Yet, it is clear that the recorded RGC bandwidths for Case 2 is higher than Case 1, which is again due to the optimised values of g_{m2} and R_2 as discussed in Section 6.5.1.

As for the stability of the TIAs, Figure 6.13b shows their Q-factor versus increasing transimpedance gain (R_1) for the 2 cases of g_{m2} and R_2. Noticeably, for both Cases 1 and 2, the modified RGC is seen to have a constant Q-factor, irrespective of R_1. Where the recorded Q-factor is lower at Case 2, employing the optimised values of g_{m2} and R_2, which aligns with the results in Section 6.5.1, where it was concluded that low g_{m2} and high R_2 (as in Case 2) results in higher bandwidth and lower peaking. Low Q-factor translates to higher phases margin as

seen in Figure 6.13c, where the modified RGC has relatively low phase margin in case 1, with the high Q-factor, yet more acceptable phase margin (more than 45°) for Case 2 with the the low Q-factor, which in turn yields more stable operation. In contrast, increasing R_1 increases the RGC Q-factor for the 2 cases, which is a result of the increase in the Miller multiplier of $C_{\mu 1}$ (A_{v1}), as such the effect of C_{mi} on the Q-factor of the RGC is enhanced.

It is worth noting that the strictly constant behaviour of the Q-factor and phase margin of the modified RGC, irrespective of R_1, is only valid when considering $p_{(1,2)}$, since its independent of R_1. Nevertheless, such behaviour is not entirely accurate for high values of R_1, especially in Case 2, where the effect of p_3 becomes more significant. As such, the simplifying assumption of a second order transfer function at which the Q-factor is calculated becomes less accurate, since the interplay between $p_{(1,2)}$ and p_3 becomes more significant at high R_1. Therefore, at high R_1 (beyond 1 kΩ), the Q-factor is expected to slightly deviate from the recorded constant value. Nevertheless, the recorded constant value still gives a reasonable estimation of the Q-factor of the modified RGC.

The effects of increasing the transimpedance gain (R_1) on the two TIAs are further studied by plotting their respective pole action, on the s-plane, as illustrated in Figure 6.14a and Figure 6.14b at $g_{m1} = 40$ mS, $g_{m2} = 160$ mS and $R_2 = 150$ Ω (Case 2), while increasing R_1 from 250 Ω to 3 kΩ. Figure 6.14a shows the pole action of the two TIAs as R_1 increases, including $p_{(1,2)}$ and p_3 of each TIA, where the conventional RGC is denoted by the cross symbol and the modified RGC by the square symbol. First, it can be observed that increasing R_1 reduces the frequency of p_3 of the two TIAs. Yet, in the two cases, the frequencies of p_3 is mostly at significantly higher frequencies than $p_{(1,2)}$, except for high R_1 in the modified RGC case. Hence, in such cases, p_3 has almost negligible effect on the TIAs bandwidth. On the other hand, for the modified RGC, it can be seen that its $p_{(1,2)}$ (black square) is independent of the R_1 value as indicated in (6.26)-(6.28). Hence, since the bandwidth of the modified RGC is largely dictated by $p_{(1,2)}$, as such making its bandwidth nearly insensitive to increasing transimpedance gain,



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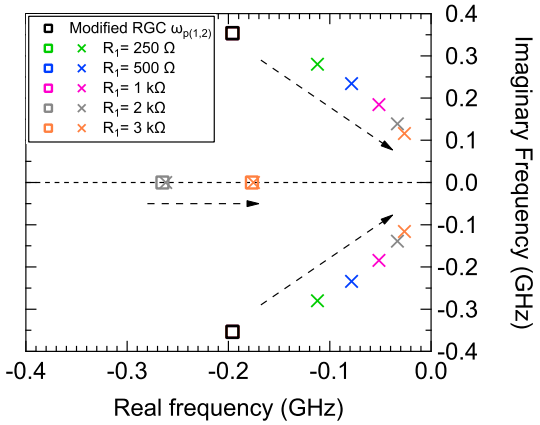


(b)

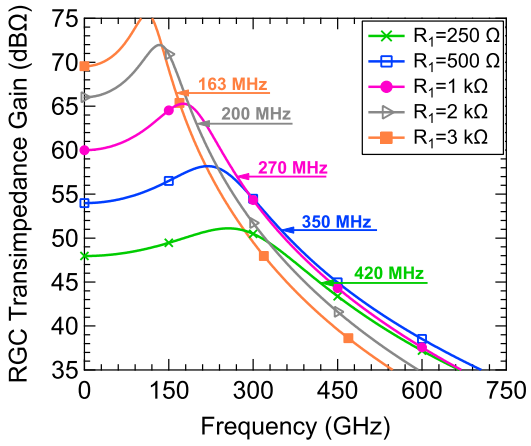
Figure 6.14: Simulations of the RGC (cross symbol) and modified RGC (square symbol) pole action for increasing R_1 at $g_{m1} = 40$ mS, $g_{m2} = 160$ mS and $R_2 = 150\ \Omega$ (a) Including $p_{(1,2)}$ and p_3 (b) Including $p_{(1,2)}$ and significant p_3

provided the frequency spacing between its $p_{(1,2)}$ and p_3 is sufficiently large. Moreover, it justifies the constant values of the Q-factor and phase margin observed in Figures 6.13b and 6.13c, respectively. Since, clearly $p_{(1,2)}$ of the modified RGC as described by its f_n and Q-factor. Nevertheless, for high R_1 (beyond 1 kΩ), the frequency spacing between $p_{(1,2)}$ and p_3 of the modified RGC becomes narrower, which in turn gradually switches the pole dominance to p_3, as such, its effect on the modified RGC bandwidth becomes more significant. Such behaviour is illustrated by Figure 6.14b, where it can be seen that for $R_1 = 2$ kΩ, the frequency of p_3 of the RGC is considerably close to its $p_{(1,2)}$. Whereas, at $R_1 = 3$ kΩ, the frequency of p_3 is even lower than $p_{(1,2)}$. Hence, the modified RGC bandwidth is now determined

by p_3 and hence, the observed reduction as R_1 increases as in Case 2 in Figure 6.13.

In contrast, for the conventional RGC, increasing R_1 pushes its $p_{(1,2)}$ (cross symbol) to the unstable region of the s-plane as indicated by the arrow, which aligns with the observed reduction in its phase margin in Figure 6.13c. In addition to, increasing R_1 reduces the distance between $p_{(1,2)}$ of the RGC and the real axis, which demonstrates the reduction in its f_n and in turn its bandwidth as observed in Figure 6.13. Hence, it can be concluded that increasing the transimpedance gain (R_1) of the RGC significantly deteriorates both its bandwidth and stability performance, which is as a result in the increase in the Miller effect of $C_{\mu 1}$.

The behaviour of the pole action of the two TIAs as the transimpedance gain (R_1) increases is illustrated by the corresponding transimpedance gain responses for each R_1 value as shown by Figures 6.15a and 6.15b. From Figure 6.15a, the bandwidth of the RGC drops by approximately 260% as the transimpedance gain increases from 250 Ω (48 dBΩ) to 3 kΩ (69.5 dBΩ). This substantial drop in bandwidth is mainly because its dominant $p_{(1,2)}$ is a function of R_1 as imposed by the Miller capacitance C_{mi} of $C_{\mu 1}$, as indicated by (6.10). In other words, increasing R_1 has the direct effect of increasing the Miller multiplier $g_{m1}R_1$ of $C_{\mu 1}$, hence reducing the frequency of f_n and in turn the frequency of the dominant $p_{(1,2)}$ dictating the RGC bandwidth, as seen in Figure 6.14a. Therefore, imposing a stringent trade-off between its bandwidth and transimpedance gain. In contrast, in Figure 6.15b, the modified RGC exhibits bandwidth behaviour that is almost independent of its transimpedance gain up to $R_1 = 1$ kΩ, which confirms the bandwidth advantage of ameliorating the inherent Miller capacitance C_{mi} of the conventional RGC as suggested by the mathematical analysis conducted in Section 6.4.1. Beyond $R_1 =$ 1 kΩ, the modified RGC bandwidth is reduced due to the reduction in the frequency of its p_3 as illustrated in Figure 6.14a. Nevertheless, even at such high R_1, the bandwidth of the modified RGC is higher than the conventional RGC. Hence, based on the above studies, it can be concluded that the modified RGC offers a significant improvement in both the bandwidth and transimpedance gain compared to the conventional design, where its bandwidth is almost independent of its transimpedance



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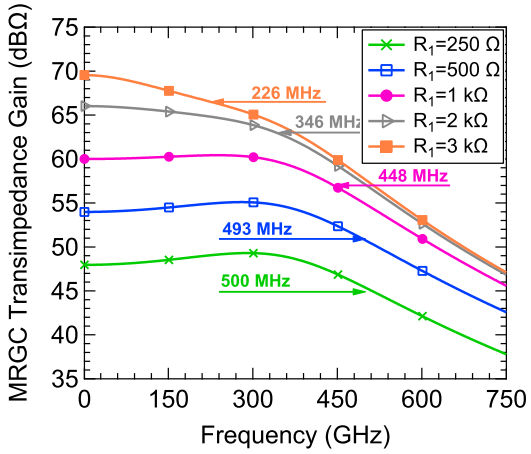


(b)

Figure 6.15: Simulations the transimpedance gain frequency responses for increasing R_1 at $g_{m1} = 40$ mS, $g_{m2} = 160$ mS and $R_2 = 150$ Ω (a) RGC (b) Modified RGC

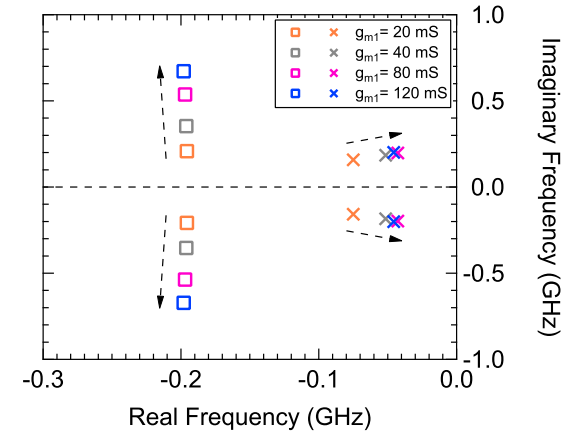
gain. Such advantage is a result of neutralising the Miller effect of $C_{\mu 1}$.

Another advantage of neutralising the Miller effect of $C_{\mu 1}$ is allowing for more effective bandwidth enhancement via g_{m1}. As previously discussed in Section 6.3.2, in the RGC TIA, increasing g_{m1} reduces the input resistance, yet its also increases the Miller capacitance C_{mi}, which counteracts the advantage of reducing the input resistance and leads to limited bandwidth enhancement and significant levels of peaking as illustrated in Figure 6.8b. On the other hand, such limitations are eliminated with modified RGC TIA, where increasing g_{m1} results in substantial bandwidth enhancement. The effect of increasing g_{m1} on the two TIAs is illustrated

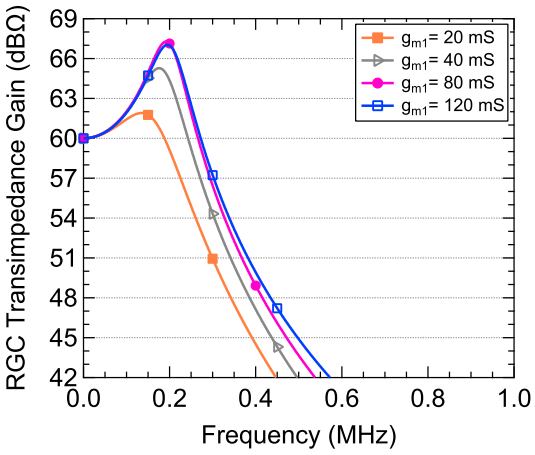
by their pole action and the corresponding transimpedance gain responses at $R_1 =$ 1 kΩ, $g_{m2} = 160$ mS, $R_2 = 150\ \Omega$, while g_{m1} is increased from 20 mS to 120 mS.

Figure 6.16a shows the pole action of the two TIAs as g_{m1} increases, including only $p_{(1,2)}$ of each TIA, since at $R_1 = 1$ kΩ, the effect of p_3 is largely insignificant. For the RGC TIA (denoted by the cross symbol), increasing g_{m1} pushes its $p_{(1,2)}$ towards the unstable region of the s-plane. Moreover, it results in minimal bandwidth enhancement as indicated by the increase in the distance between $p_{(1,2)}$ and the real axis (this distance demonstrates damped f_n). In contrast, for the modified RGC (denoted by the square symbol), increasing g_{m1} leads to significant bandwidth enhancement, as indicated by the increase in the distance between its $p_{(1,2)}$ and the real axis. Moreover, it is clear that $p_{(1,2)}$ of the modified RGC sits at much higher frequencies in comparison to the $p_{(1,2)}$ of the conventional RGC, which indicates the improvement in the TIA stability.

The behaviour of the two TIAs observed from their pole action as g_{m1} is increased can be clearly appreciated from their corresponding transimpedance gain responses for each g_{m1} value as shown by Figures 6.16b and 6.16c. From Figure 6.16b, for the RGC, increasing g_{m1} leads to a limited bandwidth enhancement and significant increase in the peaking amplitude of approximately 8 dB. In contrast, for the modified RGC, increasing g_{m1} leads to significant bandwidth enhancement of nearly 4 times as g_{m1} is increased from $g_{m1} = 20$ mS to 120 mS, with moderate peaking of only 2 dB. Hence, it can be concluded that increasing g_{m1} leads to more effective bandwidth enhancement of the modified RGC compared to the conventional design. Such advantage is a result of the amelioration of the Miller capacitance of $C_{\mu 1}$, which increase the frequency of the dominant $p_{(1,2)}$. Noting that increasing g_{m1} for the RGC and modified RGC TIAs is generally undesirable, especially in low power designs, since as discussed in Section 6.3.2, increasing g_{m1} increases the voltage drop across R_1, which mandates higher V_{CC} to maintain the bias of Q_1 and in the case of the modified RGC Q_1 and Q_3. Nevertheless, the bandwidth advantage obtained via increasing g_{m1} in the modified RGC case renders an additional degree of freedom for the designer where increasing g_{m1} is acceptable.



(a)



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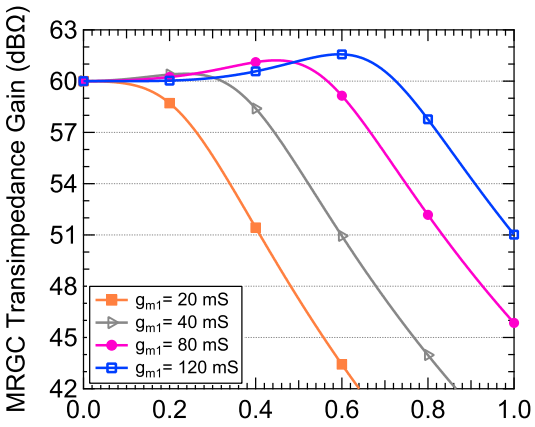
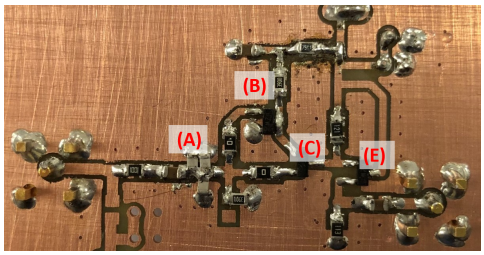
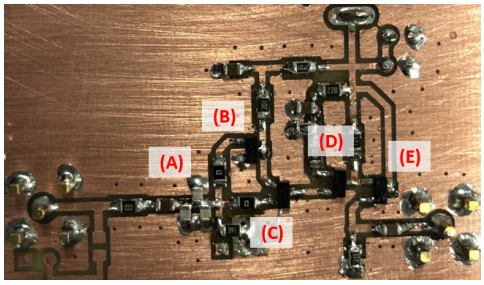


(c)

Figure 6.16: The effect of increasing g_{m1} on the modified RGC versus the conventional RGC TIA at $R_1 = 1$ kΩ, $g_{m2} = 160$ mS and $R_2 = 150$ Ω (a) pole action of the two TIAs (b) RGC Transimpedance gain (b) Modified RGC Transimpedance gain



(a)



(b)

Figure 6.17: Fabricated PCBs (a) RGC TIA (b) Modified RGC TIA, where (A) Photodiode capacitance (B) CE (Q_2) stage (C) CB (Q_1) stage (D) CB (Q_3) stage (E) Additional CC stage

6.6 TIAs Verification & Measurements

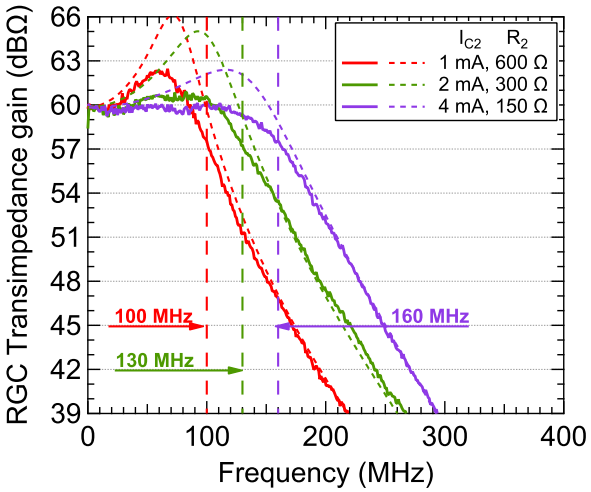
Using discrete components, the two TIAs followed by a CC stage (output buffer) were built and tested. The CC stage is designed to provide 50 Ω output matching. It is worth noting that having an output buffer stage is necessary to isolate the output of the TIAs from any external parasitic capacitances that might interfere with their responses and provide 50 Ω output impedance. Moreover, the CC stage presents a significantly high input impedance and a voltage gain close to 1. Hence, in theory, the addition of the CC stage should not result in any loading of either the RGC or modified RGC TIAs; as such, the additional CC stage has minimal effect on the performance of the TIAs, as verified in simulations. Figures 6.17b and 6.17b show the fabricated FR4 double-sided PCB of the modified RGC and modified RGC TIAs, respectively. The PCBs are populated using silicon NPN transistors BFU520A ($f_T = 10$ GHz) and with surface mount devices (SMD) including for all resistors and capacitors. The two TIAs were measured at a fixed $V_{CC} = 9$ V.

To test the TIAs performance, first, the scattering parameters of the fabricated RGC and modified RGC TIA are measured using a VNA. These are then converted into corresponding impedance parameters to obtain the transimpedance gain responses. To facilitate the measurements, the photodiode is replaced a series 1 kΩ resistor to convert the VNA voltage into current, analogous to the photodiode current and its C_{pd} is replaced by a shunt input capacitance equals 300 pF. The measured results are compared to simulation results, where the simulated results are based on post PCB layout. The simulation considers the effect of a) PCB parasitic effects b) input transmission lines c) input capacitor models. Noting that the parasitic effects of the PCB tracks, except for the input transmission lines connecting C_{pd} to the TIA, were found to be insignificant.

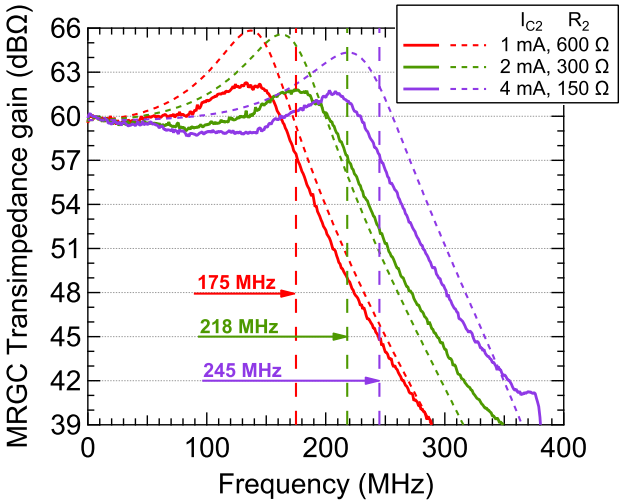
Noting that using such large values of surface mount capacitors to represent the photodiode capacitance imposes a severe limitation in demonstrating the full bandwidth advantage of the modified RGC in measurements. This is because of the low self-resonance frequency associated with such high values of capacitances. Such low self-resonance frequency interferes with the amplifier frequency response, limiting the demonstrated bandwidth enhancement that the modified RGC could achieve. Nevertheless, such measurement limitation is not prevalent if the modified RGC TIA were to be optically measured with a large-area photodiode. Even so, the following set of measurements shows the advantage of the modified RGC over the conventional design.

6.6.1 Verification of the Effect of R_{in} on Bandwidth

Studies of the RGC and modified RGC input impedance frequency behaviour concluded that increasing the voltage gain A_{v2} of the CE stage leads to substantial reduction in the DC input resistance. Nevertheless, it was shown that achieving low input resistance is not sufficient to obtain optimum bandwidth performance. This is due to the complex nature of the input dominant pole $p_{(1,2)}$. As such, when reducing the input resistance, it is essential to optimise the the values of the CE voltage gain determinants: g_{m2} and R_2 to obtain higher bandwidths. It was shown that the product of high g_{m2} and low R_2 results in significantly higher bandwidth and better



(a)



(b)

Figure 6.18: Measured (solid) and simulated (dashed) frequency responses for varying I_{C2} and R_2 at $C_{pd} = 300$ pF, $R_1 = 1$ kΩ and $I_{C1} = 1$ mA (a) RGC TIA (b) Modified RGC TIA

frequency behaviour than the product of low g_{m2} and high R_2. This is because high values of R_2 leads to reduction in the frequency of f_n and higher Q.

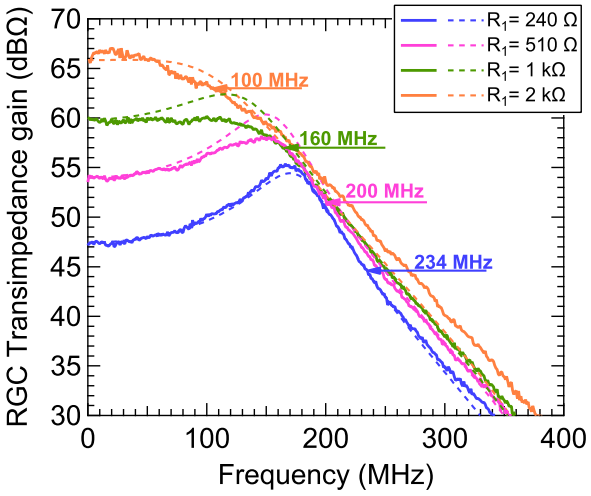
The effect of the choice of g_{m2} and R_2 on the TIAs bandwidth is verified through measurements of the frequency responses at a fixed $I_{C1} = 1$ mA and transimpedance gain equals 1 kΩ for 3 different combinations of I_{C2} and R_2, each combination maintains $A_{v2} = 24$. Maintaining A_{v2} ensures fixed R_{in} for all cases. Figure 6.18a and 6.18b shows the measured and simulated transimpedance gain re-

sponses of the RGC and modified RGC for each respective I_{C2} and R_2 combination. It can be seen that measurements are in good agreement with simulations. Noticeably, the two TIAs exhibits similar behaviour, where the bandwidth increases by approximately 60% as a result of progressively increasing I_{C2} and reducing R_2, as predicted by analysis in Section 6.5.1. Yet, noting that the respective bandwidth for each I_{C2} and R_2 case is higher for the modified RGC. This considerable increase in bandwidth between the case of low I_{C2} and high R_2 and the case of high g_{m2} and low R_2, is primarily due to the reduced frequency-dependence of the voltage gain and impedance responses of the two TIAs, rather than reduction in the DC resistance R_{in} as was shown by Figures 6.12. Such improvement in the frequency behaviour of the TIAs is due to reducing R_2, which has the direct result of increasing f_n and in turn the frequency of $p_{(1,2)}$ for the two TIAs as indicated by (6.10) and (6.26). Nevertheless, increasing I_{C2} and reducing R_2 can potentially degrade the noise performance as a result of the increase in the associated shot and thermal noise due to I_{C2} and R_2, respectively. Therefore, imposing a trade-off between bandwidth and noise performance.

6.6.2 Bandwidth versus gain of the RGC & Modified RGC

To demonstrate the bandwidth insensitivity of the modified RGC to transimpedance gain variations in comparison to the conventional RGC. The transimpedance gain responses of the two TIAs is measured while increasing R_1 in the range of 240 Ω to 2 kΩ. Recalling, the transimpedance gain of the two TIAs equals R_1 as given by (6.9). Figure 6.19 show the measured and simulated transimpedance gain responses of the RGC and modified RGC for each respective DC transimpedance gain at a fixed $C_{pd} = 300$ pF, $I_{C1} = 1$ mA and $I_{C2} = 4$ mA and $R_2 = 150$ Ω.

From Figure 6.19a, it can be seen that measurements are in a good agreement with simulations. Moreover, it can be clearly seen that the bandwidth of the RGC drops by 240% as the transimpedance gain is increased from 240 Ω (47.6 dBΩ) to 2 kΩ (66 dBΩ). This substantial drop in bandwidth is mainly because its dominant input pole $p_{(1,2)}$ is a function of R_1 as imposed by the Miller capacitance C_{mi} associated with $C_{\mu 1}$, as indicated by (6.10). In other words, increasing R_1 has the direct ef-



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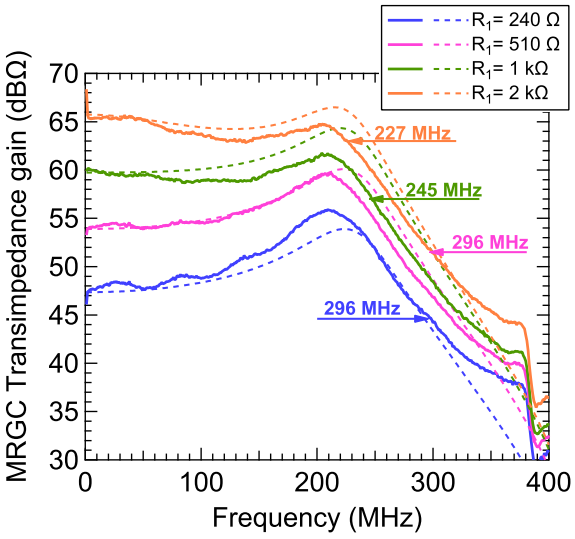


(b)

Figure 6.19: Measured (solid) and simulated (dashed) frequency responses for varying transimpedance gain at $C_{pd} = 300$ pF, $I_{C1} = 1$ mA, $I_{C2} = 4$ mA and $R_2 = 150\ \Omega$ (a) RGC TIA (b) Modified RGC TIA

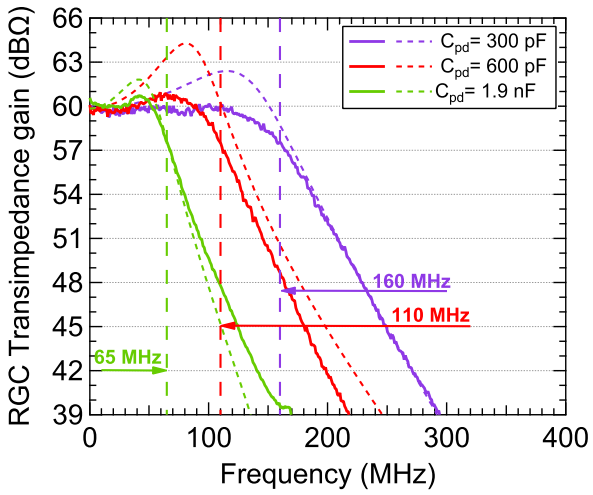
fect of increasing the Miller multiplier $g_{m1}R_1$ of $C_{\mu 1}$, hence reducing the frequency of f_n and in turn the frequency of the dominant $p_{(1,2)}$ dictating the RGC bandwidth. Therefore, imposing a trade-off between bandwidth and transimpedance gain. It is worth noting that similar bandwidth-limiting effects were observed when attempting to enhance the RGC bandwidth by reducing the input resistance via increasing g_{m1}, which in turn increase C_{mi}. Hence, limiting the RGC achievable bandwidth extension. Nevertheless, such effects are not shown, since as previously discussed,

increasing g_{m1} is generally not preferable as it could potentially limit the achievable transimpedance gain, due to associated increase in the voltage drop across R_1, hence requiring higher voltage supplies V_{CC} in order to maintain the bias conditions for Q_1. Nevertheless, the effects of increasing g_{m1} were studied in detail in Section 6.5.2.

In contrast to the behaviour observed for the modified RGC TIA shown in Figure 6.19b, where clearly the TIA exhibits bandwidth behaviour that is almost independent of its transimpedance gain, which confirms the bandwidth advantage of ameliorating the inherent Miller capacitance C_{mi} of the conventional RGC as suggested by the mathematical analysis conducted in Section 6.4.1. The bandwidth reduction of the modified RGC, as a result of increasing its transimpedance gain by almost one order of magnitude from 240 Ω to 2 kΩ, is approximately 30%, which is almost negligible in comparison to the substantial increase in the transimpedance gain. Therefore, it can be concluded that the modified RGC offers substantial bandwidth enhancement in comparison to the conventional RGC design, especially at high transimpedance gains as a result of neutralising the Miller effect of $C_{\mu 1}$. In addition to, having insensitive bandwidth performance with increasing transimpedance gain, which is particularly valuable in the application of VLC, where high gain and bandwidth are of utmost importance. Notwithstanding, such behaviour is only maintained to an extent where the output pole p_3 is sufficiently higher than $p_{(1,2)}$. Recalling, p_3 is a function of R_1 as given by (6.29), which dictates the transimpedance gain. Hence, in such case attempting to increase the transimpedance gain (beyond 2 kΩ in the examples used in this work) would result in gradual reduction in the bandwidth performance, since the frequency of p_3 becomes closer to the frequency of $p_{(1,2)}$ and therefore, would have considerable impact on the bandwidth performance.

6.6.3 Bandwidth versus C_{pd} of the RGC & Modified RGC

The bandwidth tolerance of the two TIAs to increasing C_{pd} is examined by measuring the frequency responses at transimpedance gain set to 1 kΩ (60 dBΩ) as shown by Figure 6.20. Noting that the two TIAs were measured for a wide range of C_{pd}, where the modified RGC showed bandwidth advantage compared to the conventional RGC. Nevertheless, the performance of the two TIAs are shown for these particular values of C_{pd}, since they are fairly close to C_{pd} values in the datasheets



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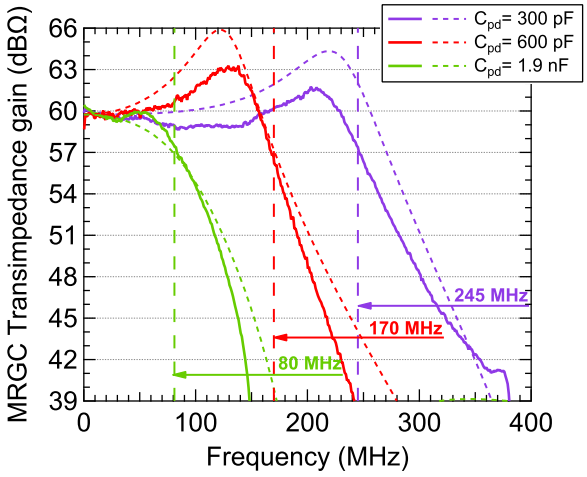


(b)

Figure 6.20: Measured (solid) and simulated (dashed) frequency responses for varying C_{pd} at $R_1 = 1$ kΩ, $R_2 = 150$ Ω, $I_{C1} = 1$ mA and $I_{C2} = 4$ mA (a) RGC TIA (b) Modified RGC TIA

of the photodiodes to be tested in Chapter 7.

From Figure 6.20a, it can be seen that the RGC maintains remarkable bandwidth tolerance against C_{pd}, where increasing C_{pd} by more than 6 times from 300 pF to 1.9 nF results in a bandwidth drop of only 2.5 times. Whereas, for the modified RGC case shown by Figure 6.20b, the bandwidth tolerance against C_{pd} is significantly improved, where for each respective C_{pd} value, the bandwidth is extended by approximately 150%, except for $C_{pd} = 1.9$ nF where the bandwidth enhancement is relatively lower, which is attributed to the dominating effect of such exceptionally large C_{pd}, which slightly limits the bandwidth gains as a result of the amelioration of the Miller capacitance of $C_{\mu 1}$. Nevertheless, it is worth noting that the obtained bandwidth advantage from the modified RGC is at the expense of slightly enhanced peaking amplitudes.

Hence, it can be concluded that the modified RGC results in a substantial improvement in bandwidth compared to the conventional design even for ultra-high C_{pd} (nano-Farads). Such bandwidth improvement is even more appreciable when compared to a traditional 50 Ω amplifier, which would offer bandwidths of only 10.6 MHz, 5.3 MHz and 1.7 MHz for $C_{pd} = 300$ pF, 600 pF and 1.9 nF, respectively. As such, employing the modified RGC results in remarkable improvement in bandwidth, which would significantly improve the utility of such large-area photodiodes in the application of VLC systems and may have other applications where high input capacitance current source input devices are encountered.

6.7 Discussion & Conclusions

This chapter has described studies of the performance of the low input RGC TIA with ultra-high C_{pd}. Analysis of the RGC at high C_{pd} showed that the complex nature of its dominant pole $p_{(1,2)}$ necessitates careful design optimisation to achieve optimal performance in terms of bandwidth, transimpedance gain and stability. Furthermore, mathematical and analytical analysis of the RGC has led to the identification the of internal Miller capacitance presented by $C_{\mu 1}$ of the CB stage as a major limitation on bandwidth and transimpedance gain. Therefore, a modification of the RGC has been proposed to eliminate this undesirable Miller capacitance effect. Through mathematical analysis and full circuit simulations, it was shown that by introducing a cascode stage, substantial improvement in bandwidth and transimpedance gain could be realised. Moreover, the newly proposed modified RGC exhibits an almost insensitive bandwidth performance to changes in transimpedance gain. Nevertheless, it is important to note that the bandwidth enhancement might be accompanied by a slight increase in the peaking amplitude, which necessitates careful design optimisations.

The performance of the two TIAs was experimentally verified through measurements of the scattering parameters of two circuits constructed using discrete components on two PCBs. Experimental results show the advantage of the new design where the bandwidth is nearly doubled relative to the traditional RGC and where the gain of the modified circuit can be increased by up to 18 dB with less than 20% loss in bandwidth. Bandwidth of 245 MHz was measured when a 300 pF capacitance was used at the input of the TIA and for an overall transimpedance gain equals 1 kΩ; which is, to the best of the author's knowledge, the widest band ever reported at such high input capacitance. Overall the new design's merits will be advantageous in the application of large transmission distance VLC link, where large-area photodiodes are required to collect enough optical signal whose photocurrent, in turn, requires higher levels of amplification to generate reasonable SNR levels for appropriate signal detection.

Chapter 7

Low Impedance Amplifiers for Large-Area Photodiode Receivers

7.1 Introduction

This chapter describes the application of the low input impedance RGC TIA to large-area photodiodes. The RGC TIA is tested within a VLC link employing commercially available silicon photodiodes of different areas and manufacturers. The bandwidth performance is evaluated by measuring the scattering parameters of the VLC link with the RGC TIA versus a 50 Ω impedance termination. Test results show a significant bandwidth extension of up to 1000% compared to the 50 Ω impedance counterpart. Despite, the remarkable bandwidth enhancement, the bandwidths obtained from the S_{21} when employing the RGC TIA showed significant departure from the predictions of measurements of the RGC TIA with the respective photodiode equivalent capacitances, in Chapter 6. This motivated an investigation into viable reasons for the shortfall in the measured bandwidths. Therefore, the author undertook several checks to ensure that the test transmitter did not affect the integrity of the receiver's measurements. Moreover, the RGC PCB was thoroughly tested to ensure it is well-functioning, as verified in Section 6.6, until it was found that the reason for the bandwidth shortfall stems from the photodiodes itself. As it was identified that the photodiodes present a resistance that comes in series between the capacitance of the photodiode and the TIA, hence, adding to the input

resistance of the TIA and, in turn, inflicting an additional bandwidth-limiting factor for VLC receivers. The presence of such series resistance of the photodiode is admittedly recognised, yet is generally overlooked by circuit designers, based on being insignificant in determining the receiver's bandwidth.

In this chapter, the photodiode series resistance is identified as a major contributor to the bandwidth limitation, especially when employing a combination of a large-area photodiode and low input impedance TIA. In this chapter, such contribution is verified and supported through modelling and parameter extraction of each of the photodiodes under test. The photodiode modelling and parameter extraction are based on return loss measurements, from which impedance responses were obtained for model fitting. Consequently, a full photodiode model is identified, which faithfully mimics measurements of each photodiode frequency response. Importantly, the derived full photodiode model and parameter extraction confirmed the bandwidth limitation of the photodiode series resistance.

Finally, the chapter describes a preliminary proposal of a circuit technique to combat the unforeseeable bandwidth limitation imposed by the photodiode series resistance. The technique is based on the introduction of negative resistance in series between the photodiode and the RGC TIA, to neutralise the bandwidth-limiting effect of the photodiode series resistance. The negative resistance is generated using the Linvill NIC circuit described in Chapter 2. Studies of the newly proposed technique showed that the bandwidth-limiting effect of the photodiode series resistance could be alleviated, so that the bandwidth advantage of the RGC/modified RGC TIAs is fully realised[1].

[1]The work on the amelioration of the photodiode series resistance by utilising the Linvill NIC is still under investigation, however, some preliminary measurements and testing of the generation of the negative resistance were carried and is included in an Appendix.

7.2 Optical Link Measurements with the Large-Area Photodiodes

This section demonstrates the application of the RGC TIA to four commercially available silicon PIN photodiodes, of different areas and from two manufacturers to examine its bandwidth extension advantage compared to a traditional 50 Ω impedance. Two of the photodiodes under test are manufactured by OSI Optoelectronics: PIN10-D and PIN25-D of areas 100 mm^2 and 600 mm^2, respectively. Whereas the other two photodiodes are manufactured by Centronic: OSD50-E and OSD100-E of areas 50 mm^2 and 100 mm^2, respectively. The four photodiodes under test are shown in Figure 7.1. The performance of each of the photodiodes is tested independently when connected to a 50 Ω load versus the RGC TIA using the simple experimental test set-up shown in Figure 7.2.

7.2.1 Experimental Set-up

The set-up consists of a PL405 commercial blue laser diode, the large-area photodiode and the RGC TIA circuit built on PCB. The laser diode is biased using a Mini-Circuit (ZFBT-4R2GWFT+) bias-T and is driven using port 1 of the VNA. A short free-space optical channel of a fixed distance connects the laser's output to the optical receiver assembly. Traditionally, photodiodes are biased by applying a bias voltage V_B to the cathode and then DC-couple the anode to the TIA. Thus

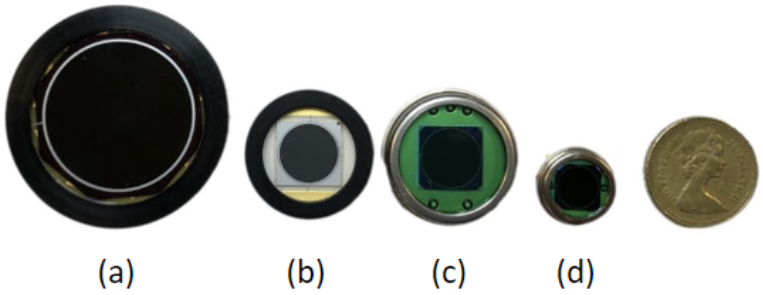


Figure 7.1: Photodiodes under-test (a) OSI Optoelectronics PIN25-D (600 mm^2) (b) OSI Optoelectronics PIN10-D (100 mm^2) (c) Centronic OSD100-E (100 mm^2) (d) Centronic OSD50-E (50 mm^2)

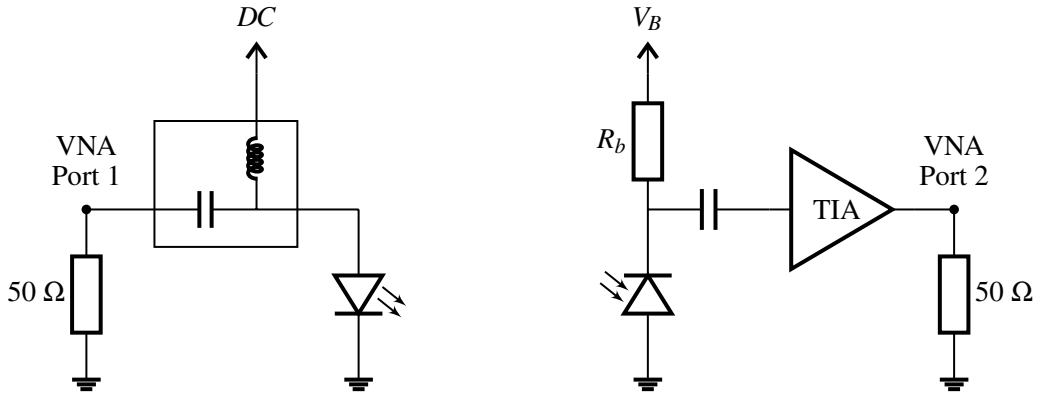


Figure 7.2: Experimental set-up used to test the large-area photodiode with the RGC TIA

applying a fixed reverse bias voltage across the photodiode with no bias resistors, to avoid added thermal noise. Nevertheless, in the set-up in Figure 7.2, each of the photodiodes under test is reverse-biased by grounding the anode and applying V_B to the cathode through a bias resistor R_b. The cathode is AC-coupled to the RGC TIA, and port 2 of VNA monitors the receiver's output. The photodiodes are biased in such a way because of the way they are physically packaged. R_b is set to be 1 kΩ.

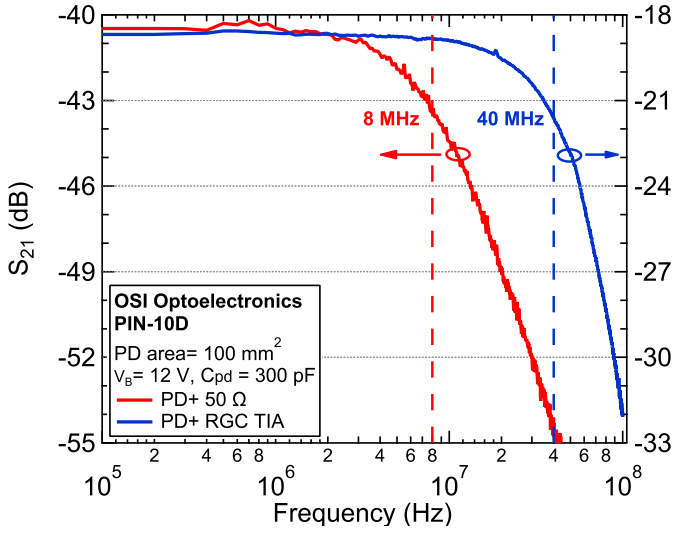
Noting that in this experiment, using LEDs to measure the performance of the optical receiver assembly would not be suitable, since the bandwidth of commercially available LEDs ranging from sub-MHz to tens of MHz is not sufficient for the desirable receiver measurements, since measurements of the RGC/modified RGC TIAs based on the photodiode equivalent capacitance in Section 6.6 predicts bandwidths over 100 MHz. Therefore, laser diodes are a more suitable light source, since their cut-off-frequencies range from hundreds of MHz to GHz. Prior to measurements of the large-area photodiode, the laser diode S_{21} response was measured at different bias currents using a 2 GHz Thorlabs silicon photodiode. The bandwidth of the laser diode was verified to be approximately 2 GHz at $I_f = 35$ mA, which is well above the predicted bandwidths of the receiver assembly, including the large-area photodiode and the RGC/modified RGC TIAs. Hence, the S_{21} measurements of the overall link would accurately reflect the receiver performance only.

Furthermore, the experiment is conducted with no focusing lens at either the transmitter or the receiver, unlike the VLC link in Chapter 4, which was constructed

to test the negative capacitance circuit with the LEDs. Such VLC link used focusing lens both at the transmitter and the receiver, where the receiver employed the 2 GHz Thorlab photodiode (250 μm) followed by a 10 kΩ TIA. Hence, enabling the reader to appreciate the advantage of using large-area photodiode in terms of the substantial increase in the received optical power. Such advantage is demonstrated by the difference in the S_{21} gains between the VLC link employing a receiver based on a small area photodiode, focusing lens and 10 kΩ TIA (Chapter 4) versus the receiver employing large-area photodiode, no focusing lens and 1 kΩ RGC TIA, where for each of the large-area photodiodes used, the S_{21} gain is either comparable or even larger than the S_{21} gain in the VLC link of Chapter 4. Moreover, despite using a different transmitter in each link (blue LED versus blue laser), the two links have similar channel length, and the VLC link in Chapter 4 employs higher gain TIA than the RGC TIA (10 kΩ versus 1 kΩ), which puts the two links at equal footing for comparison.

7.2.2 Measurements of the RGC TIA

The bandwidth performance of the receiver is examined by reverse-biasing each of the photodiodes at $V_B = 12$ V, which according to their respective datasheet should result in $C_{pd} = 300$ pF and 1.8 nF for the PIN10-D (100 mm^2) and PIN25-D (600 mm^2) and $C_{pd} = 270$ pF and 520 pF for the OSD50-E (50 mm^2) and OSD100-E (100 mm^2), respectively. Whereas, the RGC TIA is tested at a transimpedance gain of 1 kΩ and is biased so that the input resistance is approximately 1 Ω by setting $I_{C1} = 1$ mA, $I_{C2} = 4$ mA and $R_2 = 150$ Ω. According to the frequency response measurements of the TIAs with the photodiode equivalent capacitance in Section 6.6, it is predicted that at 1 kΩ for $C_{pd} = 300$ pF, the RGC/modified RGC TIAs should offer bandwidths of 160 MHz and 245 MHz, respectively. Whereas, for $C_{pd} = 600$ pF, the RGC/modified RGC TIAs should offer bandwidths of 110 MHz and 170 MHz and for $C_{pd} = 1.9$ nF the RGC/modified RGC should offer bandwidths of 65 MHz and 80 MHz, respectively. Although, the bandwidth predictions in Section 6.6 are based on exact capacitances that are also slightly higher than the photodiode capacitances from the datasheets, it was thought that these predictions



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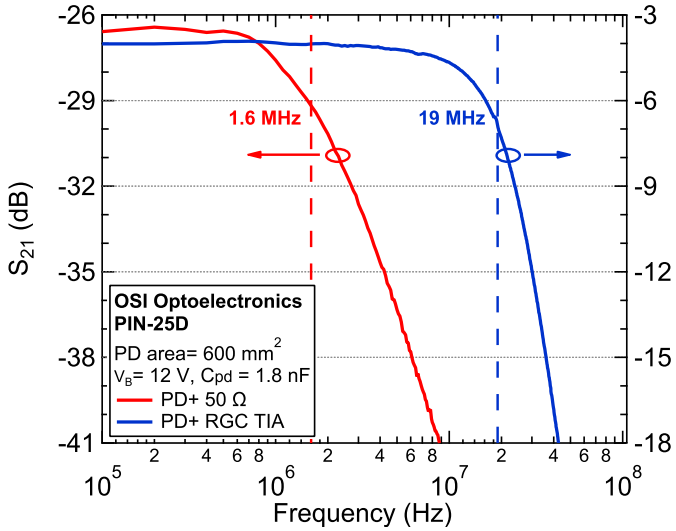


(b)

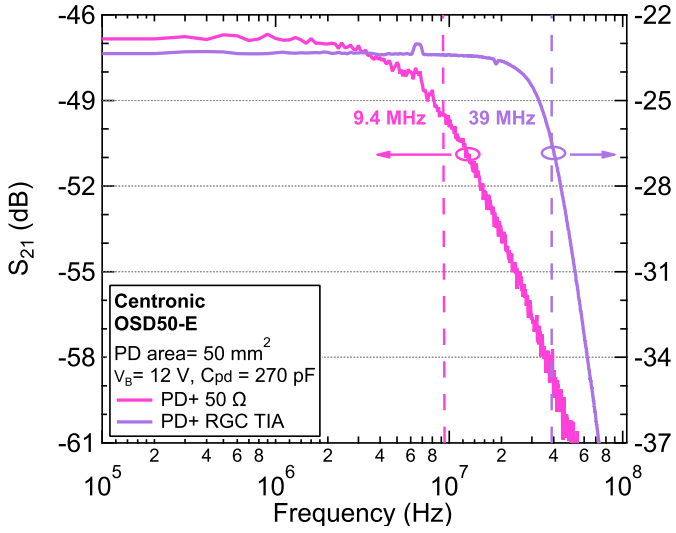
Figure 7.3: Measured S_{21} responses of the OSI optoelectronics photodiode when connected to a 50 Ω impedance versus the RGC TIA (a) 100 mm^2 (b) 600 mm^2

should still offer a reasonable approximation of the S_{21} bandwidths.

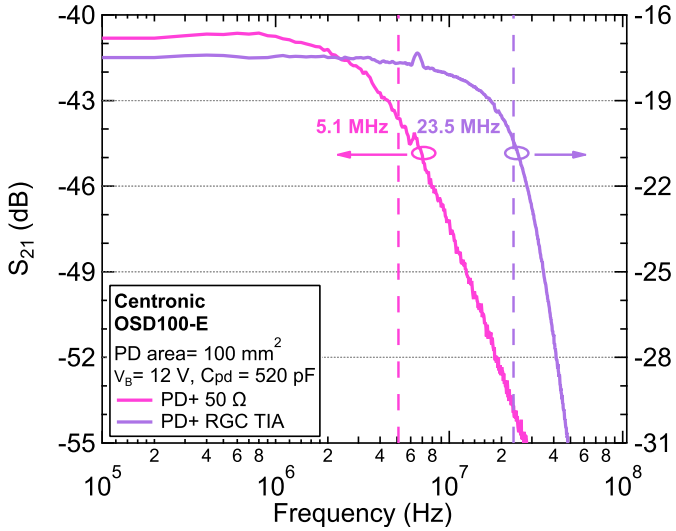
The electro-optical response of each of the photodiodes is measured independently and with the application of the RGC TIA, based on S_{21} measurements of the optical link shown in Figure 7.2. Figures 7.3a and 7.3b show the measured S_{21} responses of the PIN10-D (100 mm^2) and PIN25-D (600 mm^2) when connected to a 50 Ω versus the RGC TIA, respectively. The figures indicate the gain advantage of the RGC by having two y-axes. From Figure 7.3a, when connecting the photodiode

to a 50 Ω, the bandwidth is largely determined by an RC time constant associated with the 50 Ω and the photodiode capacitance that approximates to 300 pF and hence, the cut-off-frequency is 8 MHz. Similar behaviour is observed in Figure 7.3b, where the bandwidth of the photodiode-50 Ω combination is determined by their RC time constant ($C_{pd} = 1.8$ nF), as given by the 1.6 MHz. Interestingly, in such cases, the photodiode area is increased by 6 times (from 100 mm^2 to 600 mm^2), leading to a 6 times increase in their respective capacitances. The observed bandwidth reduction is approximately 5 times; slightly lower than expected.

On the other hand, when inspecting the S_{21} for each of the photodiodes when connected to the RGC TIA, it is clear that the RGC results in substantial bandwidth enhancement compared to the 50 Ω, of approximately five-fold and twelve-fold for the PIN10-D (100 mm^2) and the PIN25-D (600 mm^2), respectively. This significant bandwidth enhancement results from the extremely low input resistance of the RGC TIA, which pushes the frequency of the dominant input pole to higher frequencies. Moreover, the RGC does not follow the same relation between the bandwidth and photodiode capacitance (area), as in the 50 Ω impedance case. Meaning that increasing the photodiode area by 6 times did not result in 6 times the reduction in the bandwidth (only 2 times), despite the 6 times increase in the photodiode capacitance. Such behaviour results from the complex nature of the RGC dominant input pole, which warrants the TIA high tolerance to exceptionally high photodiode capacitances. Yet, interestingly the frequency responses exhibit some other unforeseeable behaviour, which defies both the TIA simulations and measurements. First, the application of the RGC TIA is more effective in extending the bandwidth of the PIN25-D (600 mm^2) over the PIN10-D (100 mm^2), despite its significantly higher capacitance. Second, the measured S_{21} (electro-optical) response shows a significant departure from what was predicted from the measured transimpedance gain responses of the RGC TIA with the photodiode equivalent capacitance in Section 6.6; the bandwidths obtained from optical measurements are a fraction of their electrical equivalent counterpart; 25% for the PIN10-D (100 mm^2) and 30% for the PIN25-D (600 mm^2) as shown in Figure 6.20a. This led the author to speculate



(a)



(b)

Figure 7.4: Measured S_{21} responses of the Centronic photodiode when connected to a 50 Ω impedance versus the RGC TIA (a) 50 mm^2 (b) 100 mm^2

the presence of other additional bandwidth-limiting factors imposed by the photodiodes; i.e other than its capacitance. Such speculation was further accentuated by the S_{21} measurements of the Centronic photodiodes shown in Figures 7.4a and 7.4b, which again exhibited some frequency behaviour discrepancies that were not predicted by the simulations and measurements of the RGC with their respective photodiode equivalent capacitances.

Figures 7.4a and 7.4b show the measured S_{21} responses of the OSD50-E

(50 mm^2) and OSD100-E (100 mm^2), when connected to a 50 Ω versus the RGC TIA, respectively. Again, the S_{21} responses of the photodiode displays similar behaviour to that of the OSI photodiodes: i) When connected to the 50 Ω, the response follows the conventional area-bandwidth relation, where doubling the photodiode area approximately halves the bandwidth as a result of doubling the photodiode capacitance; ii) In comparison to the 50 Ω, the application of the RGC results in significant bandwidth enhancement of approximately four-fold and five-fold for OSD50-E (50 mm^2) and OSD100-E (100 mm^2), respectively. Again, such bandwidth enhancement is mainly due to the ultra-low input resistance of the RGC TIA. Yet, again the recorded bandwidths displays a significant gap compared to the predictions of the TIA measurements with their respective equivalent capacitances in Figure 6.20a iii) When comparing the responses obtained in such cases to the OSI Optoelectronics photodiode cases in Figures 7.3a and 7.3b, it was found that the PIN10-D (100 mm^2) and OSD50-E (50 mm^2) presented similar bandwidths, which was thought to be justified since the photodiodes have similar capacitances. Yet, it certainly drew attention to the importance of carefully selecting the photodiode in VLC systems to obtain the highest achievable bandwidth and gain. Since the same bandwidth performance can be obtained by the PIN10-D (100 mm^2), which has double the area of the OSD50-E (50 mm^2), and as such can collect more light leading to the higher SNR. Such advantage is displayed by the higher S_{21} gain (4 dB difference). On the other hand, peculiarly, the responses obtained from the PIN25-D (600 mm^2) and OSD100-E (100 mm^2) also presented almost similar bandwidths, despite the PIN25-D having approximately 3.5 times higher capacitance (attributed to the bigger area). Such behaviour leads to the assumption of additional bandwidth-limiting factors in the OSD100-E, which constraint the achievable bandwidth of the receiver. This unpredicted frequency behaviour displayed by all four photodiode circuits is attributed to elements in the photodiode equivalent circuit model, which presents an additional series resistance R_s that is between the photodiode capacitance C_{pd} and the TIA input resistance. R_s is often in the range of a few ohms; as such, it became a convention for circuit designers to ignore it and simplify the pho-

todiode model as just a capacitor, since it is assumed that R_s has a negligible effect on the TIA performance. Nevertheless, such resistance adds to the TIA's input resistance. Hence, it is proposed that such resistance can, in fact, severely limit the bandwidth performance, especially when accompanied by a low input impedance TIA.

Steinbach (2002) reported high-frequency modelling and parameter extraction of 3 small area InGaAs photodiodes for the application of 40 Gb/s receiver [173]. The areas of the devices were not specified, but the author conjectured areas of approximately tens to a few hundred μmm^2 based on the values of the photodiode junction capacitance, which were in the range of tens of Femto Farads. In the extracted parameters, Steinbach reported the values of R_s to be 12 Ω, 18.5 Ω and 28.5 Ω for each device. Xu (2017) reported an extended model to the one reported in [173] and a semi-analytical method to determine the value of the photodiode equivalent model for devices with areas 120 μm^2 and 200 μm^2 [174]. Again R_s was estimated to be approximately 10 Ω. The modelling and parameter extraction of photodiodes is always reported for a small area and high-frequency devices, which indicated the presence of R_s of values higher than 10 Ω. There are no reports, however, of parameter extraction of large silicon photodiodes akin to the photodiodes used in this work. Therefore, it is important to conclude this work by extracting the model of these photodiodes to verify the values of R_s and, as such, bridge the gap between the predictions of the measurements of the TIA with only the simplified photodiode equivalent capacitance and the optical measurements. Moreover, none of the papers drew any conclusions into the relationship between the value of R_s of the photodiode and the latter's area, which the author expects to have some connection to the unexpected similarity in the bandwidths of TIAs employing the OSD100-E (100 mm^2) and PIN25-D (600 mm^2) photodiodes, depending on how large is R_s in each case.

Another set of measurements was taken replacing the RGC TIA with the modified RGC TIA of Chapter 6. It was noticed that unlike the results of Section 6.6, the modified RGC did not result in any bandwidth enhancement for any of the four photodiodes. Limitation seemed to be related to the photodiodes and not to the

circuit. This coupled with the frequency discrepancy of the S_{21} measurements of the photodiodes and the RGC TIA and predictions of measurements of the RGC TIA with the equivalent photodiode capacitances in Section 6.6 strongly supported the author's speculation of the presence of additional bandwidth-limiting element from the photodiode. This led to the investigation of the internal parameters of the photodiodes to assess their effect on their bandwidths, as will be investigated in the following section.

7.3 Photodiode Modelling & Parameter Extraction

This section investigates the modelling of large-area photodiodes to design wide-band VLC receivers. The photodiode modelling aims to gain insight into the effect of the intrinsic elements of the photodiode on its performance when loaded with low input impedance TIAs. As previously discussed, it is conjectured that modelling the photodiode by the simple RC passive equivalent circuit model may not be sufficient to mimic the photodiode behaviour faithfully. As such, this conjecture is investigated by measuring the S_{11} of each of the photodiodes in Figure 7.1, at different V_B, in the dark and illuminated at different light levels. The S_{11} is then converted to Z_{11} to obtain the real and imaginary impedance parts, Re(Z_{11}) and Im(Z_{11}), corresponding to the resistance and the reactance responses of the photodiode. These measurements are then compared to simulations of the simple RC passive photodiode equivalent circuit model and the two existing photodiode passive equivalent circuit models reported in [114, 175], as shown by Figure 7.5, to establish a reasonably accurate photodiode passive equivalent circuit model.

Following the photodiode passive equivalent model derivation, the parameter extraction of each of the photodiodes is detailed; based on curve fitting of their S_{11} and impedance responses and another set of measurements of their S_{21} at different V_B, using the optical link in Figure 7.2. Measurements of the S_{11}, Re(Z_{11}) and Im(Z_{11}) and S_{21} are used simultaneously to extract the fitted model parameters for each device. This guarantees that the parameters obtained from the S_{11}, Re(Z_{11}) and Im(Z_{11}) reflect the S_{21} behaviour in terms of the cut-off-frequency.

7.3.1 Photodiode Equivalent Model

The photodiodes used in VLC are often PIN diodes, which are devices with an intrinsic layer inserted between the p-type and n-type layers. Such devices have a depletion region of width W_D, which is given by (4.1). The depletion region junction capacitance C_{pd} relates to W_D, as expressed in (4.4). The photodiode will also have a shunt bulk resistance R_{sh} given by the slope of its current-voltage curve as defined by the Shockley equation in (4.2) and (4.3). Hence, such elements, C_{pd} and R_{sh} in parallel with a current source I_{pd}, are what forms the most basic photodiode passive

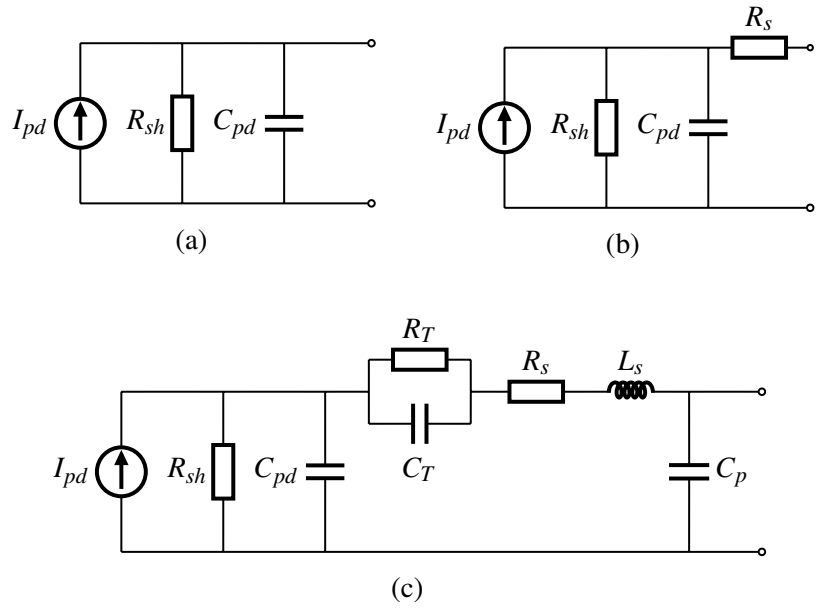


Figure 7.5: Photodiode small signal equivalent circuit model (a) Simple RC circuit model as used in [21] (b) Photodiode equivalent circuit model in [114] (c) Extended photodiode equivalent circuit model in [175]

equivalent model shown in Figure 7.5a.

The model in Figure 7.5b, accounts for the effect of the photodiode series resistance R_s. Such resistance is widely associated with the ohmic contacts of the photodiode only. However, in [176], R_s is described as the sum of the ohmic contact resistance R_c, in addition to the resistance of the undepleted region as expressed by:

$$R_s = \frac{(W_s - W_D)\rho}{A} + R_c \tag{7.1}$$

where W_s and ρ are thickness and resistivity of the substrate, respectively, and A is the diffused area of the junction. Taking the substrate parameters and area as constant, clearly, R_s is determined by W_D, which itself is a function of V_B. This suggests that such resistance is not strictly constant; it is a function of the bias condition. Moreover, interestingly, such resistance is inversely proportional to the photodiode area. Hence, implying that photodiodes with bigger areas will have smaller R_s, which may justify the unexpected similarity in the bandwidths of the RGC TIA obtained when employing the OSD100-E (100 mm^2) and the PIN25-D (600 mm^2) photodiodes in Section 7.2.2, as dictated by the relation between the

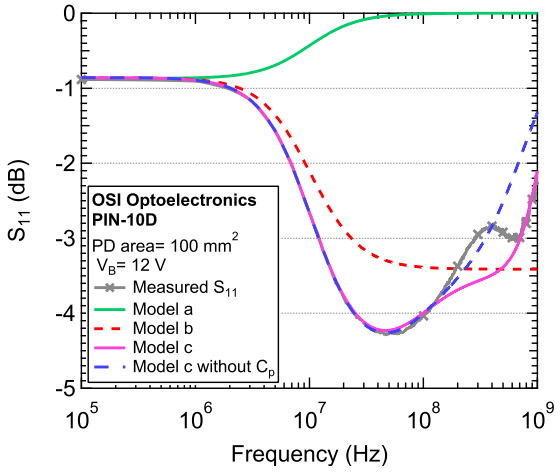
value of R_s and the photodiode area.

In [173, 175], a high-frequency photodiode equivalent circuit model is reported, as shown by Figure 7.5c. The model extends the conventional photodiode model to include the effects of the feed-line inductance L_p and the pad capacitance C_p. In addition to, an RC combination R_T and C_T, which were essential to fit the model to the s-parameters of the photodiode adequately and are described to be likely attributed to: i) Contacts that are not fully ohmic and display some Schottky behaviour, ii) a residual tunnelling contact between annealed and bond pad metal, or iii) a hole trap within the hetero-junction. This model was shown to be highly accurate at frequencies up to 40 GHz for various small area photodiodes.

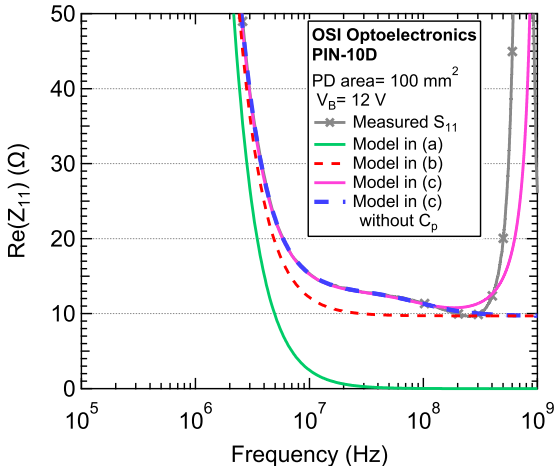
Typically, R_{sh} is in the order of several MΩ and, as such, behaves like an open circuit. Whereas, R_s is few Ohms, so it is often discarded, since it is assumed to have a negligible effect on the receiver's bandwidth. Hence, within the circuit design community, the photodiode model is often simplified to be C_{pd} only, which the author conjectures to be insufficient based on the S_{21} of the several photodiodes and the RGC TIA in Section 7.2.2. Hence, the validity of such simplification, especially in the case of large-area photodiodes, is investigated by fitting each of the photodiode models shown in Figure 7.5 to measurements of the S_{11}, derived $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ of the PIN10-D (100 mm^2). Furthermore, noting that the photodiode measurements also include the effect of R_b (1 kΩ), which is not shown as part of the models in Figure 7.1, yet is considered in the model simulations and curve fitting.

Figures 7.6a, 7.6b and 7.6c show the measured S_{11}, $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ of the PIN10-D at $V_B = 12$ V, respectively. From Figure 7.6a, it is clear that modelling the photodiode just by the RC circuit model shown in Figure 7.5a, shows a significant departure from the photodiode measured S_{11}. Whereas, considering the effect of R_s brings the model response to exhibit a similar profile with the photodiode measured S_{11}. Extending the model to consider the effects of L_p, C_p, R_T and C_T results in the most accurate emulation of the photodiode S_{11}. These trends are also reflected in the $\mathrm{Re}(Z_{11})$ and $\mathrm{Im}(Z_{11})$ of each of the models in Figures 7.6b and 7.6c, respectively.

From Figure 7.6b, it can be seen that $\mathrm{Re}(Z_{11})$ of the basic photodiode RC pas-



(a)



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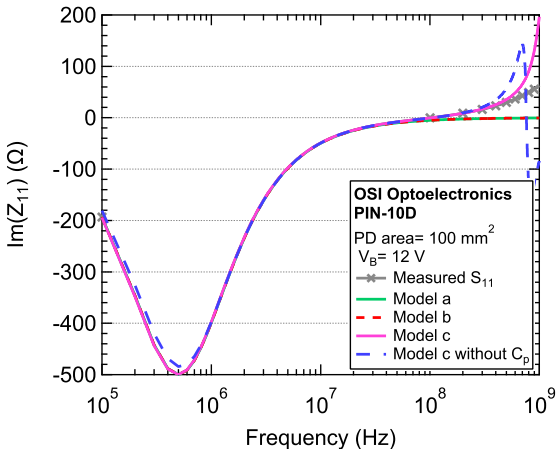


(c)

Figure 7.6: Simulations of the photodiode equivalent models in Figure 7.5 versus photodiode measurements (a) S_{11} (b) Re(Z_{11}) (c) Im(Z_{11})

sive equivalent circuit model decays to zero resistance. In contrast, the Re(Z_{11}) of the photodiode initially shows a decaying profile, until it reaches a resistive floor of approximately 10 Ω with some frequency-dependent behaviour, for an extended frequency range, before it shows a resistive rise at higher frequencies. Such behaviour is partially reflected by the model in Figure 7.5b, which considers the effect of R_s and, as such, shows a constant resistive floor behaviour. Nevertheless, the model fails to reflect both the frequency-dependent behaviour of the resistive floor and the high-frequency rise shown by the photodiode measurements. On the other hand, Re(Z_{11}) of the extended model in Figure 7.5c closely follow the frequency behaviour of the measured Re(Z_{11}) of the photodiode, this is credited to the additional R_T, C_T, L_s elements. Whereas, C_p contributes to the high-frequency rise, which is evident by the Re(Z_{11}) curves with and without C_p. This rise in resistance occurs at significantly high frequencies far above the photodiode operational frequency. Hence, as far as it concerns the modelling and design of photodiodes used in this work, C_p has almost no effect on the model accuracy within the range of interest. Nevertheless, an estimation of C_p was included for completeness.

As for the photodiode reactance, it can be seen from Figure 7.6c, that the Im(Z_{11}) curves for all of the photodiode models closely fit the measured Im(Z_{11}) by displaying a capacitive behaviour (i.e. is negative). Yet, such behaviour is only observed at low frequencies. At higher frequencies, the photodiode reactance becomes positive, suggesting that the reactance is not purely capacitive. This is only reflected by the model in Figure 7.5c, which considers the effect of the feed-line inductance.

Hence, based on the comparisons of the measured S_{11} and impedance responses of the photodiode versus the 3 models in Figure 7.1, it can be concluded that: i) Ignoring the series resistances $R_s + R_T$ results in inaccurate emulation of the photodiode behaviour, ii) For this particular photodiode, $R_s + R_T$ are estimated to be 10 Ω, which comes in series with the RGC input resistance and since, $R_s + R_T$ is significantly higher than the RGC input resistance (approximately 1 Ω). Therefore, intuitively such resistance would impose a significant bandwidth-limiting effect on the TIA, as will be verified by the next section, iii) Finally, the extended model in

Figure 7.5c shows the most accurate behaviour of the photodiode, as such is elected to be used for the parameter extraction of all four photodiodes (PIN10-D, PIN25-D, OSD50-E and OSD100-E) at different bias voltages V_B.

7.3.2 Parameter Extraction

This section describes the parameter extraction for the four photodiodes in Figure 7.1, by curve fitting simulations of the full photodiode passive equivalent circuit model shown Figure 7.5c to their measured S_{11}, Re(Z_{11}) and Im(Z_{11}) responses at different V_B. To ensure coherent model extraction for each photodiode, the model fitting is carried out by simultaneously comparing their S_{11} to their S_{21} responses when loaded by either a 50 Ω or the RGC TIA. This guarantees that the fitted parameter values from the S_{11} responses reflect the S_{21} behaviour in terms of the cut-off-frequency. The model fitting is limited to 400 MHz for the photodiodes of areas equal 50 mm^2 and 100 mm^2 and 200 MHz for the 600 mm^2 case. This was chosen in relation to the operational frequency of each photodiode, which is limited to 40 MHz in the best case. Moreover, the model curves are shown starting from 1 MHz; this is to omit the effect of R_b, which is most prominent at low frequencies as shown by Figures 7.6a-7.6c. The following list details the steps carried out for the model extraction procedure for all the photodiodes:

1. Curve fitting of the photodiode passive equivalent circuit model shown in Figure 7.5c to the measured S_{11}, Re(Z_{11}) and Im(Z_{11}) of each photodiode at different V_B.

2. Predict the cut-off-frequency of each photodiode at different V_B, when loaded by a 50 Ω, based on the fitted model parameters in step 1.

3. Compare the predicted cut-off-frequencies obtained in step 2 to the measured cut-off-frequencies from the S_{21} measurements for each photodiode when loaded by the 50 Ω.

4. If the predicted cut-off-frequencies do not match the measured S_{21} cut-off-frequencies in step 3, then update the fitted model values to achieve reasonably good matching. Otherwise, proceed to the next step.

5. Predict the cut-off-frequency of each photodiode at different V_B, when loaded by the RGC TIA based on simulations of the TIA and the corresponding fitted model parameters obtained in step 1.

6. Compare the predicted cut-off-frequencies obtained in step 5 to the measured cut-off-frequencies of the S_{21} measurements of each photodiode when loaded by the RGC TIA.

7. If the predicted cut-off-frequencies do not match the measured S_{21} cut-off-frequencies in step 5, then update the model values again until reasonable matching between the predicted cut-off-frequencies from the model and the measured cut-off-frequencies from the S_{21} is achieved.

The comparison of cut-off-frequencies obtained from the fitted model parameters to the S_{21} cut-off-frequencies of the photodiodes when loaded by the 50 Ω conducted in step 3 is sufficient to verify the accuracy of the extracted values. Nevertheless, the same procedure was carried out for each photodiode when loaded by the RGC TIA in step 6 for further verification. Moreover, the input resistance of the RGC TIA is only 1 Ω, which is significantly lower than the $R_s + R_T$ values, in contrast to the 50 Ω load, which is of comparable value to the $R_s + R_T$, which will be seen to exhibit values even higher than 10 Ω with the other photodiodes. As such, it was thought that the RGC TIA is more appropriate to measure the $R_s + R_T$.

For each photodiode, C_{pd} is estimated by de-embedding its value from the Im(Z_{11}) responses. R_s, R_T and C_T are estimated by matching the value and the profile of the resistive floor of the Re(Z_{11}) responses. Finally, L_s is estimated based on knowledge of the feed-line length and the LC resonance frequency obtained from the de-embedded C_{pd} curves from the Im(Z_{11}). The main aim of extracting the photodiodes model parameters is to establish a consistent relationship between the internal photodiode element values and bandwidth.

Figure 7.7 shows the measured S_{11} (solid) for the PIN10-D (100 mm^2) and the PIN25-D (600 mm^2) for different bias voltages V_B with simulations of their corresponding photodiode passive equivalent circuit model (dashed). Clearly, simula-

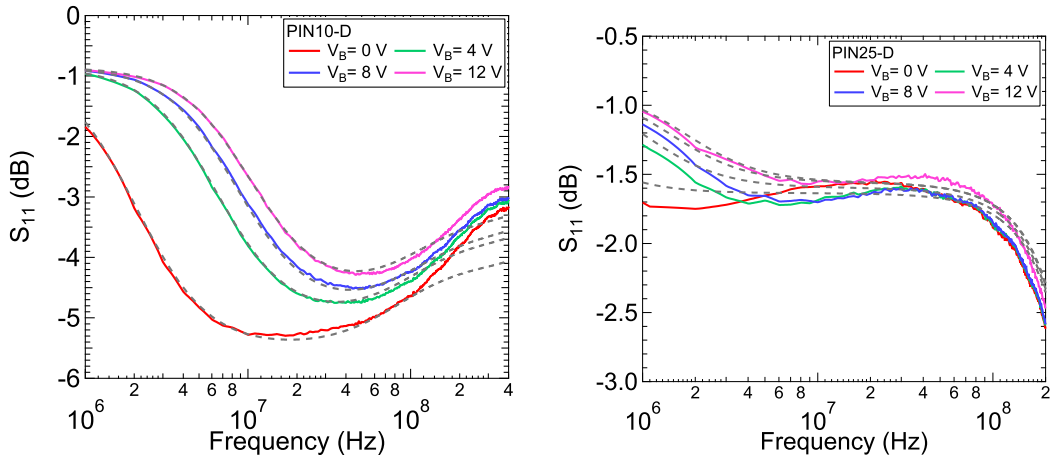


Figure 7.7: Measured S_{11} (solid) of the OSI Optoelectronics PIN10-D (left-side) and PIN25-D (right-side) versus the equivalent photodiode circuit model (dashed) at different V_B

Table 7.1: Extracted model parameters for the PIN10-D (100 mm^2) at different V_B

Bias (V)	C_{pd} (nF)	R_s (Ω)	R_T (Ω)	C_T (nF)	L_s (nH)
0	1.65	11.4	3.9	0.48	10
4	0.52	10.2	3.9	0.41	10
8	0.39	9.8	3.9	0.38	10
12	0.32	9.1	3.9	0.35	10

Table 7.2: Extracted model parameters for the PIN25-D (600 mm^2) at different V_B

Bias (V)	C_{pd} (nF)	R_s (Ω)	R_T (Ω)	C_T (nF)	L_s (nH)
0	9.6	2.8	1.9	0.2	17
4	3	2.7	1.9	0.18	17
8	2.2	2.6	1.9	0.17	17
12	1.8	2.5	1.9	0.16	17

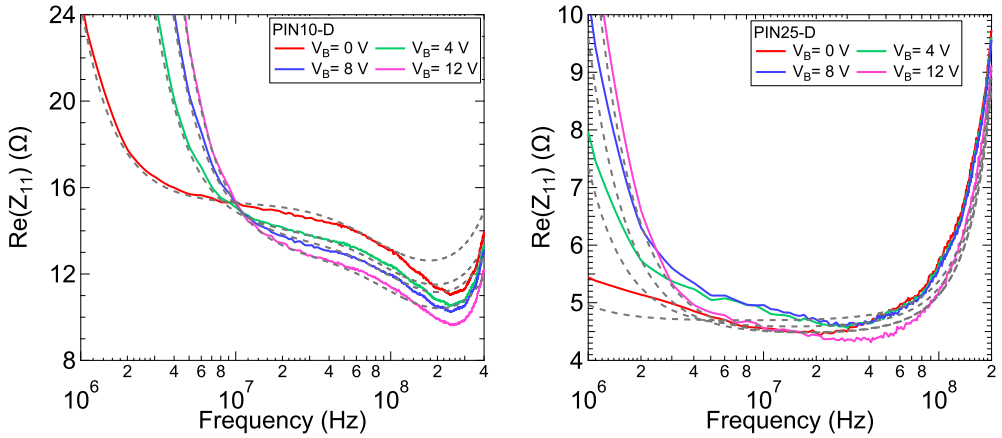
tions of the photodiode passive equivalent circuit model show reasonable agreement with the measured S_{11} responses of each of the photodiodes for all cases of V_B, with only slight variations at high frequencies for the PIN10-D (100 mm^2) case. These variations arise because of difficulties in estimating the values of C_p, but fortunately with negligible effect on the model's accuracy. The fitted parameter values of the photodiode passive equivalent circuit model are presented in Tables 7.1 and 7.2 for

the PIN10-D (100 mm^2) and PIN25-D (600 mm^2), respectively.

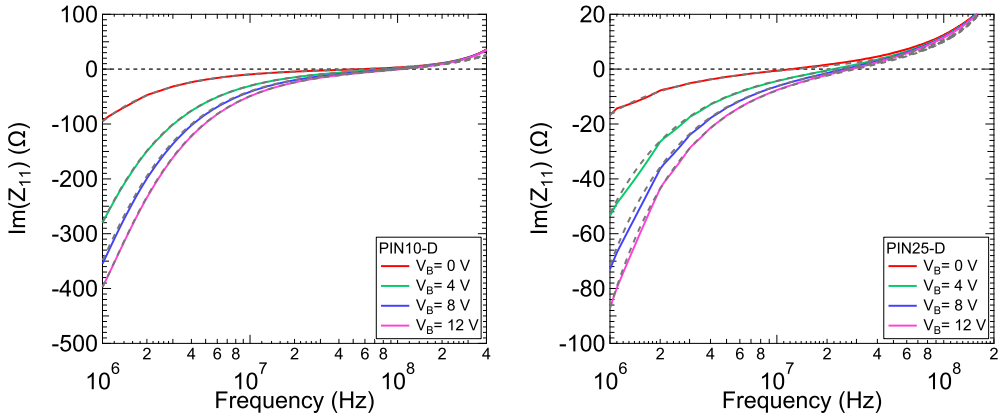
Figures 7.8a and 7.8b show the Re(Z_{11}) and Im(Z_{11}) of the two photodiodes at different V_B, respectively. From Figure 7.8a, it can be seen that for the two photodiodes, Re(Z_{11}) display a resistive floor, which corresponds to $R_s + R_T$. The resistive floor level strongly depends on the photodiode area, and to a lesser extent, on V_B, where increasing V_B results in only a slight reduction in the resistive floor level for each of the photodiodes. In contrast, the resistive floor level is significantly reduced when comparing the PIN10-D (100 mm^2) to the PIN25-D (600 mm^2), resulting from the increase in the photodiode area. These variations in the resistive floor level of the photodiodes are assumed to be due to R_s rather than R_T. Since according to (7.1), the value of R_s is a function of both the photodiode area and V_B. Whereas, R_T mainly emulates fixed properties of the photodiode structure, as such is assumed to be constant for each photodiode, irrespective of V_B.

Hence, based on the behaviour of the Re(Z_{11}) of the two photodiodes, it can be concluded that photodiodes with larger areas have a smaller sum of series resistances ($R_s + R_T$). Hence, when loaded by the RGC TIA, the PIN25-D (600 mm^2) bandwidth is largely limited by its exceptionally high capacitance ($C_{pd} = 1.8$ nF at $V_B = 12$ V) and to a lesser extent by the values of R_s and R_T. Therefore, the bandwidth achieved approaches that of Figure 6.20a, where only the effect of the simple C_{pd} model is considered. In contrast, for the PIN10-D (100 mm^2) case, the bandwidth limitation arises due to both the large value of C_{pd} and $R_s + R_T$. Therefore, the bandwidth achieved is significantly lower than predictions by the simple C_{pd} only model of Figure 6.20a. This explains why the RGC TIA was more effective in extending the bandwidth of the PIN25-D (600 mm^2) in comparison to the PIN10-D (600 mm^2) as shown in Figure 7.3.

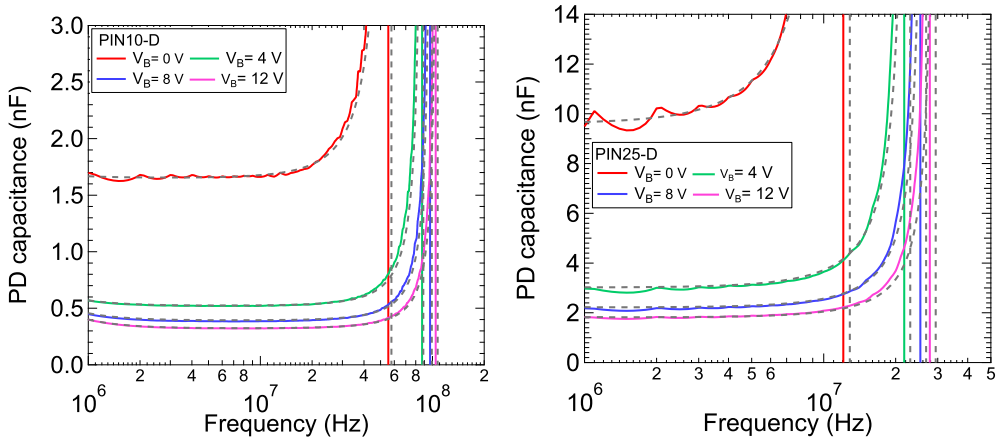
As for the reactance of the photodiodes, it can be seen from Figure 7.8b that for all V_B cases, the two photodiodes exhibit a capacitive behaviour, as indicated by their negative Im(Z_{11}) curves. Nevertheless, as the inductive effect of the feedline dominates, the Im(Z_{11}) becomes positive. The frequency at which Im(Z_{11}) is zero corresponds to the LC resonance frequency, which is used to estimate both



(a)



(b)



(c)

Figure 7.8: Measurements (solid lines) and fitted photodiode equivalent circuit model (dashed line) of the PIN10-D (100 mm^2) on the left-side and the PIN25-D (600 mm^2) on the right-side at different V_B (a) Re(Z_{11}) (b) Im(Z_{11}) (c) C_{pd}

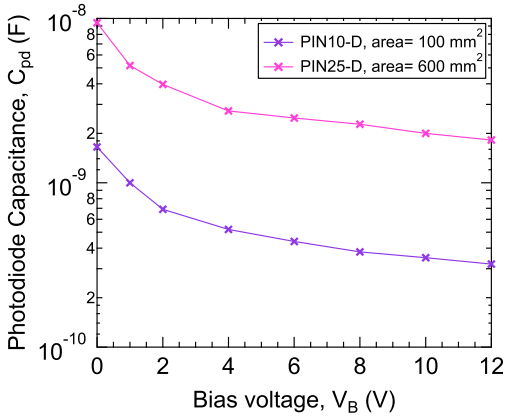
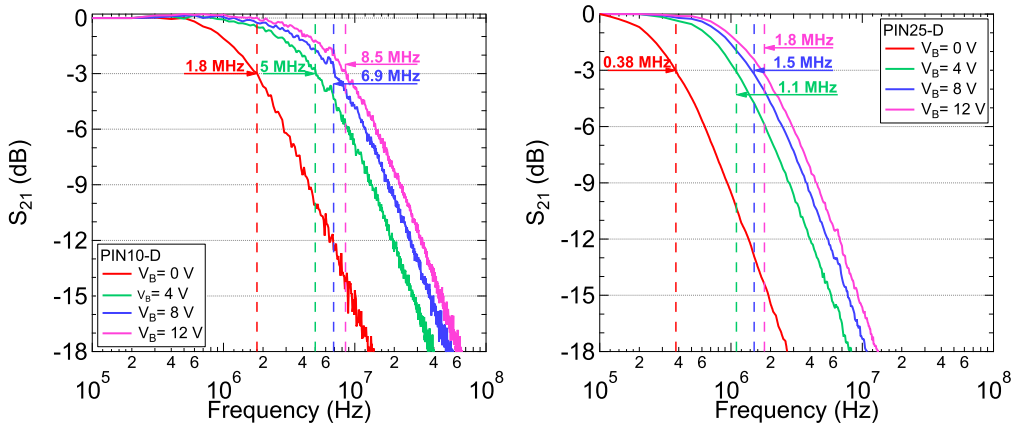


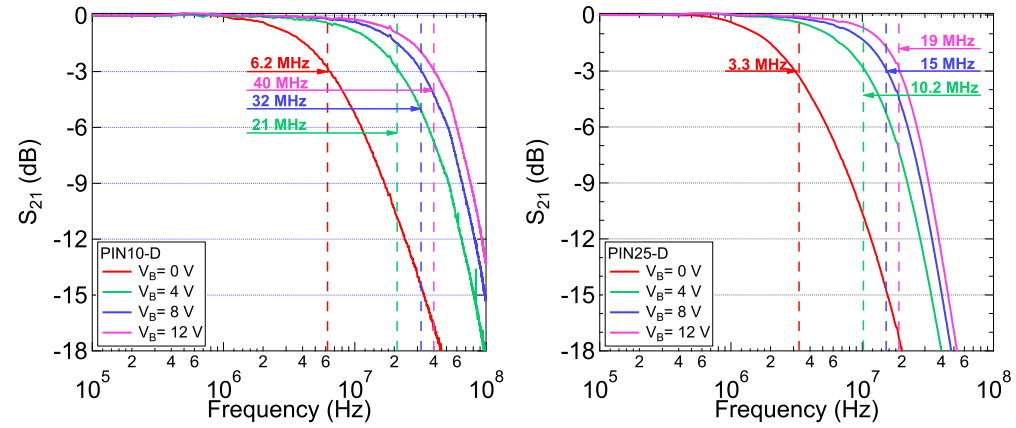
Figure 7.9: Measured C_{pd} versus V_B for the PIN10-D (100 mm^2) and PIN25-D (600 mm^2)

C_{pd} and L_s. For the two photodiodes, increasing V_B would increase W_D, which in turn reduces C_{pd} as indicated by the reduction in the Im(Z_{11}) curves (becomes more negative). Nevertheless, despite showing similar Im(Z_{11}) trend, there is a notable difference in their respective values, by a factor of 6 in all V_B cases, as expected from the factor of 6 difference in the photodiode areas. The same trend is illustrated by recording the capacitance of the photodiodes versus V_B as shown by Figure 7.9, where a factor of 6 increase in the capacitance is observed between the PIN10-D (100 mm^2) and the PIN25-D (600 mm^2). The behaviour observed in the Im(Z_{11}) responses are reflected in the de-embedded photodiode capacitance curves, shown by Figure 7.8c, where increasing V_B results in a reduction in C_{pd}, which in turn increases the frequency at which LC resonance occurs.

Figures 7.10a and 7.10b show the normalised measured S_{21} responses for the PIN10-D (100 mm^2) and PIN25-D (600 mm^2) at different V_B, when loaded by a 50 Ω and the RGC TIA, respectively. As predicted, in both cases increasing V_B, increases the cut-off-frequencies of the S_{21} responses of the photodiodes. For the 50 Ω case shown by Figure 7.10a, the bandwidth enhancement is a result of the reduction in C_{pd}, which in turn reduces the RC time constant dictating the receiver's bandwidth. Therefore, pushing the frequency of the real input pole to higher frequencies (real pole verified by the 6 dB/octave roll-off). Moreover, when comparing the photodiodes S_{21} responses when loaded by 50 Ω for all V_B cases, it can be observed that



(a)



(b)

Figure 7.10: Measured S_{21} of the PIN10-D (100 mm^2) on the left-side and PIN25-D (600 mm^2) on the right-side at different V_B (a) 50 Ω (b) RGC TIA

their cut-off-frequencies does not show a factor of 6 difference but approximately 4.7, which does not conform with their observed difference in C_{pd}. In other words, ideally, if each of the photodiodes is loaded by the 50 Ω $\|$1 kΩ and one has 6 times the capacitance, then the bandwidths observed should be 6 times smaller. Nevertheless, the sum of resistance seen by each photodiode is (50 Ω $\|$1 kΩ$+R_s+R_T$); as such, their bandwidth is given by:

$$BW = \frac{1}{2\pi(50\ \Omega \parallel 1\ k\Omega + R_s + R_T)C_{pd}} \tag{7.2}$$

where R_s+R_T is different in each case (higher for the PIN10-D case); as such, the observed bandwidth reduction does not directly correlate to the difference be-

Table 7.3: Measured and predicted bandwidths of the PIN10-D (100 mm^2) and PIN25-D (600 mm^2) at different V_B into a 50 Ω and the RGC TIA

Bias (V)	PIN10-D (100 mm^2)		PIN25-D (600 mm^2)	
	BW-50Ω (MHz)[-]*	BW-RGC (MHz)[-]$^+$	BW-50Ω (MHz)[-]*	BW-RGC (MHz)[-]$^+$
0	1.8 [1.5]	6.2 [5.9]	0.38 [0.32]	3.3 [3]
4	5.0 [5.0]	21.0 [21]	1.1 [1.0]	10.2 [11.4]
8	6.9 [6.6]	32.0 [30]	1.5 [1.4]	15.0 [17.0]
12	8.5 [8.2]	40.0 [40.0]	1.8 [1.7]	19.0 [21.8]

*Predicted bandwidths based on the extracted photodiode equivalent circuit model parameter values in Tables 7.1 and 7.2 and equation (7.2).
$^+$Predicted bandwidths based on simulations of the RGC TIA and the photodiodes equivalent circuit model using the parameter values in Tables 7.1 and 7.2.

tween their capacitances only. Another comparison of interest would be between the measured S_{21} cut-off-frequencies and the predicted cut-off-frequencies from the photodiode passive equivalent circuit model, when loaded by a 50 Ω presented in Table 7.3, where the predicted cut-off-frequencies show excellent agreement with the S_{21} measurements, as such, confirming the accuracy of the photodiode model.

On the other hand, for the RGC TIA case shown by Figure 7.10b, again increasing V_B results in a bandwidth enhancement due to the reduction in C_{pd}, hence, pushing the RGC input complex pole $p_{(1,2)}$ to higher frequencies (complex pole verified by the 12 dB/Octave roll-off). For the PIN10-D (100 mm^2) as V_B increases, the RGC TIA results in a bandwidth enhancement from approximately 3.5 to 5 times the bandwidth, in comparison to the 50 Ω responses. Whereas, for the PIN25-D (600 mm^2) as V_B increases, the RGC TIA results in a bandwidth enhancement from approximately 9 to 11 times the bandwidth in comparison to the corresponding 50 Ω responses. As previously discussed, the RGC TIA is more effective in increasing the bandwidth of the PIN25-D (600 mm^2) than the PIN10-D (100 mm^2) since it has lower values of $R_s + R_T$, due to its large-area, as verified by the parameter extraction shown in Tables 7.1 and 7.2. Furthermore, it can be noted that predictions of the S_{21} cut-off-frequencies obtained from simulations of the frequency responses of the RGC TIA with the full photodiode passive equivalent circuit model based on values in Tables 7.1 and 7.2, show good agreement with the measured S_{21} cut-off-

frequencies as shown by Table 7.3. Hence, confirming the accuracy of the model parameter extraction of the two photodiodes.

A similar procedure is conducted for the OSD50-E (50 mm^2) and the OSD100-E (100 mm^2), where again the model parameter procedure detailed earlier are carried out for each photodiode. Figure 7.11 shows the S_{11}, where it is clear that the model shows good agreement with the measured S_{11} responses of the photodiodes. The fitted parameter values of each of the photodiode equivalent model are presented in Tables 7.4 and 7.5 for the OSD50-E (50 mm^2) and OSD100-E (100 mm^2), respectively. Whereas, Figures 7.12a and 7.12b show the Re(Z_{11}) and Im(Z_{11}) of the OSD50-E (50 mm^2) and the OSD100-E (100 mm^2) at different V_B, respectively.

Figure 7.12a shows similar Re(Z_{11}) behaviour as with the PIN10-D and PIN25-D in Figure 7.8a, where again the photodiodes display a frequency-dependent resistive floor with a resistive rise at high frequencies. Again the relationship between the photodiode area and the resistive floor level is maintained, where the photodiode with the larger area, namely, the OSD100-E (top-right), displays a lower resistive floor level in comparison to the OSD50-E (top-left). On the other hand, increasing V_B barely results in any variations in the resistive floor level, unlike in the PIN10-D and PIN25-D cases. This suggests that R_s of the OSD50-E (50 mm^2) and OSD100-E is almost insensitive to V_B. The reason for such insensitivity is unclear as it requires knowledge of the internal dimensions of the photodiode structure, which is not provided by the manufacturer.

However, despite being unable to establish a consistent relation between R_s and V_B for all the four photodiodes, the modelling still confirms the presence of a resistive component corresponding to $R_s + R_T$ that is a function of the photodiode's area. Such findings are enough to justify the bandwidth performance of each photodiode with the RGC TIA shown in Figures 7.3 and 7.4. For example, it is now clear why the OSD100-E (100 mm^2) showed similar bandwidth performance to the larger PIN25-D (600 mm^2), despite the latter having almost 4 times higher C_{pd}. Nevertheless, because the PIN25-D (600 mm^2) has a larger area, it has nearly 4 times lower sum of $R_s + R_T$ than the OSD100-E (100 mm^2), which offsets the

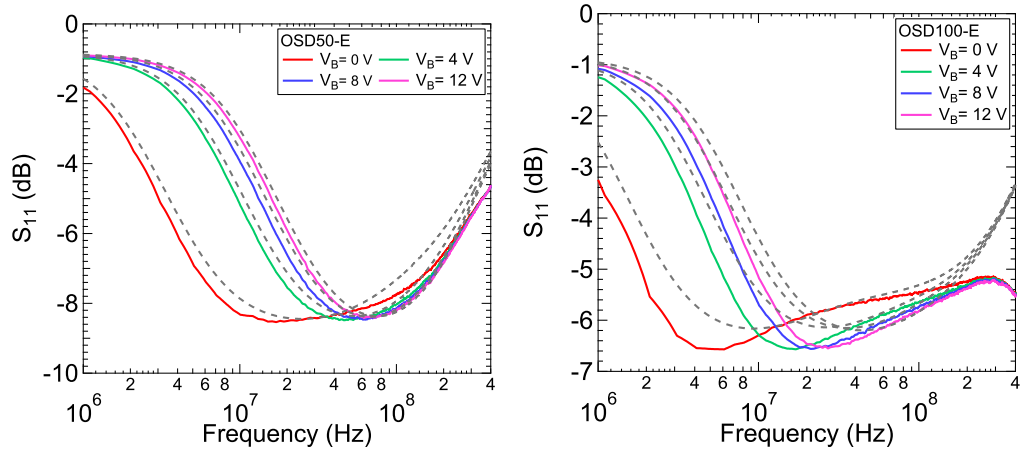


Figure 7.11: Measured S_{11} (solid) of the OSD50-E (50 mm^2) on the left-side and OSD10-E (100 mm^2) on the right-side versus the equivalent model (dashed) at different V_B

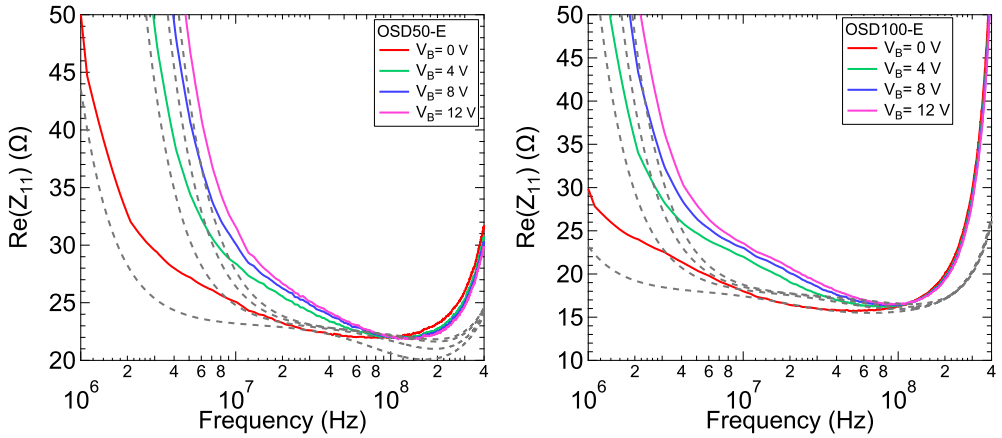
Table 7.4: Extracted model parameters for the OSD50-E (50 mm^2) at different V_B

Bias (V)	C_{pd} (nF)	R_s (Ω)	R_T (Ω)	C_T (nF)	L_s (nH)
0	1.1	18.3	4.8	0.38	20
4	0.36	18.2	4.8	0.22	20
8	0.26	18.1	4.8	0.16	20
12	0.22	18.0	4.8	0.14	20

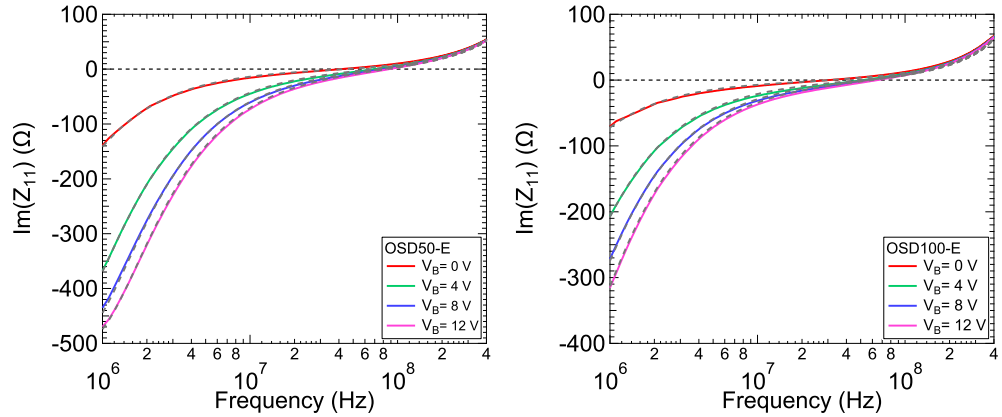
Table 7.5: Extracted model parameters for the OSD100-E (100 mm^2) at different V_B

Bias (V)	C_{pd} (nF)	R_s (Ω)	R_T (Ω)	C_T (nF)	L_s (nH)
0	2.2	15.1	2.9	2.8	20
4	0.73	15.0	2.9	1.1	20
8	0.53	14.9	2.9	0.76	20
12	0.45	14.8	2.9	0.55	20

effect of its higher capacitance and hence, the observed similarity in the bandwidths of the two photodiodes. Such characteristics favour the PIN25-D (600 mm^2) for VLC receivers over the OSD100-E (100 mm^2), since it offers almost the same bandwidth performance yet a much higher ability to harness light. Hence, it provides better SNR performance, which emphasises the importance of carefully choosing the photodiode used for the VLC receiver.



(a)



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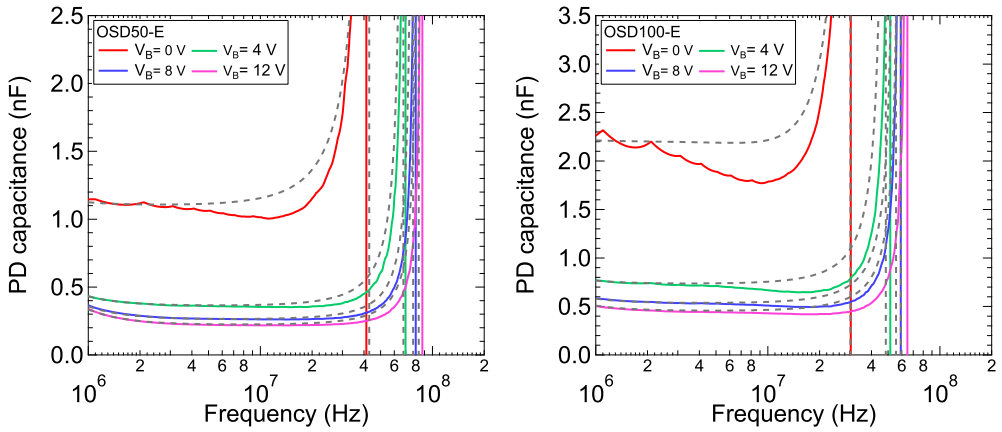


(c)

Figure 7.12: Measurements (solid lines) and fitted model (dashed line) of the OSD50-E and OSD100-E at different V_B (a) Re(Z_{11}) (b) Im(Z_{11}) (c) C_{pd}

As for the reactance, it can be seen from Figure 7.12b that for all V_B cases, the photodiodes show capacitive behaviour at low frequencies up until the resonance

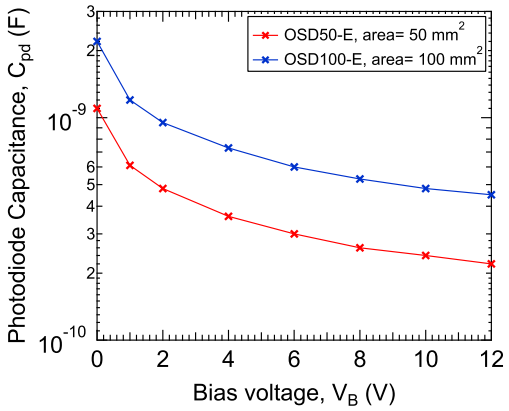
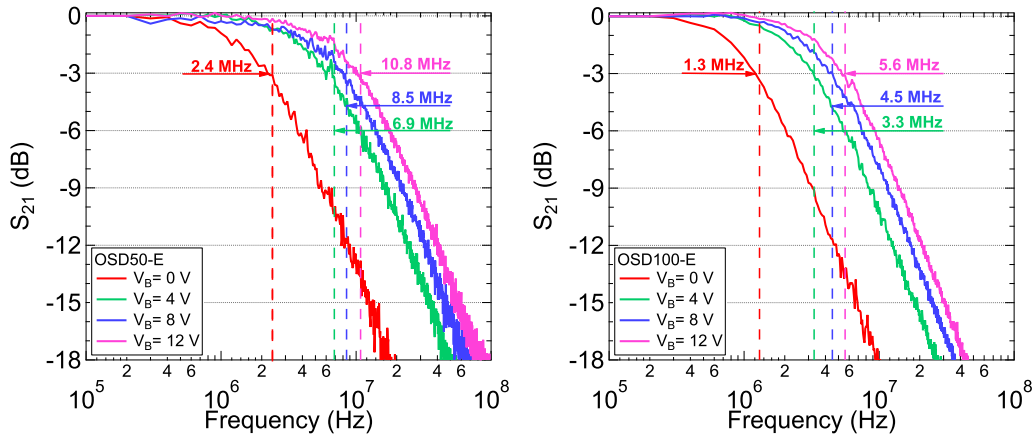


Figure 7.13: Measured C_{pd} versus V_B for the OSD50-E (50 mm^2) and OSD100-E (100 mm^2)

frequency, where the inductance of the feed-line dominants. The Im(Z_{11}) values of the two photodiodes indicates approximately a factor of 2 difference for all V_B cases, which again coincides with the factor of 2 difference in their areas. The same trend can be illustrated by recording each of the photodiode's capacitance versus V_B as shown by Figure 7.13, where a factor of 2 increase is observed. The behaviour observed in the Im(Z_{11}) responses is reflected in the de-embedded photodiode capacitance curves, shown by Figure 7.12c, were increasing V_B results in a reduction in C_{pd} and in turn increases the frequency at which the LC resonance occur.

Figure 7.14 shows the normalised measured S_{21} responses for the OSD50-E and OSD100-E at different V_B. Again, increasing V_B results in an increase in the S_{21} cut-off-frequency, which is a result of the reduction in C_{pd}. Reducing C_{pd} reduces the RC time constant, dictating the receiver's bandwidth and hence, the observed bandwidth enhancement. The S_{21} cut-off-frequencies of the two photodiodes shows approximately a factor of 1.9 difference for all V_B cases, which is slightly less than their observed difference in C_{pd}. The difference in C_{pd} showed a factor of 2, whereas R_s of the OSD100-E is only 30% lower than the OSD50-E, as such, the sum of resistances ($R_s + R_T + 50\ \Omega$) seen by the two photodiodes is not significantly different so doubling C_{pd} translated to almost halving the bandwidth. On the other hand, when comparing the cut-off-frequencies of the measured S_{21} responses and the photodiode equivalent model parameters shown in Tables 7.4 and 7.5, it is clear



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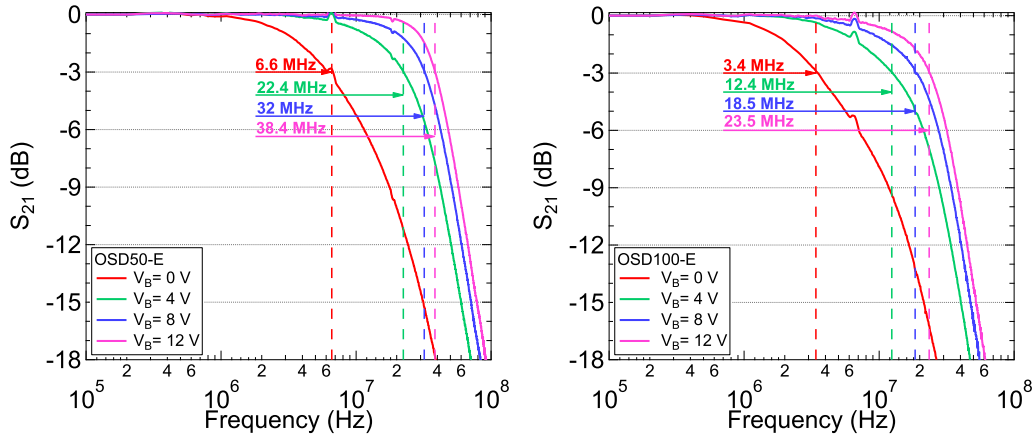


(b)

Figure 7.14: Measured S_{21} of the OSD50-E (50 mm^2) on the left-side and OSD100-E (100 mm^2) on the right-side at different V_B (a) 50 Ω (b) RGC TIA

that the predicted cut-off-frequencies from the model show excellent agreement with the S_{21} measurements, which confirms the accuracy of the photodiode model parameter extraction.

Based on the findings of the parameter extraction of the four photodiodes under test, it can be concluded that the model shown in Figure 7.5c provides a reasonably accurate estimation of each of the photodiode's behaviour. Moreover, extracting the photodiode model parameter's prior to the design of the TIA is of importance in identifying the key bandwidth-limiting elements. Therefore, this procedure should be extended to the design of all optical receivers and, in particular, VLC receivers employing large-area photodiodes, especially when followed by a low input resis-

Table 7.6: Measured and predicted bandwidths of the OSD50-E (50 mm^2) and OSD100-E (100 mm^2) at different V_B into a 50 Ω and the RGC TIA

Bias (V)	OSD50-E (50 mm^2)		OSD100-E (100 mm^2)	
	BW-50Ω (MHz)[-]*	BW-RGC (MHz)[-]$^+$	BW-50Ω (MHz)[-]*	BW-RGC (MHz)[-]$^+$
0	2.4 [2.0]	6.6 [6.1]	1.3 [1.1]	3.4 [3.8]
4	6.9 [6.2]	22.4 [20]	3.3 [3.3]	12.4 [12.1]
8	8.5 [8.6]	32.0 [29]	4.5 [4.6]	18.5 [17.4]
12	10.8 [10.2]	38.4 [35.0]	5.6 [5.4]	23.5 [21.2]

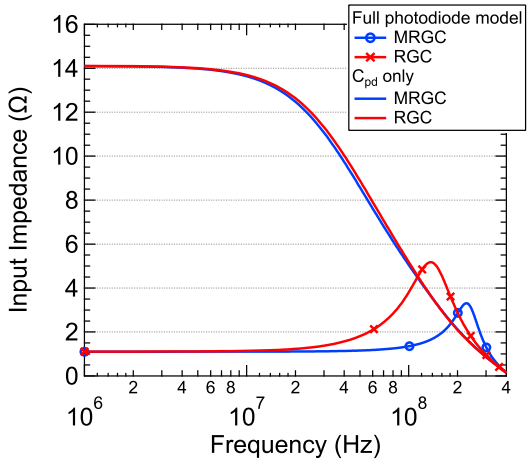
*Predicted bandwidths based on the extracted photodiode equivalent circuit model parameter values in Tables 7.4 and 7.5 and equation (7.2).
$^+$Predicted bandwidths based on simulations of the RGC TIA and the photodiodes equivalent circuit model using the parameter values in Tables 7.4 and 7.5.

tance TIA. As such, avoid inaccurate predictions of the receiver's bandwidth as encountered in Chapter 6, where the traditional approach of photodiode modelling was followed, and the effect of the photodiode resistive elements including R_s and R_T was ignored, leading to over-estimation of the receiver's bandwidth. Omitting such resistances is a common pitfall for most circuit designers, which is made more evident in the next section by examining the performance of the RGC and modified RGC TIAs with the full photodiode model versus the simplified model.

7.4 RGC/Modified RGC with the Photodiode Model

This section investigates the performance of the RGC and modified RGC TIAs with the full photodiode passive equivalent circuit model in Figure 7.5c versus the simple RC passive equivalent circuit model in Figure 7.5a. The TIAs are simulated using the NPN silicon transistors BFU520A at the same bias conditions of Section 7.2.2, at which $I_{C1} = 1$ mA and $I_{C2} = 4$ mA, $R_2 = 150\ \Omega$ at 1 kΩ transimpedance gain, with the output buffer (CC stage) at $I_{C3} = 0.5$ mA. The photodiode passive equivalent circuit model is taken from the extracted parameters of the PIN10-D (100 mm^2) at $V_B = 12$ V presented in Table 7.1.

Figures 7.15a and 7.15b show the input impedance and transimpedance gain responses of the two TIAs for the full photodiode passive equivalent circuit model versus the simplified passive equivalent circuit model, respectively. By inspecting the frequency behaviour of the TIAs in Figures 7.15a and 7.15b, three key observations can be made: i) The sum of resistances $R_s + R_T$ adds to the TIAs input resistances, which significantly enhances their value compared to the simplified photodiode passive equivalent circuit model that includes the input resistance of the TIAs only (resistance increase from 1 Ω to 14 Ω). Consequently, the bandwidth of the TIAs drops substantially, as illustrated by the corresponding transimpedance gain responses in Figure 7.15b. ii) Clearly, the bandwidth obtained by simulating the RGC TIA with the photodiode full passive equivalent circuit model matches the bandwidth obtained by its corresponding S_{21} response in Section 7.2.2 as illustrated in Figure 7.3a. Whereas, the bandwidth obtained from the simplified passive equivalent model leads to overestimating the TIAs bandwidths. ii) For the simplified equivalent model, there is a clear advantage of employing the modified RGC TIA, which improves the impedance frequency behaviour of the conventional RGC by shifting the impedance peak to higher frequencies while suppressing its peak. Such improvement in the impedance frequency behaviour of the RGC TIA translates to bandwidth enhancement, as seen in Figure 7.15b. Nevertheless, such an advantage is eliminated in the case of the full photodiode equivalent model since the effect of $R_s + R_T$ becomes dominant. Thus, the modified RGC TIA does not have the



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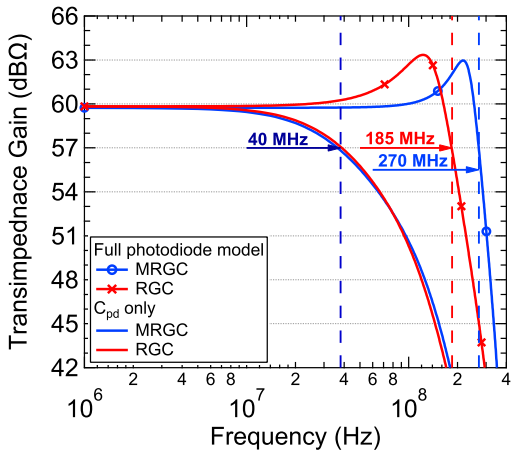


(b)

Figure 7.15: Simulations of the RGC and modified RGC TIAs with the full and simplified photodiode equivalent circuit model in Figures 7.5a and 7.5c based on parameter extraction of the PIN10-D at $V_B = 12$ V (a) Input impedance (b) Transimpedance gain

predicted bandwidth advantage.

Hence, it can be concluded that the series resistance $R_s + R_T$ of the photodiode significantly constrains the achievable bandwidth of VLC receivers when using the RGC and modified RGC TIAs. Nevertheless, if the undesirable effect of such resistances $(R_s + R_T)$ is neutralised, then the bandwidth advantage of the low input resistance RGC TIA predicted in Chapter 6 can be fully realised. In addition to also realising the advantage of ameliorating the Miller effect of $C_{\mu 1}$ of the RGC TIA and, in turn, the additional bandwidth advantage of the modified RGC TIA.

Such conclusions resulted in a proposal to employ a circuit technique based on the introduction of negative resistance in series between the photodiode and the low input impedance TIA. Details of the means of realising the negative resistance and the application of the circuit technique to the RGC and modified RGC TIAs are described in the following section.

7.5 Neutralising the Series Resistance of Photodiodes

This section describes a preliminary proposal of a circuit technique to combat the bandwidth-limiting effect of the series resistances $R_s + R_T$ encountered in large-area photodiodes. As previously discussed, these resistances add to the input resistance of the RGC TIA and, as such, severely limit its bandwidth advantage. Hence, the proposed circuit technique introduces a negative resistance in series between the photodiode and the RGC TIA to neutralise the effect of $R_s + R_T$. As such, fully realise the bandwidth advantages of the RGC and modified RGC TIAs. Similar to what was employed in Chapter 4. The negative capacitance was generated using a purpose designed negative capacitance circuit to obtain a grounded negative capacitance connected in parallel with the LED's junction capacitance.

On the other hand, for large-area photodiodes, the bandwidth-limiting series resistance is offset via a floating negative resistance element, which is connected in series with $R_s + R_T$. The floating negative resistance is generated using one of Linvill's NIC circuit configurations [68], which was described in Chapter 3. The generated negative resistance is then applied to the full photodiode passive equivalent circuit model in Figure 7.5c and the RGC/modified RGC TIAs to investigate its effectiveness in neutralising $R_s + R_T$ and, as such, extending the bandwidth of the VLC receiver.

7.5.1 Negative Resistance Generation

The generation of the floating negative resistance element is achieved using the Linvill OCS floating NIC shown by Figure 7.16. As previously discussed in Chapter 2, the open circuit stable (OCS) floating NIC is one of the two NIC circuit configurations proposed by Linvill (1953) in [68], where the other configuration is the short circuit stable (SCS) NIC. The key difference between the two configurations is the node at which the input is taken, which entails their stability criterion. If the input is at the emitter nodes, then the NIC is OCS; otherwise, if the input is taken at the collector nodes, the NIC is SCS. The NIC circuit in Figure 7.16 is the OCS type, which means it is essential to abide by the OCS stability criterion to realise stable operation. The stability of such circuit has been extensively studied

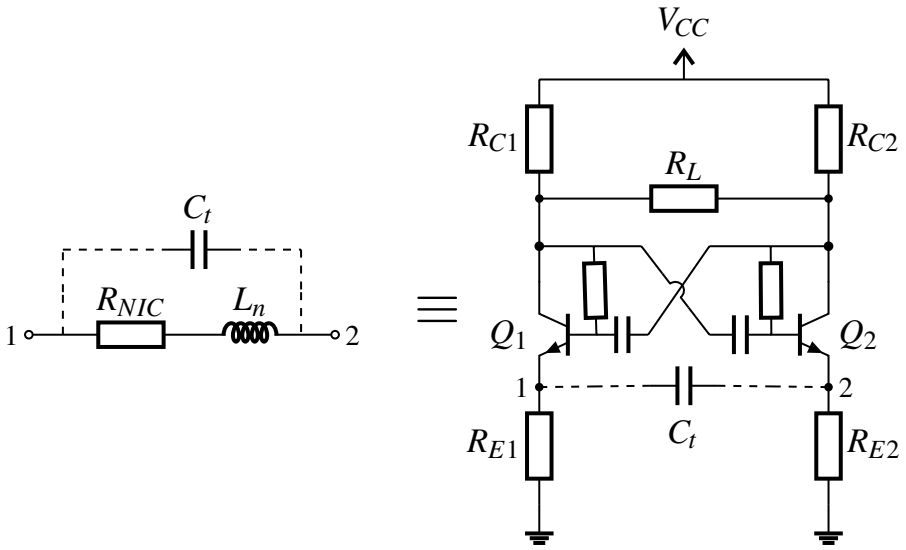


Figure 7.16: Linvill OCS NIC circuit generating negative floating resistance and its passive equivalent circuit model

in [55, 68, 79, 80], as such studies included in this work is limited to describing its operation and application to the large-area photodiodes and the RGC TIA.

In Figure 7.16, the NIC circuit consists of a cross-coupled transistor pair (Q_1 and Q_2), which achieves the positive feedback necessary for phase inversion so that difference in the transistor's collector currents will have opposite polarity to the difference in their collector voltages. Hence, the load resistance R_L appears negative at the emitter nodes. Therefore, assuming ideal transistor's with negligible internal resistive losses, capacitances and large bias resistors, resulting in negligible NIC loading. As a result, the NIC resistance presented at the emitter nodes is given by:

$$R_{NIC} = \frac{2}{g_m} - R_L \tag{7.3}$$

Clearly, if $R_L > 2/g_m$, then the overall resistance is negative. When assuming ideal transistors, choosing to operate at a combination of either low I_C and high R_L or high I_C and low R_L makes no difference in the quality of the generated negative resistance. Nevertheless, in practice, the intrinsic capacitances and inductances of the transistors (Q_1 and Q_2) will modify the NIC negative resistance component so that it becomes frequency-dependent. In addition to generating another reactance

component that comes in series with the generated negative resistance. Where it was found that the NIC reactance can be emulated by an inductor L_n in series with the R_{NIC} component as shown by the passive equivalent circuit model in Figure 7.16. The NIC passive equivalent circuit model was verified through simulations, as will become evident later in Figures 7.17a and 7.18a. The NIC inductance will deteriorate the quality of the generated negative resistance depending on the values of I_C and R_L. Moreover, as previously discussed in Chapters 2 and 3, operating at high I_C may compromise the NIC stability; due to the nature of its operation, which is based on positive feedback. Hence, a trade-off between the NIC circuit stability and the quality of the generated negative resistance is required.

The generated negative resistance is examined by simulating the input admittance response (Y_{11}) of the NIC circuit in Figure 7.16 at terminal 1 (emitter of Q_1), while terminal 2 is terminated using port 2 impedance termination. The imaginary and real parts of Y_{11}, corresponding to the NIC conductance $\mathrm{Re}(Y_{11})$ and susceptance $\mathrm{Im}(Y_{11})$ are then obtained. Where the reciprocal of the $\mathrm{Re}(Y_{11})$ is used to obtain the generated negative resistance, and the $\mathrm{Im}(Y_{11})$ is used to estimate L_n. It is worth noting that such simulation arrangement will generate a grounded negative resistance (since terminal 2 is grounded). Although the aim is to generate floating negative resistance to be connected in series between the photodiode and the RGC TIA, it is not possible to examine the behaviour of a floating negative resistance independently since the NIC circuit needs to be terminated to provide a ground reference. The termination can be either through the impedance of a port terminal or by additional circuitry like the RGC TIA. The simulation uses the NPN silicon transistors BFU520A at $I_C = 3$ mA for different R_L cases. Moreover, simulations of the NIC passive equivalent circuit model shown in Figure 7.16 is fitted to the admittance responses of the NIC circuit to first illustrate its accuracy in emulating the NIC behaviour and second, estimate the value of L_n.

Figures 7.17a and 7.17b show the simulated NIC conductance $\mathrm{Re}(Y_{11})$ and the generated negative resistance at different R_L, with their corresponding passive equivalent circuit model, respectively. Clearly, the passive equivalent circuit model

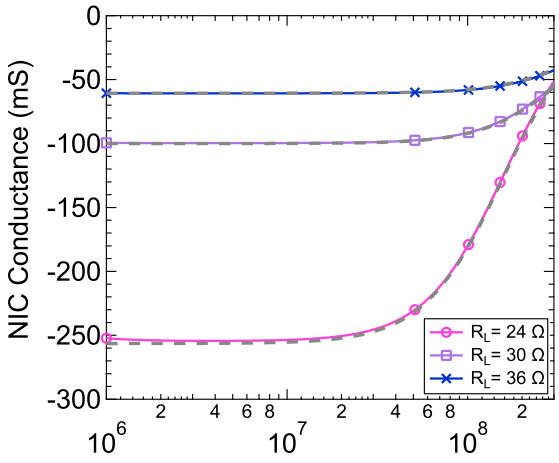
Table 7.7: Extracted passive equivalent model parameters for the NIC circuit in Figure 7.16 at different R_L

R_L (Ω)	R_{NIC} (Ω)	L_n (nH)
24	-3.9	4.0
30	-10	4.7
36	-16.5	5.8

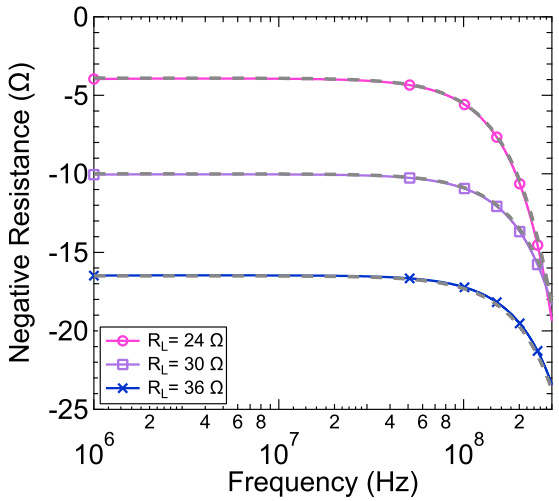
shows excellent agreement with the simulations of the NIC circuit for all the R_L cases. As such, confirming its accuracy in emulating the NIC behaviour. The fitted parameter values of the NIC passive equivalent circuit model for all R_L cases are presented in Table 7.7.

From Figure 7.17a, it can be seen that the NIC conductance is negative, as such indicating the generated negative resistance. Moreover, increasing R_L increases the NIC conductance, which in turn reduces the generated negative resistance (becomes more negative) as reflected by derived negative resistance curves in Figure 7.17b and the passive equivalent parameter values in Table 7.7. Additionally, the NIC conductance exhibits a frequency-dependent behaviour, especially at higher frequencies. Such behaviour is a result of the non-ideal intrinsic elements of the transistors. Moreover, the degree of frequency dependence of the NIC conductance depends on R_L, which is more significant for the lower R_L. These variations in the frequency dependence of the NIC conductance is important to consider when designing the NIC since they affect both the quality and the operational frequency range of the generated negative resistance. Such behaviour is also reflected in the derived negative resistance shown by Figure 7.17b, where clearly $R_L = 24\ \Omega$ shows higher frequency dependence in comparison to the 30 Ω and 36 Ω cases.

As for the NIC susceptance shown by Figure 7.18a, increasing R_L leads to a reduction in the magnitude of the $\mathrm{Im}(Y_{11})$ response, which was found to correspond to an increase in L_n of the NIC passive equivalent circuit model as shown by fitted parameter values in Table 7.7. First, such inductance is important to consider since it affects the overall quality of the generated negative resistance. Second, when applying the NIC circuit to the RGC TIA, the NIC inductive component will appear



(a)

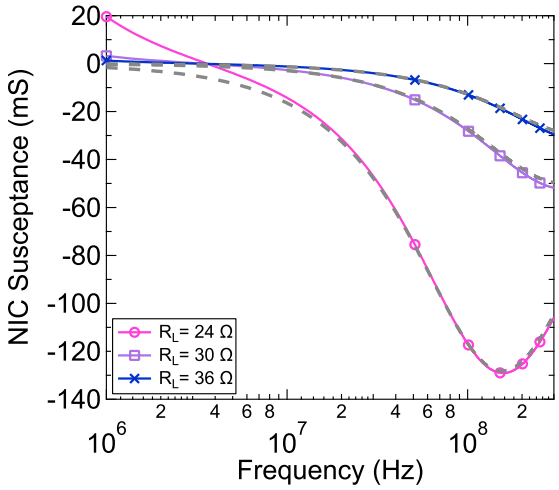


(b)

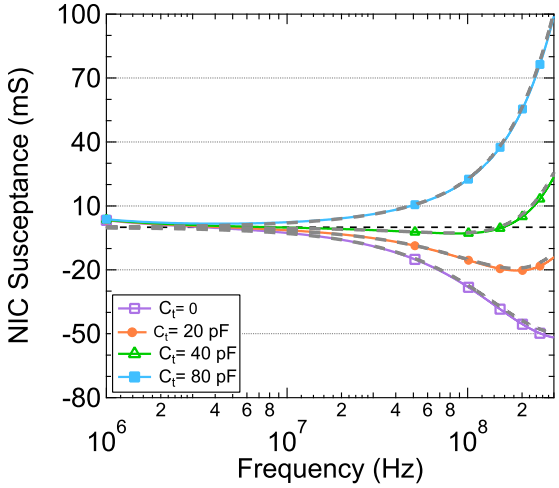
Figure 7.17: Simulations of the Linvill OCS NIC circuit (solid) and passive equivalent circuit model (dashed) for different R_L (a) Input conductance (b) Negative resistance

at the RGC input, as such may result in excessive peaking in its transimpedance gain response if such inductance is too high.

One technique that enables the modification of the NIC susceptance is proposed by White (2002), where the Linvill OCS NIC is configured to generate negative capacitance for the non-Foster matching of electrically small antennas [53]. The generated negative capacitance is optimised using a tuning capacitor C_t between the NIC emitter nodes as shown by Figure 7.16, as such provide improved antenna matching. In [53], C_t is realised using a varactor diode to provide flexibility



(a)



(b)

Figure 7.18: Additional capacitance to compensate for NIC inductance of Linvill OCS NIC circuit (a) Without and (b) With tuning capacitance C_t

in tuning its value to optimise the NIC performance. On the other hand, in the context of this work, C_t will appear in parallel with the combination of the series R_{NIC} and inductance as illustrated by the NIC passive equivalent model in Figure 7.16. Hence, C_t can be useful in tuning the NIC susceptance to reduce the effect of L_n, which improves the quality of the effective negative resistance generated by the NIC. The effect of C_t on the NIC susceptance is investigated for different values of C_t at a fixed $R_L = 30\ \Omega$ and $I_C = 3$ mA as shown by Figure 7.18b. It can be seen that the addition of C_t results in an increase in the NIC susceptance for all C_t values.

Moreover, for C_t equals 40 pF and 80 pF, the susceptance changes from negative to positive. The advantages of using C_t to tune the NIC susceptance will become evident in the following section covering the application of the OCS NIC to the full photodiode passive equivalent circuit model and the RGC TIA, where the addition of C_t leads to further bandwidth extension.

Hence, based on the studies of the Linvill OCS NIC, it can be inferred that when configured to generate negative resistance, the admittance presented by the NIC circuit is a combination of a negative resistance R_{NIC} in series with the inductance L_n. Where R_{NIC} is determined by g_m and R_L as given by (7.3) and L_n is due to the intrinsic capacitances and inductances of the NIC transistors. Such impedance combination is seen between the emitter nodes (terminal 1 and 2) as a floating impedance, as such can be connected in series in applications where compensation for resistive losses is beneficial.

7.5.2 Negative Resistance-RGC TIA for Large Photodiodes

This section investigates the effectiveness of the Linvill OCS NIC circuit in extending the bandwidth of large-area photodiode when connected to the RGC TIA. The bandwidth extension is achieved by neutralising the bandwidth-limiting effect of the photodiode's series resistances $R_s + R_T$ by introducing a series negative resistance R_{NIC}. Ideally, if $R_{NIC} = R_s + R_T$, as such completely neutralising the bandwidth-limiting effect of $R_s + R_T$, then the RGC bandwidth should present the bandwidths predicted based on measurements of the RGC TIA with only the photodiode equivalent capacitance C_{pd} at its input. Nevertheless, as previously discussed in Section 7.5.1, it is not practicable to realise pure negative resistance. Yet, the NIC admittance is a combination of a frequency-dependent negative resistance R_{NIC} in series with the inductance L_n. Hence, due to the frequency-dependent nature of R_{NIC} and the presence of the inevitable L_n, complete neutralisation of $R_s + R_T$ is not feasible. As such, the application of the OCS NIC can only extend the RGC bandwidth so that it approaches its predicted bandwidths with only C_{pd} at its input, depending on the quality of neutralising the $R_s + R_T$ component. Therefore, it is important to optimise the quality of the generated negative resistance to maximise the RGC bandwidth extension.

Figure 7.19 illustrates the passive equivalent circuit model of the OCS Linvill NIC when connected in series with the photodiode and the RGC TIA, where the RGC input impedance is simplified by only considering its resistive component R_a.

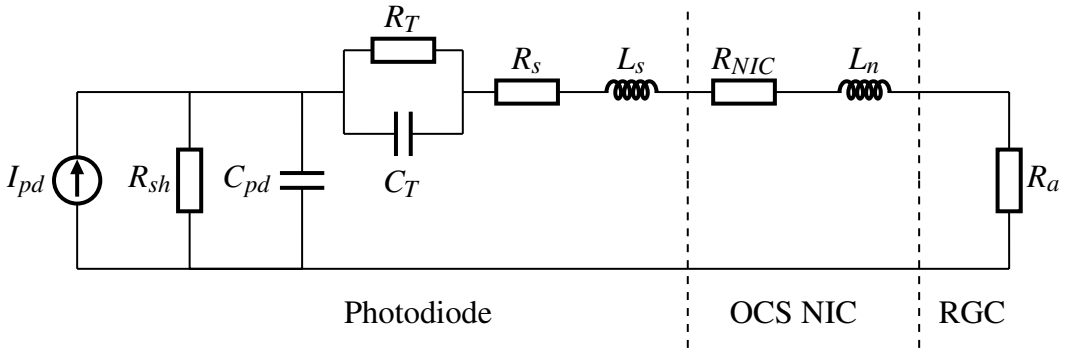


Figure 7.19: Photodiode and NIC passive equivalent circuit model

Whereas, Figure 7.20 shows the practical circuit implementation of the Linvill NIC connected in series between the photodiode equivalent model and the RGC TIA.

To investigate the effect of offsetting the series resistances $R_s + R_T$ on the RGC bandwidth performance, the frequency responses of the circuit in Figure 7.20 is simulated using the BFU520A. The photodiode equivalent circuit model is simulated based on the extracted model parameters of the PIN10-D at $V_B = 12$ V shown in Table 7.1, where $C_{pd} = 320$ pF and $R_s + R_T = 13\ \Omega$. Furthermore, the RGC is biased at $I_{C3} = 1$ mA, $I_{C4} = 4$ mA and R_{C4} = 150 Ω to obtain input resistance of approximately 1 Ω at 1 kΩ transimpedance gain. Whereas, the OCS NIC is biased at $I_C = 3$ mA for R_L cases of 24 Ω, 27 Ω and 30 Ω, which corresponds to R_{NIC} approximately of $-4\ \Omega$, $-7\ \Omega$ and $-10\ \Omega$, respectively. Figures 7.21b and 7.21a shows the simulated transimpedance gain and input impedance responses of the circuit in Figure 7.20 for the different R_L cases versus the RGC responses with the full photodiode equivalent model only (without the OCS NIC).

From Figure 7.21a, it is clear that for all R_L cases, the addition of the OCS NIC stage results in a significant reduction of the input impedance in comparison to the RGC input impedance with the full photodiode equivalent circuit only. For the RGC and the full photodiode equivalent model, the resistance is approximately 14 Ω, corresponding to the sum of $R_s + R_T + R_a$. The addition of the OCS NIC reduces the input resistance so that it is approximately 10 Ω, 7 Ω and 4 Ω, which corresponds to $R_s + R_T + R_{NIC} + R_a$ for each R_L value. Hence, it is clear that the OCS NIC results in effective neutralisation of $R_s + R_T$. Nevertheless, it can be observed that the reduction in the input resistance is also accompanied by a high-frequency peaking, which is enhanced as R_L increases. Such peaking is a result of the complex nature of the RGC input dominant pole $p_{(1,2)}$, which was studied in Chapter 6 (as illustrated in Figure 6.4b). Moreover, the interplay of the NIC inductance L_n with the RGC TIA also leads to increased peaking. Attempting to reduce the input resistance below 4 Ω to reach 1 Ω, as such approach complete neutralisation of $R_s + R_T$ will result in further peaking with minimal bandwidth extension.

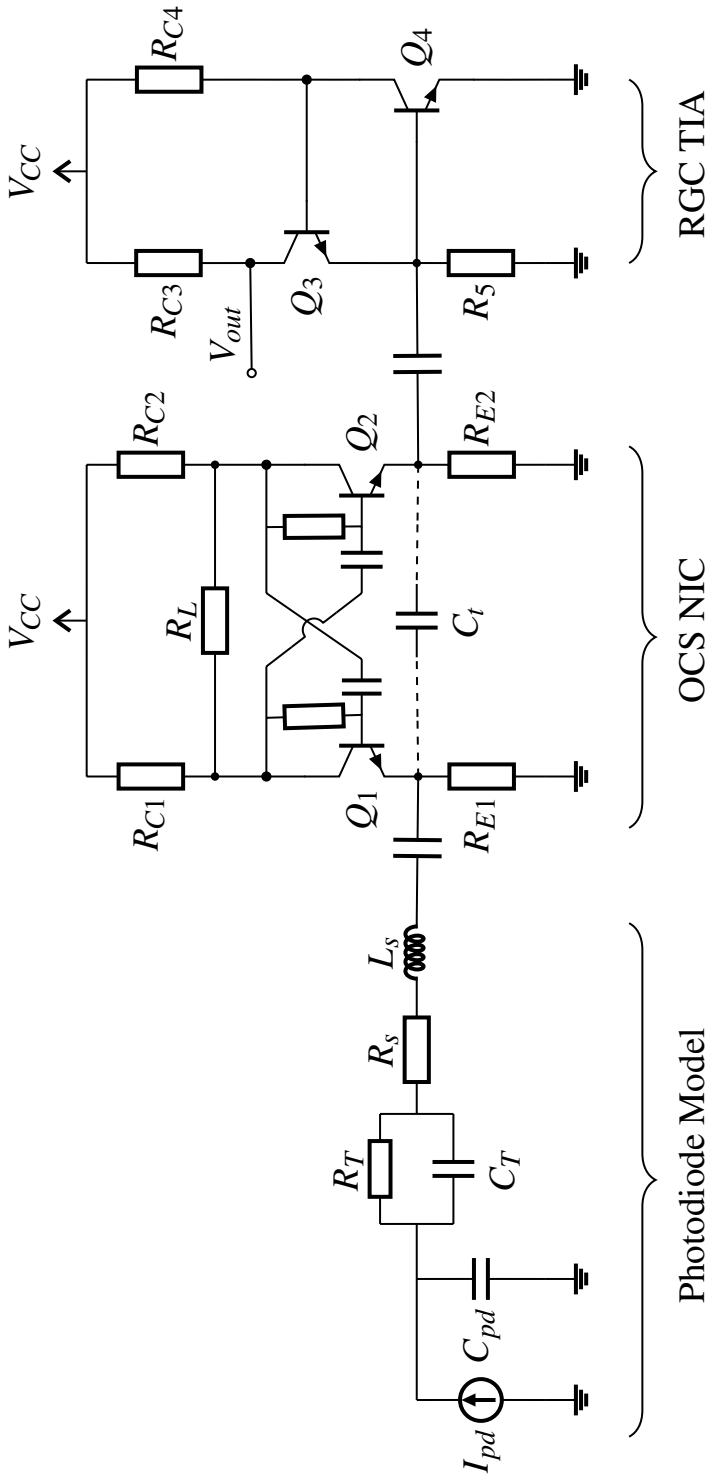
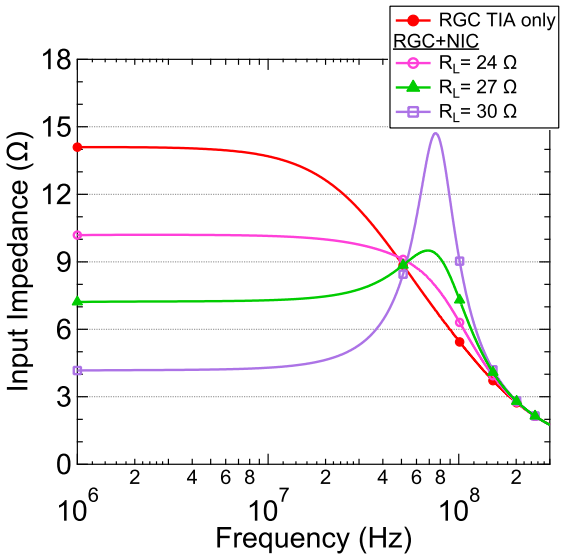
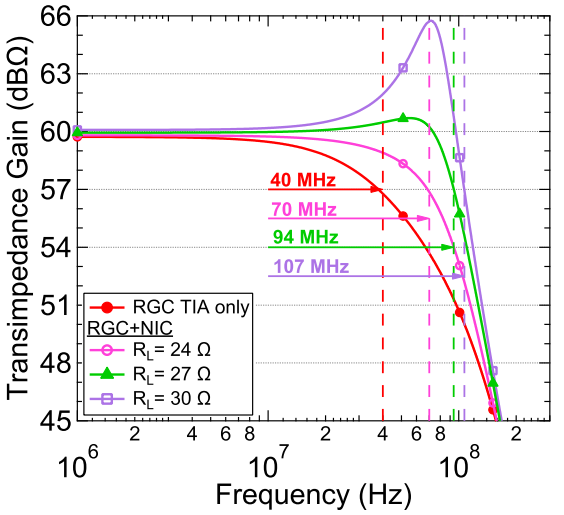


Figure 7.20: Linvill OCS NIC circuit generating negative floating resistance to compensate for the photodiode series resistances $R_s + R_T$



(a)



(b)

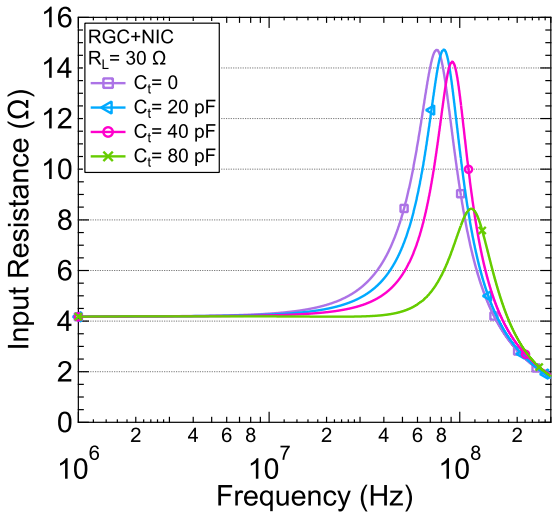
Figure 7.21: Simulations of the application of the negative resistance circuit (OCS NIC circuit) to the full photodiode equivalent model and the RGC TIA as shown in Figure 7.20, for different R_L values (a) Input impedance (b) Transimpedance gain

The advantage of offsetting the series resistances $R_s + R_T$ is reflected in the transimpedance gain frequency response shown by Figure 7.21b. Showing substantial bandwidth enhancement of 175%, 235% and 267% for $R_L = 24\ \Omega$, 27 Ω and 30 Ω, respectively, relative to the RGC TIA. Such bandwidth enhancement is due to the reduction in the photodiode series resistance at the TIA input (as a result of offsetting $R_s + R_T$), which pushes the dominant input complex pole of the RGC

TIA to higher frequencies. Moreover, peaking is observed for higher R_L, resulting from the interplay of the negative resistance and the RGC input impedance. Therefore, to avoid such high peaking levels, it is best to opt for R_L value that achieves a reasonable compromise between reducing the input resistance and well-behaved frequency behaviour.

On the other hand, instead of opting for lower R_L values to suppress the peaking amplitude of the transimpedance gain response, yet compromise the level of neutralising $R_s + R_T$ and, in turn, the achievable bandwidth. It is possible to opt for higher R_L, yet use C_t to tune the NIC susceptance. Hence, suppress the peaking amplitude and achieve further bandwidth extension. Under the same bias conditions and a fixed R_L, the effect of adding C_t to the circuit in Figure 7.20 is investigated by examining its input impedance and transimpedance gain responses. Figure 7.22a and 7.22b shows the input impedance and the transimpedance gain responses of the combination of the photodiode equivalent model, the OCS NIC and the RGC TIA for $R_L = 30\ \Omega$ at different values of C_t, respectively. Figure 7.22a, it can be seen that increasing C_t pushes the impedance peak to higher frequencies while suppressing its amplitude. Such behaviour is reflected in the corresponding transimpedance gain responses in Figure 7.22b, where increasing C_t leads to a significant bandwidth enhancement as a result of shifting the transimpedance gain peak frequency, while also suppressing its amplitude from over 6 dB to almost 3 dB. The observed bandwidth enhancement is approximately 144% in comparison to the case without C_t; such bandwidth enhancement matches the RGC bandwidth predictions with only C_{pd} at its input illustrated in Figure 6.20a. Hence, it can be concluded that the OCS effectively neutralises the bandwidth-limiting effect of the photodiode series resistance, where careful optimisation of the OCS NIC design parameters such as R_L and the addition of the tuning capacitor C_t can lead to substantial bandwidth enhancement of the receiver.

Lastly, the RGC TIA in Figure 7.20 is replaced by the modified RGC TIA to examine the effect of the OCS NIC on its bandwidth performance. Recalling that bandwidth measurements of the modified RGC with only C_{pd} at its input predicted



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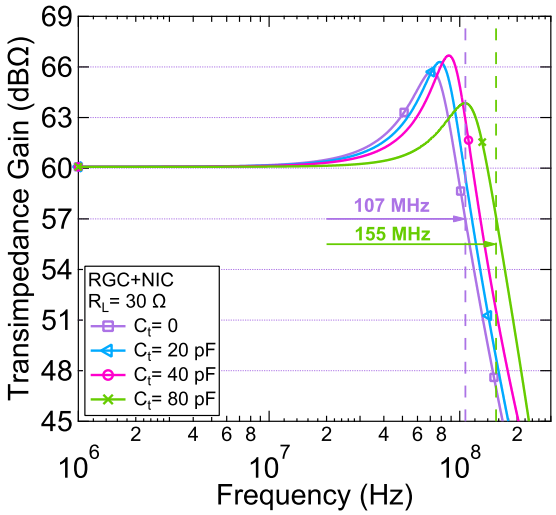


(b)

Figure 7.22: Simulations of the application of the negative resistance circuit (OCS NIC circuit) to the full photodiode equivalent model and the RGC TIA as shown in Figure 7.20 at $R_L = 30\ \Omega$ for different values of the tuning capacitor C_t (a) Input impedance (b) Transimpedance gain

an almost 150% bandwidth enhancement over the conventional RGC TIA as shown in Figures 6.20a and 6.20b. Such bandwidth advantage results from the amelioration of the bandwidth-limiting Miller capacitance inherent in the conventional RGC TIA. Unfortunately, when the modified RGC was measured with the photodiodes in Figure 7.1, the modified RGC did not show the expected bandwidth advantage, due to the dominant bandwidth-limiting series resistances $R_s + R_T$ of the photodi-

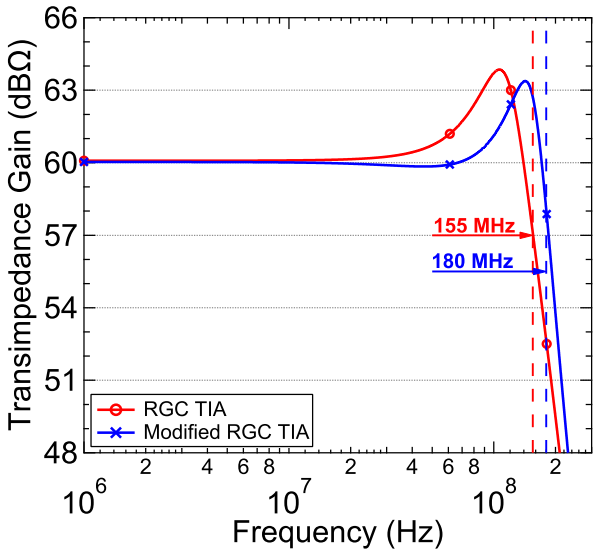


Figure 7.23: Simulations of the application of the negative resistance circuit (OCS NIC circuit) to the full photodiode equivalent model and the RGC TIA versus the modified RGC TIA at $R_L = 30\ \Omega$ and $C_t = 80$ pF

ode. Such behaviour was later verified by simulations of the input impedance of the modified RGC with the full photodiode equivalent circuit model in Section 7.4 as illustrated by Figures 7.15a and 7.15b.

Under the same bias conditions and photodiode model parameters, the OCS NIC is applied to the modified RGC TIA with the full photodiode equivalent circuit model at $R_L = 30\ \Omega$ and $C_t = 80$ pF. Figure 7.23 shows the transimpedance gain responses of the modified RGC versus the conventional RGC TIA. The increased bandwidth is expected to be further enhanced with optimised circuit design, and this is proposed as an area of further investigation.

7.6 Discussion & Conclusions

This chapter commenced with the application of the RGC TIA to four commercially available large-area silicon photodiodes of different areas and two different manufacturers within a VLC link. The bandwidth performance of each photodiode was evaluated by measuring the scattering parameter of the VLC link with the RGC TIA versus a 50 Ω impedance. Measurements of the S_{21} responses of the four photodiodes with the RGC TIA showed substantial bandwidth extension compared to loading with the 50 Ω case, ranging from 350% to over 1000% depending on the photodiode area and values of its internal elements. Despite, the remarkable bandwidth enhancement, the bandwidths obtained from the S_{21} when employing the RGC TIA showed significant departure from the predictions of measurements of the RGC TIA with the respective photodiode equivalent capacitances in Chapter 6. Moreover, S_{21} measurements of the link with the modified RGC TIA showed no bandwidth advantage over the RGC TIA, unlike what was predicted in Chapter 6.

The unforeseeable discrepancies between the bandwidths recorded by the S_{21} measurements and predictions of the TIAs bandwidths with the photodiode equivalent capacitance motivated an investigation into the internal parameters of the photodiodes, from which it was concluded that simplifying the photodiode passive equivalent circuit model as just a capacitor is not sufficient to predict its behaviour, faithfully, and in turn leads to inaccurate predictions of the TIA frequency behaviour and bandwidth. Moreover, the photodiode presents a sum of series resistances $R_s + R_T$, which adds to the input resistance of the TIA and hence, severely limits the achievable bandwidth, especially when using low input impedance TIAs. Nevertheless, it was shown that the bandwidth-limiting effect of the series resistance could be neutralised through a newly proposed circuit technique that introduces a series negative resistance between the photodiode and the TIA. The newly proposed circuit technique exploits the Linvill OCS NIC to generate the series negative resistance. Studies of the Linvill OCS NIC showed that a high-quality negative resistance could be generated by careful optimisation of the NIC design parameters, which suggests it to be a good candidate for the neutralisation of the bandwidth-limiting series

resistance of the photodiodes for high capacity visible light communication systems. The utility of the proposed NIC is demonstrated through simulations of the RGC/modified RGC TIAs with a full photodiode passive equivalent circuit model, which resulted in substantial bandwidth extension of the two TIAs.

Chapter 8

Conclusions

8.1 Summary & Discussion

The feasibility of VLC systems is mostly hindered by the highly bandwidth-limited optoelectronic devices, which severely limits data transmission rates. Previous research work focused on the efficient utilisation of the limited bandwidth offered by the optoelectronic devices (LEDs and photodiodes) by: (i) Adopting advanced modulation formats, such as OFDM and CAP, to maximise the number of transmitted bits per symbol, (ii) Use of efficient equalisation techniques such as the use of neural network equaliser at the receiver, (iii) Exploiting the colour dimension to enable wavelength division multiplexing (WDM), as such provide additional spectrum. Others resorted to improving the available bandwidth by employing devices with higher bandwidths such μLEDs and lasers. Only few researchers have exploited bandwidth enhancement circuits to circumvent the bandwidth limitation imposed by either the LEDs or the photodiodes. The work of this thesis focused on this last aspect.

The main objective of this research work was to improve the utility of the highly bandwidth-limited optoelectronic devices in VLC systems. To improve the utility of VLC optoelectronic devices, the research in this thesis has explored the design and application of new circuit techniques and topologies to extend the bandwidth of VLC transmitters and receivers. For the first time, this research proposed the utilisation of negative capacitance circuits to offset the bandwidth-limiting junc-

tion capacitance of high power large-area LEDs. Unlike other commonly used LED bandwidth extension circuits, the circuit in this thesis LED do not incur any loss in the optical power intensity of the compensated LED. Negative capacitance, which was synthesised using a new type of circuit and which was demonstrated to generate a wide range of high quality stable negative capacitances. The negative capacitance circuit was then applied to different colour LEDs, each demonstrating significant bandwidth enhancement without compromising optical power.

Moreover, the research proposed the utilisation of large-area photodiodes to enhance the power collection of VLC receivers and, therefore, boost the received optical power to afford a larger channel span. However, large-area photodiodes are associated with large junction capacitances, which severely limits the receiver bandwidth. Hence, this research proposed to circumvent such bandwidth limitation by utilising low input impedance transimpedance amplifiers, where particular attention was given to the regulated cascode (RGC) TIA configuration. Critical studies of the RGC TIA led to the identification of an internal Miller capacitance as bandwidth-limiting. Hence, a new modified RGC TIA was developed to eliminate the Miller effect through a modified cascode configuration, demonstrating improved transimpedance gain, bandwidth, and stability performance over the conventional design. A summary of the thesis is given in the paragraphs below.

Chapter 1 set an outline for the thesis and presented its contributions to knowledge. Moreover, it described the main challenges facing VLC systems, which lie in the bandwidth limitation imposed by the optoelectronic devices and the highly attenuating free-space optical channel. It also presented a survey of the key technologies that enabled multi-Gbps data transmission. This chapter highlighted some of the shortcomings of the state-of-art VLC system from which the justification and motivation of this work were drawn. Moreover, the chapter described the research directions chosen for this research work to address some of the limitations described.

Chapter 2 described the concept of negative impedance elements in their different forms, including negative resistance, capacitance and inductance, where each

can be realised either as a floating or grounded element. Floating negative elements are suitable for applications requiring a series connection, whereas the latter is for applications that need parallel connection. The chapter critically reviewed the key circuit techniques to generate negative impedance, particularly negative capacitance. The review included techniques based on two-port networks known as negative impedance converters (NICs) and circuits based on amplifiers using the Miller effect. Two key NIC circuits were discussed, including the Linvill NIC configuration in its two varieties and the op-amp-based NIC, coupled to a description and discussion of negative capacitance circuits based on the Miller effect in their differential and single-ended form.

Based on the reviewed circuit techniques, it was inferred that the operation of all negative impedance circuits is based on the use of positive feedback to manipulate the current-voltage of a given load impedance, which then appears as negative at the circuit input. As a consequence of positive feedback, such circuits are prone to instability, which often imposes some design challenges in realising stable negative elements. The chapter shows how some circuits could function independently as a negative capacitance and, as such, are more versatile in their applications. Others can generate negative capacitance only when integrated within a specific structure, like a differential stage, limiting their utility to a particular application. The wide range of applications reviewed have not addressed semiconductor junction devices similar to LEDs, and this led to the new research of Chapter 3.

Chapter 3 proposed new studies and analysis of a negative capacitance circuit reported in [46]. The circuit performance was studied and verified through modelling, simulations and experimental measurements. It was shown to offer a stable negative capacitance suitable for compensating the LED junction capacitance. The circuit was based on two transistors and a compensating capacitor C_c configured to create the positive feedback necessary to negate C_c. Analysis of the equivalent circuit model of the circuit established that it presents an input impedance that is a combination of a negative capacitance equals $-C_c$ in series with negative resistance $-R_c$. Through extensive modelling and simulations of the equivalent circuit model,

it was found that the range of operation and quality of the generated negative capacitance relies on three factors: i) The inevitable negative resistance component of the circuit impedance presented by the transconductance of the transistors, which degrades the efficacy of the negative capacitance circuit in neutralising any given capacitance. ii) Appropriate choice of the transistors is crucial since it was shown that the transistor lead inductances results in an LC resonance, which dictates the high cut-off-frequency of the frequency range of the generated negative capacitance. iii) Other circuit elements such as the biasing resistors, if not sufficiently high, may result in resistive loading of the negative capacitance circuit, which results in scaling of the value of the generated negative capacitance.

Despite such undesirable performance limiting factors, detailed modelling led to the design optimisations necessary to achieve a stable wide-band negative capacitance. It was found that the quality of the generated capacitance can be enhanced by minimising the undesirable negative resistance either by increasing the bias currents of the transistors or by using an additional compensating series resistance at the circuit input. Subsequently, the advantage of the negative capacitance circuit was verified by designing a practical circuits and measuring the scattering parameters of these circuits, constructed using discrete components on a PCB. Measurements showed that careful design allows a stable for the use in the equalisation of the bandwidth-limiting LED junction capacitance. Furthermore, measurements and simulation of the circuit demonstrated a wide range of negative capacitance values, showing its versatility and utility in applications beyond LED compensation, such as in high-speed optical fibre communications and possibly other applications beyond telecommunications, where the compensation of any performance-limiting capacitances is desirable.

Chapter 4 described the design, application and verification of the newly proposed LED bandwidth extension technique based on the negative capacitance circuit of Chapter 3, when applied to two commercially available LEDs of different colours and manufacturers, which resulted in bandwidth extension of up to 400% for a slow large-area blue LED and 500% for a relatively faster smaller area red

LED, with zero loss in the LED output optical power. Hence, from a systems point of view, the proposed LED bandwidth extension technique enhances the available bandwidth without degrading the SNR, significantly boosting the system capacity. These advantages were contrasted with other commonly used LED bandwidth extension techniques through a dedicated review of previously reported circuits, which established that such techniques are mostly based on passive analogue equalisers, which often incur a substantial loss in optical power. Hence, imposing a stringent trade-off between the LED bandwidth and optical power.

Such bandwidth advantages were achieved by following a methodical design approach to tailoring the negative capacitance circuit according to the distinct characteristics of each LED. Initially, a brief review of LED modelling was conducted to identify the most appropriate LED passive equivalent circuit model to aid in predicting the LED behaviour. A basic and a high frequency LED passive equivalent circuit models were described, where the basic model included dynamic resistance, junction capacitance and ohmic contact resistance. Whereas, the latter included additional parasitic effects from the packaging. The review concluded that the simple LED model can serve as a reasonable approximation in predicting the raw LED bandwidth and when compensated using the negative capacitance circuit. Subsequently, mathematical analysis of the passive equivalent circuit model of the LED, when connected to the negative capacitance circuit, was conducted, from which derivations of the compensated LED model transfer function was derived. The compensated LED model transfer function consisted of two zeros and two poles that can be either real or complex conjugate. Simulations of the impedance responses and pole-zero action of the compensated LED model transfer function concluded that the effectiveness of the negative capacitance circuit in extending the LED bandwidth is dictated by the interplay of the negative capacitance and negative resistance components with the raw LED model. Hence, requiring careful optimisations of the $-C_c$ and $-R_c$ values to enhance the achievable LED bandwidth extension, while also maintaining a reasonable peaking level. Such findings were verified through measurements of the scattering parameters of the negative capacitance circuit with

the passive equivalent circuit model of the LED constructed on a PCB.

Finally, since the application of the LED bandwidth requires knowledge of the parameter values of the LED equivalent circuit model, a simple parameter extraction procedure was conducted for both the blue and the red LEDs. Based on the LED extracted parameters, the negative capacitance circuit was adjusted to reach appropriate bandwidth extensions of each LED.

Despite the significant bandwidth enhancement, the proposed LED bandwidth extension technique does not come without disadvantages in the increased power dissipation and added noise. Nevertheless, the power consumed by such a circuit is only a fraction of the LED forward current, especially when employing high power LEDs, which also applies to its accosted noise contribution, which is expected to be lower than the shot noise contribution of the LED.

In Chapter 5, a comprehensive review of different transimpedance amplifier configurations was presented. The chapter highlighted the design challenges involved in achieving wide-band, high gain performance, especially in the presence of high photodiode capacitances. In particular, in VLC systems, where employing large-area photodiode is highly desirable to boost the received signal power and, in turn, the SNR. Yet such photodiodes are associated with ultra-high photodiode capacitance, which severely limits the VLC receiver's bandwidth.

Towards finding solutions to tackle the long term research problem of preventing the photodiode capacitance from limiting the optical receiver's bandwidth, the chapter presented a timeline like survey of the progression in the design of TIA configurations with high tolerance to photodiode capacitance. Starting with the classical shunt feedback amplifiers, it was gathered that the bandwidth and stability of such TIAs are highly dependent on the photodiode capacitance. Moving to the first report on the use of low input impedance stages featuring the common base configuration, which marked a step-change in the design of optical receivers by exploiting the low input resistance of the common base stage to isolate the photodiode capacitance from determining the TIA bandwidth. Nevertheless, such bandwidth advantage is at the expense of slightly increased noise compared to the

traditional common emitter and common collector stages. The chapter then discussed numerous reports of the common base TIAs and reports of its modifications featuring the well-acknowledged regulated cascode configuration, which was proposed as a modification of the common gate stage that uses a local feedback stage to enhance the transconductance of the common gate employing FETs to match the performance of BJTs. One section reviewed the common base/common gate stage and reports of their modifications, including different feedback configurations and ways to realise differential operation. Another section was dedicated to the regulated cascode stage and its modifications, which mainly featured configurations that aim to boost the transconductance of TIAs employing FET transistors without significantly increasing the current consumption.

Based on the reviewed low input impedance configurations, three key conclusions were drawn: i) The apparent suitability of employing low input impedance TIAs as front-end VLC receivers, Since such TIAs are highly insensitive to the exceptionally high photodiode capacitances encountered with the large-area photodiodes proposed to be used in VLC systems, ii) A particular topology that has been identified from this review, for its remarkable utility in designing low input impedance TIAs with ultra-wide bandwidth performance is the RGC TIA. Nevertheless, most of the reports of RGC, including those reported for VLC application, were based on the use of very small photodiode capacitances. iii) The unexplored potential of employing bipolar devices instead of FETs for its advantage of higher g_m at any given bias current, therefore, can easily achieve low input resistance in designs like the CB and RGC configurations without resorting to additional bandwidth extension techniques. Such conclusions prompted further study of the behaviour of the RGC TIA with large photodiode capacitances based on a design employing BJTs with the intent of optimising its utility, particularly in terms of transimpedance gain and bandwidth performance in the application of VLC systems.

Chapter 6 focus was on studying the RGC TIA performance with ultra-high photodiode capacitances, which led to the proposal of a modification of the conventional design that treats some of its inherent limitations and as such offers enhanced

bandwidth and transimpedance gain. The proposed modification was based on a critical performance analysis of the conventional RGC design, which identified an internal Miller effect as bandwidth-limiting. The proposed design modification of the RGC TIA introduced a cascode stage and hence, eliminated the bandwidth-limiting Miller effect. A comparative study of the two RGC designs based on frequency responses and pole-zero plots metrics has culminated that the modified design can achieve substantial improvement in bandwidth and stability performance.

The performance of the two TIAs was experimentally verified through measurements of the scattering parameters of two circuits constructed using discrete components on two PCBs. Experimental results showed the advantage of the new design where the bandwidth was nearly doubled relative to the traditional RGC, leading to a recorded bandwidth of 245 MHz at 300 pF for an overall transimpedance gain of 1 kΩ; which to the best of the author's knowledge is the widest bandwidth ever reported at such high input capacitance.

Chapter 7 described the application of the RGC TIA to large-area silicon photodiodes. The RGC TIA was tested within a VLC link employing commercially available silicon photodiodes of different areas and manufacturers, where the areas of the photodiodes under test ranged from 100 mm^2 to 600 mm^2. The use of such exceptionally high area photodiodes in VLC systems is in itself unconventional; since such devices impose a severe bandwidth limitation on the receiver bandwidth, such restriction is often avoided by employing photodiodes of significantly smaller areas. Nevertheless, such small area photodiodes are often incapable of collecting sufficient light to cater to long-distance transmission. As such, the proposal of using such large-area photodiodes, by optimising their bandwidth performance, is considered a significant improvement towards a more practical VLC implementation. The bandwidth performance was evaluated by measuring the scattering parameters of the VLC link with the RGC TIA versus a 50 Ω impedance termination. Measurements showed that employing the RGC TIA offers a substantial bandwidth enhancement of up to 1000% compared to the 50 Ω impedance counterpart.

Despite the remarkable bandwidth enhancement, the recorded bandwidth

showed a significant departure from predictions based on measurements of the TIA with the equivalent photodiode capacitance at its input. Investigations into the reasons for such discrepancies led to identifying the photodiode series resistance as an additional bandwidth-limiting factor. Such series resistance is often neglected by circuit designers and the photodiode modelling is often simplified as just a capacitor. Nevertheless, it was shown, through extensive modelling of several large-area photodiodes, that such simplification fails and consequently leas to inaccurate prediction of TIAs bandwidth. Consequently, a full photodiode equivalent circuit model was derived and verified through measurements of the scattering parameters of each of the photodiodes at different reverse bias conditions, from which it was established that such series resistance imposes a significant limitation on the photodiode bandwidth, especially when loaded by low input impedance TIA.

Finally, the chapter described a preliminary proposal of a circuit technique to combat the bandwidth-limiting effect imposed by the photodiode series resistance. The technique was based on introducing a series negative resistance to offset the bandwidth-limiting effect of the photodiode series resistance. The series resistance was generated by using one of the Linvill negative impedance converters configurations. The potential of the proposed technique was demonstrated through simulations of the negative impedance converter circuit, and the regulated cascode TIA was the full photodiode equivalent circuit model, which showed significant bandwidth enhancement as a result of neutralising the photodiode series resistance and, as such, fully realising the bandwidth advantage of the low input impedance RGC TIA.

The work presented in this thesis has demonstrated the advantage of employing optimised circuit techniques to improve the bandwidth of VLC transmitters and receivers by using new and rather unconventional circuits. It proposed the use of negative capacitance to extend the bandwidth of LEDs, which is fundamentally different from all reported LED bandwidth extension techniques since it achieves bandwidth extension without incurring any optical power loss and allows for bespoke equaliser design, based on the specific LED characteristics, leading to significant bandwidth

enhancement. Nevertheless, it is worth noting that the bandwidth advantage of the negative capacitance circuit is at the expense of slight increase in power consumption of the LED driver circuit and in turn the VLC transmitter. Furthermore, the thesis proposed the use of exceptionally large-area photodiodes with optimised amplifier design based on a modification of the regulated cascode configuration, which featured a substantial improvement in bandwidth and transimpedance gain. Again, the bandwidth and transimpedance gain advantage of the designed amplifier come at the cost of slightly degrading the noise performance, which is a typical limitation encountered in using the TIA configuration reported in this thesis. Nevertheless, the resultant bandwidth enhancement led to substantial improvement in the utility of such highly bandwidth-limited devices and hence, allowing higher detected optical powers and better SNR ratios, which is a fundamental requirement to enable high data rates long-span VLC links.

The research presented in this thesis opens new avenues of future work and research, including experimental work of a VLC link utilising the proposed circuit techniques on the transmitter and receiver, simultaneously. Based on the research reported here, other areas of interest and improvements for future investigation are identified, and are described briefly in the following section.

8.2 Further Investigations & Research Directions

The work and conclusions developed throughout this thesis motivates further investigations and future lines of work as listed below.

8.2.1 Further Investigations

- **Implementation of a fully optimised VLC link utilising the proposed circuit techniques**: The research presented in this thesis covered the application of new circuit bandwidth extension techniques of the transmitter and the receiver individually. Testing the performance while combining the negative capacitance circuit at the transmitter and utilising the low input impedance RGC with the large-area photodiode at the receiver, potentially at variable practical link distances, could improve the overall performance.

- **Improving the utility of the negative capacitance circuit in extending the bandwidth of LEDs**: Combine the negative capacitance circuit with other optically lossless LED bandwidth extension techniques, such as circuits adopting pre-emphasis stage as reported in [108] or carrier sweep out stages as in [107], could lead to further enhancement in the achievable bandwidth.

- **Studies of other relevant figures of merit for the RGC and Modified RGC TIA**: Figures of merits such as the noise performance and dynamic range have not been addressed in this thesis as the focus was on bandwidth maximisation. Noise analysis and optimisation are particularly important, especially in the presence of the ultra-high photodiode capacitances of the proposed large-area photodiodes. Joint optimisation of gain, bandwidth and noise would be a challenging, yet a worthwhile study.

- **Further investigation and verification of the photodiode bandwidth extension negative resistance technique**: Chapter 7 concluded the presence of the bandwidth-limiting photodiode series resistance, which severely limits the bandwidth advantage of the low input impedance RGC/modified RGC TIAs. A new bandwidth extension circuit technique was proposed, based on the use of negative resistance in series with the photodiode series resistance,

hence offsetting its bandwidth-limiting effect and enhancing the bandwidth of the receiver. The proposed circuit demonstrated prospective enhancement in bandwidth through preliminary simulation studies, yet it was not shown experimentally with the photodiode. Prior to the experimental demonstration, it is necessary to conduct further studies on the stability and interaction of the negative resistance circuit with the RGC/modified RGC based on mathematical derivations and circuit analysis of the proposed technique. This is to aid in understanding the nature of the system poles and the overall stability limits, which is imperative to practical realisation.

8.2.2 Future Research Directions

- **Optimisation of the proposed circuits techniques for fabrication as integrated circuits for high-speed applications**: The circuit techniques proposed in this thesis demonstrated substantial improvements in bandwidths of the VLC transmitters and receivers. The author envisages that such advantages are also transferable to high-speed applications, including optical fibre communications. In particular, the negative capacitance circuit can be used to neutralise the photodiode capacitance of optical fibre receivers, which are in the femto to pico-Farad range. Such an application requires high f_T transistors and an optimised layout, which may well require the fabrication of Silicon or III-V integrated circuits.

- **Multiple input multiple output VLC system using a large-area photodiode array**: Maximise the overall bit rate by aggregating several LEDs and large-area photodiode similar to the OSI Optoelectronics SPOT 9DMI, which is a common substrate photodiodes segmented into four separate active areas of approximately 20 mm^2 and therefore smaller associated capacitances compared to the photodiodes of Chapter 7. Designing the receiver's circuitry would employ the proposed low input impedance TIAs with appropriate modifications. In addition to adopting the relevant de-multiplexing techniques to separate the different LED data channels at the receiver akin to techniques

reported in [6, 177].

Altogether, this thesis explored new circuit techniques, designs and models of optoelectronic components and electronic circuits that make use of highly bandwidth-limited optoelectronic devices. A number of original contributions have been made, with five papers published. It is hoped that the proposed designs will pave the way to future practical implementations of VLC systems.

Appendix A

Linvill NIC Verification and Measurements

This appendix describes some preliminary measurements of the generation of negative resistance using the OCS NIC circuit of Chapter 7. A stable negative resistance was built and tested based on Linvill's OCS NIC circuit shown in Figure 7.16 with the addition of stabilizing resistors R_{stb} at the bases of Q_1 and Q_2. Figure A.1 shows Linvill's NIC fabricated on an FR4 PCB. The PCB is populated using silicon NPN transistors BFU520A ($f_T = 10$ GHz) and SMD for all resistors and capacitors. The scattering parameters of the fabricated NIC are measured using a VNA, which are then converted into its corresponding admittance parameters, to obtain the generated negative resistance. The bias currents of Q_1 and Q_2 are constantly maintained so that the value of $I_{C1} = I_{C2} = I_C$.

First, the NIC circuit utility is verified by measuring the quality of its negative

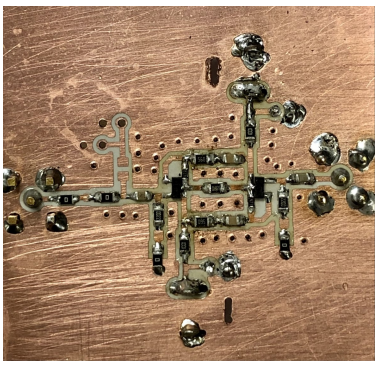


Figure A.1: Fabricated OCS NIC PCB

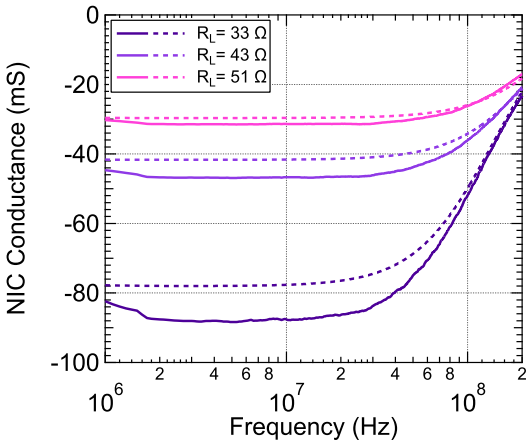
resistance generation. The NIC circuit is then applied to an equivalent model representing the photodiode and the low input impedance TIA to examine its effectiveness in extending the bandwidth of the equivalent circuit model of the photodiode and the TIA.

A.1 Negative Resistance Generation

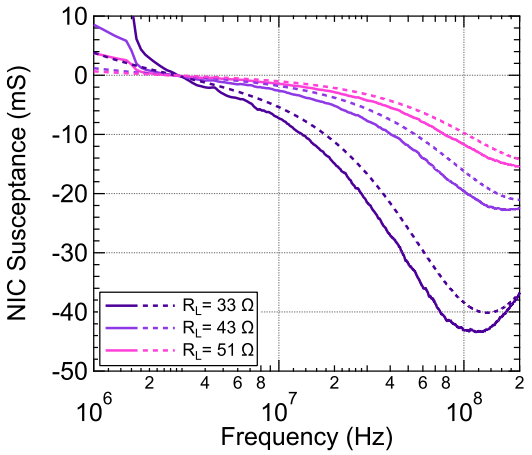
The quality of the negative resistance generation is examined by measuring the NIC circuit at $I_C = 3$ mA for $R_L = 33\ \Omega$, $43\ \Omega$ and $51\ \Omega$, which according to 7.3 should correspond to negative resistances equals $-16\ \Omega$, $-26\ \Omega$ and $-34\ \Omega$, respectively. Figures A.2a, A.2b and A.2c illustrate the measured and simulated OCS NIC conductance, susceptance and the derived negative resistance. Clearly, it can be seen that measurements presents good agreement with the simulations.

From Figure A.2a, the NIC conductance is negative, as such indicating the generated negative resistance. Moreover, increasing R_L increases the conductance, which in turn reduces the generated negative resistance (becomes more negative) as reflected in Figure A.2c showing the derived negative resistances. Moreover, for all R_L curves, it can be seen that the NIC conductance is relatively constant up to 60 MHz, then the conductance starts to show a frequency dependent behaviour that is mostly significant for $R_L = 33\ \Omega$. Such frequency dependent behaviour of the NIC conductance is reflected by the corresponding negative resistance curves shown in Figure A.2c. Such behaviour was also observed in the simulations of both the NIC circuit and its passive equivalent model as in Figure 7.17.

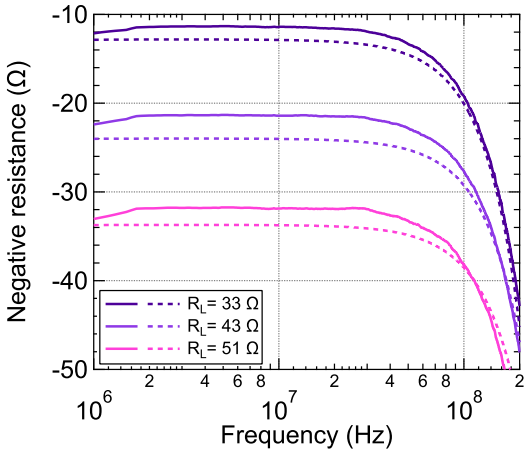
Whereas Figure A.2b, shows the measured and simulated susceptance of the NIC for the different R_L cases. It is clear that measurements show similar trends to that observed by the simulations of the circuit and its passive equivalent circuit model in Figure 7.18b.



(a)



(b)



(c)

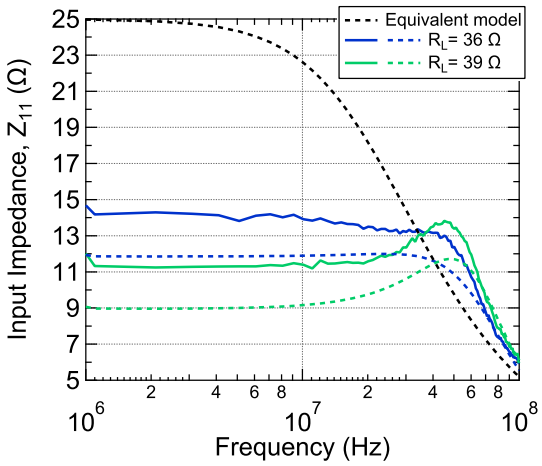
Figure A.2: Measured (solid) and simulated (dashed) OCS Linvill NIC at $I_C = 3$ for different R_L (a) Conductance (b) Suscpetance (c) Negative resistance

A.2 Linvill NIC-Photodiode-TIA Equivalent Model

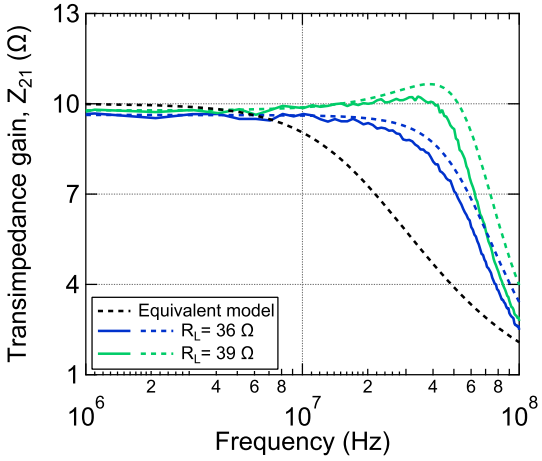
The OCS NIC circuit is then tested with the photodiode equivalent circuit model connected to terminal 1 of the NIC circuit (emitter node of Q_1 in Figure 7.16) and a shunt resistor acting as the TIA input resistance connected to terminal 2 of the NIC circuit (emitter node of Q_2 in Figure 7.16). Such arrangement would place the negative resistance generated by the NIC in series between the photodiode equivalent circuit model and the TIA resistance as illustrated by the passive equivalent circuit model in Figure 7.19.

The photodiode equivalent model are based on values close to the extracted parameters of the PIN10-D at $V_B = 12$ V, where $C_{pd} = 300$ pF and $R_s + R_T = 15\ \Omega$. Whereas, the shunt resistance R_a representing the TIA input resistance is set to 10 Ω. Noting that the RGC presents much lower input resistance (few Ω), yet R_a is initially set to 10 Ω for the sake of stability. Nevertheless, lower values of R_a equals 5 Ω and 2.5 Ω were also measured. Moreover, when the NIC is loaded by the photodiode equivalent model and amplifier resistance R_a, the NIC operation was not entirely stable. Therefore, the stabilising resistors R_{stb} in the feedback were increased until stable operation was achieved. Nevertheless, increasing R_{stb} results in degradation and scaling of the generated negative resistance, which in turn means that the measured negative resistances deviates from the theoretical predication given by (7.3). Similar behaviour was observed with the negative capacitance circuit of Chapter 3, were the addition of R_{stb} in the negative capacitance circuit in Figure 3.16a also resulted in scaling of the generated negative capacitance as illustrated in Figure 3.17, yet it ensured stable operation. Hence, in practice, realising stable of such circuits is often a compromise between stability and the quality of the generated element.

Figure A.3 shows the measured and simulated input impedance Z_{11} and transimpedance gain Z_{21} responses of the OCS NIC circuit with the photodiode and TIA equivalent models for $R_L = 36\ \Omega$ and 39 Ω. From Figure A.3a, clearly, the NIC results in a reduction of the resistance of the passive equivalent model, which corresponds to the sum of $R_s + R_T + R_a$ as given by the 25 Ω. Such resistance is reduced to approximately 15 Ω and 11 Ω for the $R_L = 36\ \Omega$ and 39 Ω.



(a)



(b)

Figure A.3: Measured (solid) and simulated (dashed) responses of overall network including OCS Linvill NIC, photodiode and TIA equivalent circuit model (a) Impedance response (b) Transimpedance gain

Clearly, the NIC circuit results in a reduction in the input impedance as opposed to the resistance of the passive equivalent circuit. Moreover, looking at the Z_{21}, the effect of ameliorating the resistance R_s leads to significant bandwidth enhancement.

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