A Goertzel Filter Based System for Fast Simultaneous Multi-Frequency EIS

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***Abstract*—Bioimpedance measurement is a non-invasive, radiation-free, and inexpensive method for measuring the electrical properties of biological tissues. In applications where transients occur, the commonly used swept sinewave is replaced with broadband signals such as multisine. This makes the signal generation and the extraction of the real and imaginary parts of the impedance challenging. In this brief, an alternative to traditional fast Fourier transform (FFT) or coherent demodulation is presented. Based on the Goertzel filter, this alternative is simpler and requires very few digital resources. Its robustness to the harmonic fold back phenomenon, enables simple ternary current pulses to be used for excitation. The developed digital architecture is capable of simultaneous demodulation of 16 frequencies with an accuracy of 97% and 96% on the magnitude and phase measurement respectively. Employing a ternary sequence allows the use of a low power H-bridge current driver. The analog front-end and demodulation algorithm were implemented in an ASIC using a 180-nm CMOS technology. The system was tested on an isolated pig heart distinguishing edema from non-edema tissue by impedance changes.**

***Index Terms*— Application specific integrated circuit (ASIC), electrical impedance spectroscopy (EIS), Goertzel algorithm, H-bridge current driver, ternary sequence.**

I. Introduction

Impedance measurement is an established method for non-invasive tissue analysis. In the biomedical field, it covers a wide range of applications, for example, lung monitoring [1], cancer detection [2], and myocardial edema [3]. Impedance measurement has major advantages; it is non-invasive, radiation-free, and cheaper than most traditional clinical devices. Electrical impedance spectroscopy (EIS) aims to analyze the impedance of a sample under test (SUT) over a specified bandwidth and for a specified set of discrete frequencies. Typically, a controlled current source is used for better control of the injected charges in the SUT [4] and is driven with a swept current sinewave throughout the required bandwidth. The demodulation of the voltage potential at the SUT is recorded simultaneously and the complex impedance is estimated.

In a significant number of applications where a transient occurs (e.g., cardiac monitoring, flow cytometry or any moving tissue), a very fast measurement across a wide frequency spectrum is required to obtain the instantaneous impedance spectrum [5]. In such applications, the traditionally used swept-sine waveform is replaced with broadband signals. They contain energy spread throughout the entire bandwidth of interest and thus, the impedance spectrum is estimated with a single and fast measurement. In [5], Sanchez *et al.* provide an extensive review and comparison of commonly used broadband signals. However, the demodulation to extract the real and imaginary parts of the impedance is more complex with broadband signals.

Traditionally, EIS systems with broadband excitation are based on bench-top devices including a data acquisition board. The waveform is digitally generated by a computer and converted to the analog domain via a fast digital-to-analog converter. The SUT is excited by a current driver in the analog front-end (AFE), and the resulting voltage after amplification is digitized by a high-speed high precision analog-to-digital converter (ADC). The demodulation is often performed on a computer. In some compact systems the computer is replaced with a dedicated micro-controller or an FPGA.

In this brief, a novel digital EIS solution for simultaneous multi-frequency excitation and demodulation is presented. The traditional FFT or coherent demodulation method is replaced by a Goertzel filter [6]. This, together with the use of tertiary signals for excitation, allows fast complex demodulation of an arbitrary excitation waveform of 16 frequencies simultaneously, requiring relatively few digital resources.

II. System Architecture

A. System Specification

The prototype EIS system shown in Fig. 1 comprises an application specific integrated circuit (ASIC) and an external 12-bit ADC (AD9237). The ASIC includes the AFE with an H-bridge current driver for current injection and a current feedback instrumentation amplifier (IA) [8] for voltage recording. It also includes a digital logic unit for system control, waveform generation and demodulation. A computer configures the measurement via a MATLAB interface and displays results. Excitation and readout paths are ac coupled for safety reasons.

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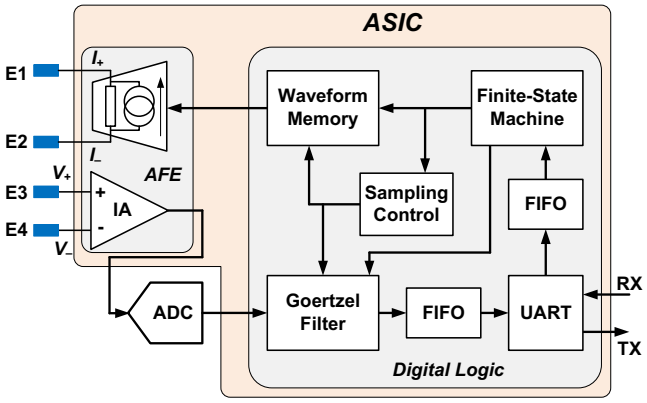


Fig. 1. Overall EIS measurement system architecture.

Fig. 2 shows the circuit implementation of the H-bridge current driver. The source (transistor M0) of the current driver is controlled by a linear feedback loop. By measuring the current through a sensing resistor, $R_f = 100\,\Omega$, the loop regulates the source output I_+ by comparing the measured voltage V_o to the input voltage V_{in}. The sink current I_- from transistor M1 is also controlled by a feedback arrangement [7]. The common mode voltage (V_{cm}) across the load is measured and compared to a zero-reference level (V_{ref}). Any mismatch within the H-bridge current driver between the source and sink is compensated by autozero feedback to ensure the voltage across the load (R_L) after ac coupling, as shown in Fig. 2, is fully differential.

A dedicated memory block in the ASIC stores up to 2048 samples for the ternary excitation sequence. Digital samples are simultaneously demodulated for 16 frequency points via the Goertzel filter block which is detailed in Section II.B. The memory waveform output, Goertzel filter and ADC are synchronously clocked via the sampling control unit. The overall system is controlled via a finite state machine (FSM). A UART interface transmits and receives data from a computer. Various parameters can be tuned via the UART interface, for example, the demodulation frequency, sample frequency and measurement duration. The waveform memory can be also written via the UART interface.

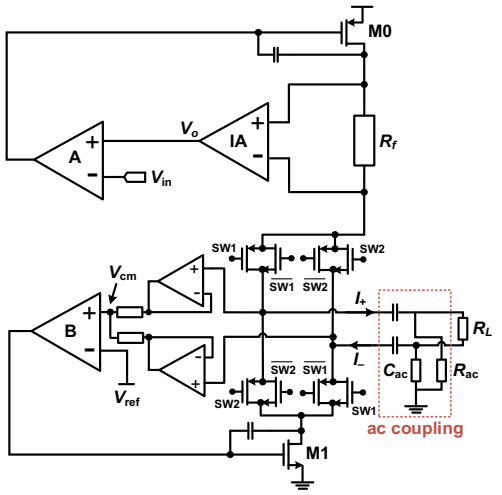


Fig. 2. Circuit implementation of the H-bridge current driver.

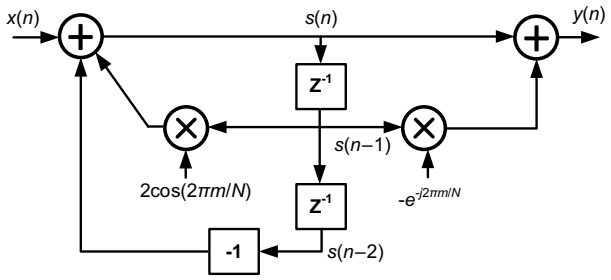


Fig. 3. IIR filter structure of the Goertzel algorithm.

B. Goertzel Filter

Traditionally, demodulation is performed using an FFT or coherent demodulation. The FFT is a very efficient way of computing the Fourier transform when a large number of bins is required. However, bio-impedance measurements require fewer than 20 bins for acceptably accurate estimation [5], wasting most of the computed bins. FFT can perform demodulation only for integer bins, and thus is inaccurate when used with optimal tones distribution [9]. The FFT algorithm requires N samples simultaneously, and memory is dedicated to this storage, increasing the resource cost. In addition, FFT computation adds delay, which can be problematic for applications requiring a very high measurement rate. The other method, coherent demodulation, can be realized either in the analog or digital domain. The analog version offers good performance and low power consumption. However, complexity greatly increases when simultaneous multi-frequency is required [10]. Cross coupling between frequencies decreases the accuracy, especially at high frequencies. Also, this approach suffers from lack of flexibility. The digital version of coherent demodulation overcomes the accuracy and flexibility issues but at the expense of large memory requirements. Sine and cosine values for each frequency points must be stored in lookup tables. In addition, this method suffers from harmonic fold back, decreasing accuracy due to harmonic distortion.

The Goertzel filter is an alternative to these two commonly used methods. It performs the complex demodulation for each frequency point desired. It was reported in 1958 by Gerald Goertzel [6] and was initially developed as an efficient way to compute trigonometric functions. It also provides an efficient way to compute discrete-time Fourier transform (DTFT) with only two coefficients. The DTFT of a discrete N samples signal $x(n)$ can be rewritten in a recursive form:

$$y(n) = W_N^m y(n-1) + x(n), \tag{1}$$

where $W_N^m = e^{\frac{-2j\pi mn}{N}}$, $n \in [0, N]$, $y(-1) = 0$, and $x(N) = 0$.

Thus, when $n = N$:

$$X(m) = y(N) \tag{2}$$

where $X(m)$ is the DTFT of the signal $x(n)$ evaluated at the bin m after N samples. The z-transform of the recursive equation yields the following transfer function:

$$\frac{Y(z)}{X(z)} = \frac{1 - W_N^m z^{-1}}{1 - 2\cos\left(\frac{2\pi m}{N}\right) z^{-1} + z^{-2}}. \tag{3}$$

TABLE I
DIGITAL COST COMPARISON WITH OTHER METHODS

Method	Real multiplications	Real additions	Memory required
Coherent demodulation	$2NK$	$2NK$	$2NK$ samples
FFT	$N\log_2(N)$	$N\log_2(N)$	N samples $N/2$ coefficients
Goertzel filter	$(N+2)K$	$(2N+1)K$	$3K$ coefficients

which is realized using the structure shown in Fig. 3. The filter can be separated into two parts: a second-order infinite impulse response (IIR) filter with one real multiplication, and a feedforward path using one complex multiplication. The filter part is performed N times (with $x(N) = 0$), whereas the feedforward can be performed only once, for $s(N)$. In total $N + 2$ multiplications and $2N + 1$ additions are required. Three coefficients are stored: one for the recursive part and two for the feed-forward part, with complex multiplication (real and imaginary part coefficients). The computation time for estimating a frequency point is $(N + 1)T_s$, where T_s is the sample period. Thus, once the N sample input signal is acquired, the Goertzel filter adds one sample period delay before outputting a demodulated frequency point.

Table I provides a comparison of the digital cost (number of operations and memory requirement) for coherent demodulation, FFT and Goertzel filter. K is the number of bins being demodulated simultaneously. The Goertzel filter requires about half the number of multiplications than the traditional coherent demodulation and the same number of additions. The memory requirement for Goertzel filtering is very advantageous as it stores only three coefficients per bin. To further reduce memory requirement, only the IIR part can be embedded in the digital logic. Once the N samples are processed, $s(N)$ and $s(N-1)$ are transmitted to a computer to perform the last complex multiplication and process the data. This reduces N samples to two values for each bin to be transmitted (identical to the coherent modulation and FFT) while requiring to store only one coefficient. The Goertzel filter can accurately estimate the frequency content for a non-integer bin by applying a simple correction factor after the feedforward path [11]:

$$y(n)_{corrected} = y(n)e^{-j2\pi m}. \tag{4}$$

It should be noted that because the filter is resonating around the bin of interest [12], this demodulation method does not suffer from harmonic fold back problems.

C. Implementation of the Goertzel Filter

Despite the simplicity of the proposed algorithm, its circuit implementation is challenging. The influence of fixed-point arithmetic has to be assessed and a suitable digital architecture designed to minimize the digital resources required.

1) Overflow

Because of the registers' finite length in fixed-point implementation, overflow can occur when the internal value exceeds the maximum possible value, causing large errors at the filter output. Because its poles lie on the unit circle, the Goertzel filter output tends to increase rapidly. It is shown in [13] that

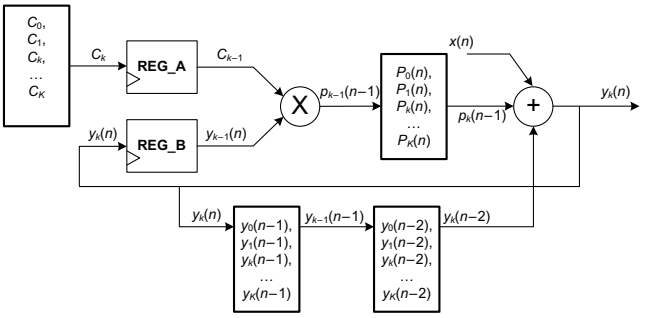


Fig. 4. Digital implementation of the Goertzel filter.

the relationship between the maximum input value x_{max} and the filter output $y(n)$ can be expressed as:

$$x_{max} < \frac{|y(n)|}{\sum_{\tau=0}^{N-1} h(\tau)} \tag{5}$$

where $h(\tau)$ is the impulse response of the Goertzel filter. From (5), the required register length can be evaluated. This number increases quite rapidly, but the filter does not require a large number of samples for an accurate estimation (typically a few hundreds). Note that each register is reset after the N-sample sequence. For this design, 32-bit length registers were chosen, each providing up to 4096 samples.

2) Round-Off Error

When multiplying two integers using finite precision, the required output register length increases dramatically. To overcome this the output value is scaled down by fixed-point division. This division introduces quantization noise [14], called the *roundoff effect.* Assuming this noise is uniform, additive and uncorrelated, the total injected power of the noise is:

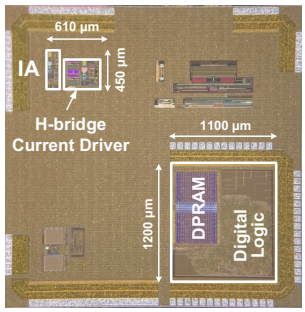
$$\sigma_{tot}^2 = \sigma_{ADC}^2 + \sigma_{scaling}^2 \tag{6}$$

where σ_{ADC}^2 is the quantization noise present in the input signal and $\sigma_{scaling}^2$ is the quantization noise introduced by the fixed point multiplication. Therefore, if the coefficient precision is chosen large enough in comparison to the length of the input data, the noise due to scaling can be neglected. The architecture in this design uses 22-bit precision for the coefficients.

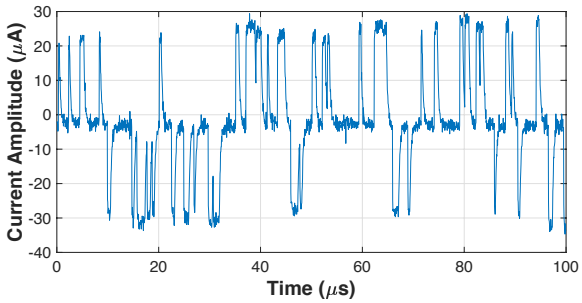
3) Digital Implementation

Digital implementation of IIR filters has been thoroughly studied in the literature, and when pipelined with "look-ahead" architecture allows fast and highly parallelized design [15]. However, these structures require multiple parallel multiplications. This increases the resources required and can cause overflow issues, especially with the Goertzel algorithm. In the implementation shown in Fig. 4, the architecture takes advantage of parallelizing and pipelining by using one single filter to compute the complex value for different bins.

The filter is clocked K times faster than the sampling frequency, allowing K multiplications and K additions for K bins to function between two input samples. Computation is parallelized, the multiplication for the bin k is computed at the same time as the addition for the bin $k + 1$. REG_A and REG_B are input registers for the multiplier cell. This structure



(a)



(b)

Fig. 5. (a) ASIC micrograph with on-chip DPRAM, digital logic including Goertzel algorithm and H-bridge current driver. (b) Ternary current generated by the ASIC.

allows demodulation of 16 bins at 5 MSps with a 40 MHz system clock.

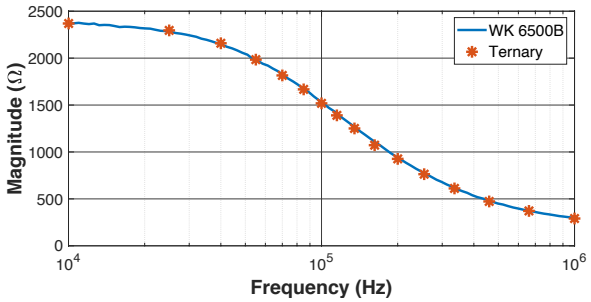
III. Measured Results

A. System Performance Evaluation

The ASIC shown in Fig. 5(a) was implemented in a 180-nm CMOS technology. The measured bandwidth of the H-bridge current driver was 1 MHz for a load impedance of up to 50 kΩ. The peak-to-peak output current ranges from 50 µA to 1 mA. To test the autozero performance, a 10 kΩ resistor was used as the load after two 100 nF ac coupling capacitors (C_{ac}) and two 1 MΩ pulldown resistors (R_{ac}) as shown in Fig. 2. The H-bridge current driver generated 156 kHz, 100 $\mu A_{p\text{-}p}$, 50% duty cycle square wave current continuously for 5 hours. The measured dc voltage across the load resistor was 160 µV, indicating a dc current of 16 nA.

To demonstrate the accuracy of the Goertzel filter-based EIS system, an impedance was measured using ternary broadband excitation. A classic 16-multisine signal with a BQL distribution [5] from 10 kHz to 1 MHz was first generated. Then, the signal precision was reduced to 3 levels: -25 μA, 0 and +25 μA (Fig. 5(b)). The measurement was realized over 250 µs, which is 2.5 cycles of the lowest frequency, with the first cycle for settling. Each relative phase was individually tuned to decrease the crest factor [5]. The load was a RC composed of a (2200 Ω || 4.7nF) in series with a 150 Ω resistor.

The resulting signal was sampled at 5 MSps. The measured impedance spectrum was compared to that obtained with a Wayne Kerr 6500B impedance analyzer. Phase and magnitude results are shown Fig. 6. The maximum measured error is about 10 Ω (3%) and 2° (4%) at 1 MHz. SNR was estimated from the method described in [5]. It is about 65 dB at 10 kHz and



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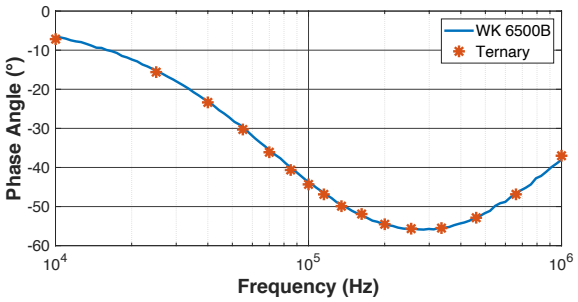

(b)

Fig. 6. Measured magnitude (a) and phase (b) of the RC load with the proposed system using ternary excitation current, compared with results from a WK 6500B impedance analyzer.

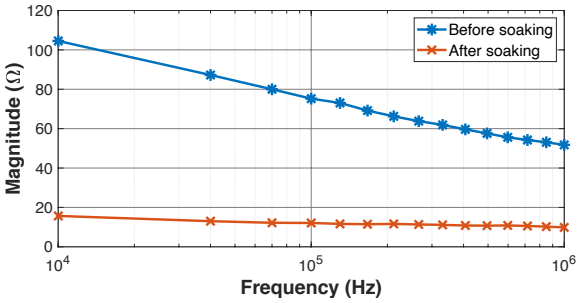

Fig. 7. Impedance of the pig's heart before and after soaking in PBS.

decreases to 48 dB at 1 MHz. The Goertzel filter is able to demodulate the highly degraded multisine excitation ternary current nearly as precisely as an accurately synthesized multisine waveform. The same measurement was performed with 12-bit multisine excitation current. The result was only 0.2% different from that using ternary current.

B. Ex-Vivo Measurement on Isolated Pig Heart

The system was evaluated on an ex-vivo isolated pig heart using a tetrapolar EIS configuration. Four TME-2 67T pacing wires (Osypka Medical, Germany) were used as electrodes with their needles placed in a straight line 4 mm apart. In this configuration, the outer electrodes were used for current injection, and the two inner electrodes for voltage measurement. The excitation current was the same ternary sequence described in Section III A and Fig. 5 (b), with an amplitude of 50 $\mu A_{p\text{-}p}$. To simulate edema in the tissue the pig heart was soaked in phosphate-buffered saline (PBS) for one hour. Impedance measurements were taken before and after the soaking. Results are shown in Fig. 7. The system was able to detect small changes in impedance, and a shift in the impedance value was clearly observed before and after soaking. The shift

TABLE II COMPARISON WITH OTHER WORK

Parameter	[16]	[17]	[18]	[19]	This Work
Technology	FPGA	FPGA	0.35 μm CMOS	0.35 μm CMOS	180 nm CMOS
Excitation waveform	Swept-sine	Multisine/ swept-sine	Multisine	Swept-sine	Ternary
Demodulation method	FFT	I/Q	Analog I/Q	MP-D[a]	Goertzel filter
Simultaneous demod. freq.	1	N/A	2	1	16
Bandwidth (kHz)	0.1–500	<1000	0.1–1000	1×10^{-7}–100	<1000
Power (mW)	N/A	N/A	3.4[b]	0.32	12

[a]Magnitude and phase detection; [b]per channel.

represents the absorption of the fluid by tissue, similar to edema.

C. Power Consumption

The ASIC has a DPRAM memory for storing the ternary excitation waveform. The measured power consumption of the digital logic was 9 mW when idling and 12 mW when continuously performing measurements. The current driver and IA consume 45 µW and 660 µW, respectively.

IV. DISCUSSION AND CONCLUSION

Table II provides a comparison with other work. The system and implementation presented here aim to demonstrate simultaneous complex demodulation using a Goertzel filter. The method provides accurate results over a wide bandwidth (10 kHz to 1 MHz) demanding very little memory and digital resources. It requires to store only one coefficient per demodulated bin, and four multipliers for the demodulation of 16 bins. Furthermore, the Goertzel algorithm provides instantaneous frequency demodulation of the recorded signal. With a 250 µs measurement time window this system is able to compute up to 4000 impedance spectra per second. In addition to its simplicity, the Goertzel algorithm has the major advantage of being insensitive to harmonic fold back, allowing the use of a low-resolution excitation waveform such as the ternary sequence shown in Fig. 5(b). Without compromising the SNR, the implementation of the waveform generator requires only 2 bits, greatly reducing the memory requirement, and hence resulting in less power and area consumption.

To assess the relative performance of digital demodulation methods, a figure of merit (FOM) was proposed in [20]:

$$\text{FOM} = (\text{Power}) \times (\text{Measurement Time}) \times (\text{Error }\%)^2. \quad (7)$$

Assuming a maximum 4% measurement error, thanks to its very fast demodulation capabilities, while maintaining good accuracy and reasonably low power consumption, the proposed architecture has a FOM of $0.048\ \text{mJ}.\%^2$, showing nearly twice the FOM of the method in [20].

The ternary excitation current can be generated using a simple H–bridge current driver rather than a linear driver [21]. This reduces the circuit complexity of the current driver and its power consumption. The integrated H-bridge current driver consumes only 45 μW of power. Future integration of the ADC will provide a complete, low power single-chip solution for broadband EIS.

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