Indium Phosphide Photonic Circuits on Silicon Electronics

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Abstract: The intimate integration of photonics and electronics in transceivers facilitates energy-efficiency, bandwidth acceleration and a route to radical miniaturization. We present and implement a wafer-to-wafer integration method which combines electronic and photonic foundry technologies.

1. Introduction

The motivation to integrate electronic and photonic systems [1] in an aligned manufacturing process is long-standing, but this now becomes a necessity with the sub-systems envisaged for future data center technologies [2], light based detection and ranging [3], and future, high-density neuromorphic and programmable photonics. High-speed, high-density, low-energy, electrical interconnects within transceivers also enable performance advances through feed-forward equalization [4], optical serialization [5], equalization [6], and driver voltage reduction [7].

Photonic transceivers require precision DC biasing and wideband impedance matching to ensure data integrity. Historically separately-designed photonic and electronic chipsets have been implemented with bias tees and 50 Ω interfaces to facilitate interoperability and tractable design, but this is no longer attractive as speeds increase within a restricted energy envelope. Components need to be placed closer together within the package, towards a combined 3D assembly and ultimately within the same processed wafer. Researchers are actively exploring a range of schemes for the integration and embedding of photonic circuits within electronic systems. Silicon modulators have been integrated within silicon electronics [8-11]. Indium phosphide (InP) electronics and InP photonics have been monolithically integrated [12]. InP remains the material system of choice for efficient light sources and the highest-performance modulators in telecommunications, motivating the integration of InP circuits with silicon through a range of wafer-bonding methods [13-14]. However there has been relatively little work on the intimate integration of InP photonic integrated circuits with silicon electronics. The decision on which components to place in InP technology and silicon technology is fraught with technological and commercial uncertainties. Advanced CMOS processes evolve at such a pace and are used in such high production that it may be impractical to monolithically integrate photonic designs and re-port to the latest technology nodes. The need to produce in fabs which are not sized for the addressed markets may also add unacceptable cost. In our approach, we integrate the complete photonic integrated circuit within foundry-sourced InP and combine with electronic circuits in silicon.

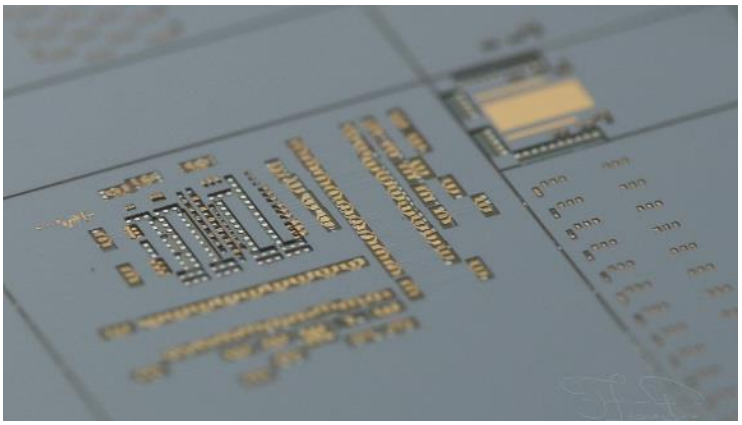

Fig 1. Indium phosphide photonic integrated circuit membrane wafer bonded to a BiCMOS wafer including the electronic interface

The foundry model for producing integrated circuits has long existed for electronics and this is now becoming established for photonic integrated circuits [15]. It is now technologically feasible to produce application specific designs with small series foundry processes for both technologies, motivating co-designed, foundry-produced electronic and photonic systems. We use InP PICs to allow for sustained reductions in energy and footprint and increase in bandwidth as the technology platforms evolve [16], and silicon electronics as a widely accepted commercial solution with highly-developed process design kits. Our approach extends the wafer bonding methods developed for our nanophotonics platform [13] to foundry-sourced InP PIC wafers, electronics and the associated co-designed devices. We present the co-designed EAM/drivers and MZM/drivers, demonstrate interoperability, and

present wafer-to-wafer assembly methods for increased bandwidth, with reduced loss interconnection. Figure 1 shows our first wafer-to-wafer assembly demonstration.

2. Die-to-die assembly of co-designed circuits

Electro-absorption modulators (EAM) have been produced using advanced foundry platforms and are demonstrated with data rates of 64Gbit/s and beyond [17-18]. These are used in combination with the bespoke drivers. A 2 × 56 Gb/s PAM-4 dual-channel EAM driver has been designed and produced in a 0.25-µm SiGe:C BiCMOS process [19] and delivers a maximum of 2 V peak-to-peak amplitude when single-ended connection is made. The driver is DC-coupled to the optical modulator, enabling a simple bond-wire connection between electronic and photonic chips. Concepts have been devised to remove the bias T and obtain a tunable output voltage at the output of the driver [20]. The EAM operates in the L-band at 1590 nm, with a DC bias set at –1.6 V for on-off keying non-return to zero modulation. Fig 2 shows the experimental layout and the measured eye-diagrams for a data rate of 20 Gbit/s and 36Gbit/s [21]. The reduced bandwidth relative to the individual component performance is primarily attributed to the bond-wire and bond-pad reactances.

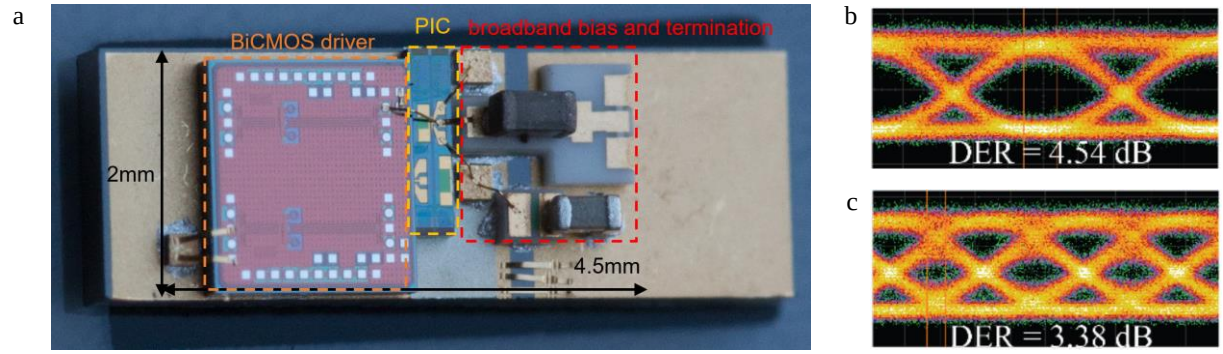

Fig 2: *Direct die-to-die connection for electro-absorption modulator-driver combination operating with 20Gbit/s and 36Gbit/s modulation.*

Phase modulators using InP, multi-quantum-well (MQW) designs have been demonstrated with 40 Gbit/s Mach-Zehnder modulator (MZM) performance with a foundry process, and have been reported elsewhere [22]. A low-power, high-efficiency, linear driver has been developed in the same 0.25 µm SiGe: C BiCMOS technology for this class of optical modulator. The driver features a small-signal gain of 18 dB, and a 3-dB bandwidth of 40 GHz and delivers a maximum output amplitude of 4 V peak-to-peak to a 100 Ω differential load. With inductor-peaking, this driver achieves 34 ps ± 3 ps group delay from DC to 50 GHz. In time-domain measurements, this driver achieves a measurement platform limited symbol rate of 56 Gb/s NRZ and 28 Gbaud PAM4 [23]. Die-to-die interfacing will be reported.

3. Wafer-to-wafer bonding of integrated circuits

The wafer-to-wafer bonding of pre-defined circuits requires a methodology to (i) accommodate topography on both the electronic and photonic wafers, (ii) ensure accurate alignment between electronic and photonic circuits and (iii) provide electronic connection between circuit elements. Benzocyclobutene (BCB) polymer is used for the bonding material owing to its adhesion quality, low dielectric constant and compatibility with Si and InP industries [24]. A low resistance metal interconnection technique has been devised and validated for carrying the high speed RF signals [25]. Fig. 3 shows process module validation for creating electrical vias between the Si and InP. The BCB layer is opened, patterned and subsequently plated to create low resistance interconnects between the top and bottom surfaces. Details in Fig 3 show break-free connection and uniform metal thickness. Daisy-chained DC test structures show unmeasurably low excess resistance due to the vias indicating that the resistance is dominated by the gold tracks. The process module has subsequently been integrated into the full process flow to include the assembly of foundry-sourced PIC and BiCMOS wafers.

Fraunhofer HHI and NXP Semiconductor produced the integrated circuit wafers containing the ICs for the photonics and electronics respectively. The electronic ICs are as specified in section 2. The completed wafer-scale assembly is shown in Fig 1. High-frequency test structures are on the left and a functional circuit on the right. At this specifc location an optical receiver is shown. The RF test structures give measurement limited bandwidths of 67GHz for lengths up to 1mm.

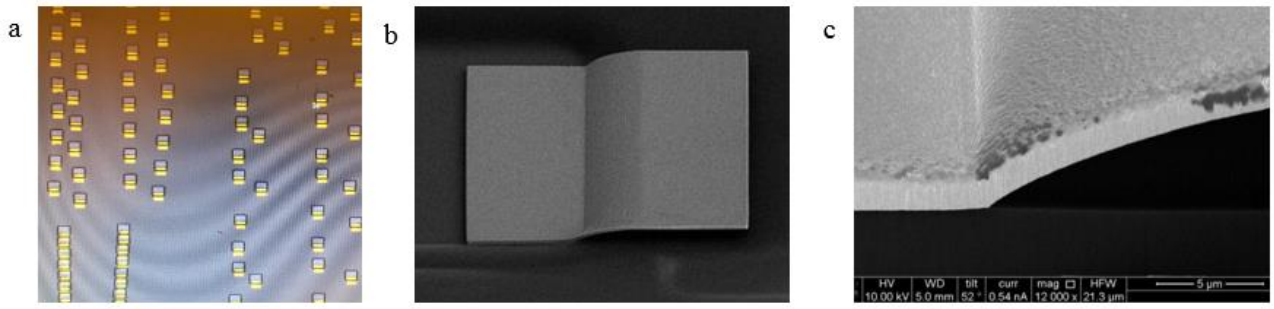

Fig 3: Through polymer vias with a) completed process module showing top-to-bottom-surface electrodes connection b) one via with dimensions 116×116 µm² and c) detail of via to show break-free connection.

4. Summary

Electronic and photonic components and circuits have been designed for high speed interoperability, with leading-edge-performance using foundry processes. These have been separately assessed with 40Gbit/s performance, as well as in combination using direct die-to-die assembly with only short bond-wires and bond-pads between the circuits. This does compromise bandwidth, motivating a wafer-to-wafer method to assemble these circuits. This has been validated, and characterization of the interconnects indicates that low-loss broadband interconnection is feasible. The first wafer-to-wafer bonded, co-designed circuits have been created and insights will be presented.

5. Summary

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6. References

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