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DESIGN OF LINEAR AND NONLINEAR CIRCUITS USING DERIVATIVE SUPERPOSITION

By

Gholamreza Ataei

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ABSTRACT

Modern communication systems require a wide variety of linear and nonlinear circuits such as power amplifiers and frequency multipliers. The derivative superposition (DS) technique has been proposed for the design of linear and nonlinear circuits. A DS circuit uses a number of field effect transistors (FETs) in parallel with each other and having different gate widths and operating points. This allows the designer to control the shape of the transfer characteristic to meet a particular linear or nonlinear specification. This technique has been chosen to be the subject of the work in this thesis.

It is shown that a MMIC DS power amplifier using a novel phase reversal form of DS achieves a two tone carrier to interference ratio (c/i) of 45 dBc with an efficiency of 22.5 % close to 1 dB compression around 0.5 GHz providing a better compromise between linearity and efficiency than conventional single amplifier classes. A novel composite Doherty-DS structure is proposed which is capable of providing a wider dynamic range for better c/i performance close to 1 dB compression and a good compromise in terms of efficiency compared to those of either the Doherty or the DS amplifiers alone.

The DS approach is used to design a nonlinear function circuit for a quasi-optical tracking system and a MMIC frequency tripler design which achieves a considerable suppression of unwanted frequency products. A refined version of the DS frequency tripler is proposed which employs a rat race coupler for operation well into the microwave region.

During this work some improvements were made to the set-up for the intermodulation distortion measurements of FETs, a study of factors affecting distortion of various FETs was carried out and a visualisation technique was developed for mapping the distortion of a FET allowing identification of an optimum bias and loading condition.

Acknowledgements

I wish gratefully to thank my supervisors Dr. David Haigh and Dr. Danny Webster who made this work possible. Dr. Haigh, for his endless support, enthusiasm, encouragement and proof reading and always being willing and available for discussion despite his hectic schedule during the period of this thesis. Dr. Webster, for his continuous technical support, inspiration, encouragement and never ending enthusiasm and always being eager and available for discussion despite his busy schedule throughout the period of this thesis.

I would like to thank Dr. Paul Brennan for his very helpful comments on the M.Phil. to Ph.D. transfer thesis.

I would like to thank my fellow Ph.D. student and friend Mervin Hutabarat for useful discussions during this work.

I wish to extend my thanks to all my friends who have given me their support and provided me with much needed comfort away from the academic life.

Lastly, but by rights first, I would like to thank my parents and sisters for their patience, support and love throughout the period of this thesis.

به پدر و مادرم

از برای عشق بیکران

"هل یستوی الذین یعلمون و الذین لا یعلمون إنما یتذکر أولوا الألباب"

(سوره الزمر، آیه ۹)

علم تقلیدی برد بهر فروخـــت
چون بیاید مشتری بر فروخـت

مشتری علم تحقیقی حق است
دایما بـــازار او بـا رونـــق است.

(مثنوی معنوی، دفتر دوم، ابیات ۳۲۶۵و ۳۲۶۶)

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Chapter 1

Introduction

1.1 Linear and Nonlinear Circuits in Modern Communication Systems

In modern communication systems there is an increasing need for linear and nonlinear circuits of several types depending upon application. Linear power amplifiers are needed in most applications. The need for linearising, in the case of a power amplifier for example, arises from the fact that when multiple inputs are applied to a nonlinear device frequency components not present in the input signal will be generated at the output. These new frequency components are referred to as harmonic and intermodulation distortion products. These distortion products can cause interchannel interference in multi-channel communication systems. In general, it is the 3rd order and other odd order intermodulation distortion products which have the most significant effect, as they lead to the generation of interfering signals which are close to the parent tones within the passband of the system. 2nd order and other even order distortion products are of less concern since these products are usually out of band and can be removed easily by filtering strategies.

Examples of nonlinear circuit applications can be found in limiters, frequency doublers, frequency triplers, mixers and triangle to sine wave converters.

Many circuit design approaches are available for designing both linear and nonlinear circuits. An approach recently proposed which is compatible with microwave frequency applications and considered worthy of more detailed study is derivative superposition.

1.2 Derivative Superposition Approach

A derivative superposition (DS) circuit [1], [2], [3] consists of a set of FETs connected in parallel with different gate widths and with different DC offsets from a common gate bias voltage. The same RF drive is applied to each device. As we shall see in Chapter 2 of this thesis, the nonlinearity of a FET can be described by its transconductance and its transconductance derivatives. A FET has peaks in its first and second transconductance derivatives g_2 and g_3, respectively, and a sign reversal in g_3 as a function of gate bias. The derivative superposition technique can combine these derivatives with the correct value of phase and amplitude in order to achieve a desired linear or nonlinear transfer characteristic.

Derivative superposition has been successfully used previously to design low distortion small signal amplifiers [3], [4]. Derivative superposition has also been used to design frequency doublers and triplers [5].

1.3 Aim of Project

In this work it is aimed to design more demanding MMIC versions of linear and nonlinear circuits using the derivative superposition technique. For the linear circuit a DS power amplifier is attempted with the aim of achieving low 3rd order intermodulation distortion at high input power levels close to 1 dB compression. Nonlinear circuits based on the derivative superposition technique are also attempted. These include the application of DS technique to realise a nonlinear function circuit required for a quasi-optical tracking system. Improved frequency triplers are also designed for operating in the microwave frequency range.

1.4 Statement of Collaboration

The following paragraphs state the portions of the work which are carried out in collaboration with others.

The use of the new load resistor configuration for low distortion measurements (Sections 4.3.1 and 4.3.2) was carried out in collaboration with Mervin Hutabarat.

The idea of the bias tee arrangement (Section 4.3.3) was suggested by Dr. Danny Webster and carried out in collaboration with Mervin Hutabarat.

The idea of trying to produce a new visualisation technique for optimum design of amplifiers (Section 5.5) was suggested by Dr. Danny Webster.

The basic design work on a nonlinear function circuit to be used in a quasi-optical tracking system (Chapter 6) was carried out in collaboration with Dr. Danny Webster.

The idea of the use of the sign reversal technique with derivative superposition for the design of power amplifiers (Section 7.2) was originally suggested by Dr. Danny Webster.

The idea of a composite Doherty-DS structure (Section 7.3) was originated by Dr. Danny Webster.

Use of derivative superposition for designing frequency triplers (Chapter 8) was first proposed, in a basic form, by Dr. Danny Webster.

All other work described in this thesis, apart from review materials referenced to the open literature, is the sole work of the author.

1.5 Review of Chapter Contents

The work presented in this thesis is divided into several chapters. In the following sections we will briefly described the contents of these chapters.

In Chapter 2 we will give an overview of GaAs technology together with some of the advantages of this technology. Then, we give a description of some of the most frequently used terminology in nonlinear analysis. Then, some of the most popular nonlinear analysis techniques including time domain techniques, harmonic balance and Volterra series analysis will be discussed. Following that some of the most common nonlinear device characterisation techniques will be described. Then, a description of some of the most popular simulator models will be given.

In Chapter 3 we will look at some general requirements for linear and nonlinear circuits which arise in practical systems. We will examine the common-source FET amplifier paying attention to its distortion generation mechanism and some of the factors influencing its distortion characteristics. Then, the distributed amplifier will be discussed. The derivative superposition technique based on common-source amplifiers as a mean of linearisation will be discussed and a derivative superposition amplifier using high-pass transmission lines will be reviewed [4]. A comparison of linearisation techniques for small and medium signal applications and nonlinear applications will be presented and some of the most frequently used linearisation techniques for power amplifiers will be discussed.

In Chapter 4 we will consider some of the problems involved in the measurement of intermodulation distortion (IMD) in more detail. These include the problems of residual distortion and use of a high impedance probe to provide a load to a

device under test other than 50 Ω. We will then discuss ways of reducing residual distortion and ways of avoiding the use of a high impedance probe by a load resistance configuration which avoids the introduction of associated distortion and noise. Then, we will present a way of improving intermodulation distortion measurement results obtained by on-wafer measurement of IC chip devices. Finally, we will report the development of a high frequency distortion measurement set-up for operating frequencies of around 0.5 GHz which uses a rat race coupler.

In Chapter 5 we will first investigate some of the factors which influence the intermodulation distortion performance of a FET using SPICE. These factors include the gate and drain bias points, voltage gain and the effect of input power levels. Then, detailed measured intermodulation distortion performances of some sample FETs including MESFETs, HEMTs, MOSFETs and Si-JFETs will be compared and discussed. Then, we will show that by using a nonlinear mapping technique with a suitable graphical interpretation, it is possible to identify low distortion regions of operation whilst still giving small signal matching [6].

In Chapter 6 we will apply the derivative superposition technique to a nonlinear circuit which can be used in a quasi-optical tracking system [7], [8]. We will discuss the development of a nonlinear function circuit required for a quasi-optical tracking system application. Derivative superposition [1], [2], [3] will be used to realise this nonlinear function circuit [8] to generate a conjugate phase beam for the quasi-optical system. Due to delays at the University of Glasgow, none of the submitted circuit designs for this particular application have been fabricated.

In Chapter 7 we propose a novel form of the derivative superposition technique for the design of MMIC power amplifiers. We first present some distortion measurements carried out in order to characterise a MMT F20 FET device. Then, a Parker Skellern model [9], [10], [11], [12] is extracted for simulation purposes. Then, we describe the derivative superposition strategy used for this design [5]. Results of simulation using Super Deriv [13] will be presented. These include spectral regrowth and adjacent channel power ratio (ACPR) simulations. Then, the measured performance of the MMIC DS power amplifier will be studied including single and two tone efficiencies and two tone carrier to interference ratio performance. The effect of load resistance, drain bias and voltage offset on distortion will also be studied. Then, some simulations will be carried out on the Doherty circuit [14], [15], [16]. We then, explore the possibility of designing a composite Doherty-DS amplifier. The simulation results of carrier to interference ratio and efficiency for a reference FET, the Doherty circuit, the DS circuit and the composite Doherty-DS structure will be presented.

In Chapter 8 we will demonstrate the possibility of designing frequency triplers with the derivative superposition method both for 100 MHz and microwave frequency operation. The circuit for the lower frequency of operation uses a differential pair for the required subtraction whereas, the design for the microwave frequency operation employs a rat race coupler. The design procedure and the simulated performance of the frequency triplers for both 100 MHz and microwave frequency operation will be presented.

In Chapter 9 we draw general conclusions of the work presented in this thesis and some possible future work will be outlined.

1.6 List of Publications

The author has contributed to the following publications.

1. D R Webster, G R Ataei, A Assenov, D G Haigh and I Thayne, "Reduction of 3rd-order Intermodulation Distortion through the use of a High Pass Transmission Line Implementation of Derivative Superposition and through the use of Channel Dopped HEMTs", *IEE Colloquium on Analogue Signal Processing*, 20th November 1996, Oxford, U.K.

2. D R Webster, G R Ataei, D G Haigh and Risto Kaunisto, "Factors Influencing Intermodulation Distortion Performance of a FET", *IEEE High Performance Electron Devices for Microwave and Optoelectronic Applications Workshop*, November 1997, London, U.K.

3. D R Webster, G R Ataei and D G Haigh, "High-Pass Lumped-Element Transmission Lines", *IEEE Microwave and Guided Wave Letters*, Vol. 8, No. 1, January 1998.

4. D R Webster, G R Ataei, A E Parker and D G Haigh, "Developments in Linear and Nonlinear FET Circuit Design using Derivative Superposition", *IEE Oxford Brookes*, November 1998, U.K.

5. D R Webster, A E Parker, M Hutabarat, G R Ataei, D G Haigh and P Radmore, "Experience of Developing and Using CAD Tools For III-V FETs Effectively in a Nonideal World", *IEE Colloquium on Effective Microwave CAD Tools*, May 1999, London, U.K.

6. G R Ataei, "Low Distortion Power Amplifier Using Derivative Superposition", *PREP 99*, January 1999, Manchester, U.K.

7. D R Webster, K van der Zanden, G R Ataei, M T Hutabarat, D Schreurs and D G Haigh, "Large Signal Frequency Dispersion Effects in Indium Phosphide HEMTs", *IEE Colloquium on Advances in Semiconductor Devices*, January 1999, London, U.K.

8. D R Webster et al. "Observations on the Nonlinear Behaviour of Single and Double InGaP/GaAs HBTs", *EDMO'99 - The 7th IEEE International Symposium on High Performance Electron Devices for Microwave & Optoelectronic Applications,* King's College London, London, UK - 22-23 November 1999.

9. D R Webster, G R Ataei and D G Haigh, "Low Distortion MMIC Power Amplifier Using a New Form of Derivative Superposition", *Submitted to IEEE Transactions on Microwave Theory and Technique.*

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[6] D R Webster, G R Ataei, D G Haigh and Risto Kaunisto, "Factors Influencing Intermodulation Distortion Performance of a FET", *IEEE High Performance Electron Devices for Microwave and Optoelectronic Applications Workshop*, 1997, London, U.K.

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Chapter 2

Background

2.1 General

In this chapter we will first give an overview of GaAs technology together with some of the advantages of this technology. Then, some of the passive and active devices used in GaAs technology will be discussed. After that we will give a description of some of the most frequently used terminology in nonlinear analysis. Then, some of the most popular nonlinear analysis techniques including time domain techniques, harmonic balance and Volterra series analysis will be discussed. Following that some of the most common nonlinearity characterisation techniques will be described. Finally, a description of some of the most popular simulator models will be given.

2.2 GaAs Devices and Technology

Gallium Arsenide (GaAs) has evolved in many industrial and research laboratories over the past three decades. The fabrication of stable high resistivity GaAs material was made possible by the development of the Liquid-Encapsulated Czochralski (LEC) method of growing GaAs ingots [1]. The research into the fabrication of GaAs based transistors was first carried out by Jim Turner at Plessey Research (Caswell). This led to the development of GaAs bipolar transistors and later on triggered interest for the fabrication of GaAs field effect transistors [2]. The earlier devices had a gate length of 24 μm and produced power gain in the VHF region. A 4 μm gate length transistor was fabricated in 1967. This device was capable of producing 10 dB gain at 1 GHz and it became the first commercial device, called the GAT1. The GAT1 was marketed by Plessey Optoelectronics and Microwave Ltd. Later on in 1971, the first 1 μm device was developed by using the electron

beam lithography method. This device was capable of producing gain at 10 GHz and it was marketed as GAT3.

The integration of semiconductor devices and circuits was reported in 1968 by Texas Instruments. Later on in 1984 the first complete analogue GaAs IC foundry appeared producing 14 GHz FETs.

GaAs based technology progressed gradually by making use of new processing steps. These steps included the dry etching technique which selectively etches III-V materials. Use of the Molecular Beam Epitaxy technique opened up the possibility of growing layers of a few molecules thick on a substrate.

The improvement in GaAs technology caused the emergence of various kinds of hetrostructure based devices. These include Hetrojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs).

Having stated a brief history of GaAs based technology, we will next discuss the properties of the GaAs substrate which make it attractive. Then, we will describe some passive and active GaAs devices.

2.2.1 Advantages of GaAs

Gallium Arsenide (GaAs) as a semiconductor material has many advantages over the widely used silicon. The high electron mobility (about six times larger) and high saturated drift velocity of GaAs compared to silicon enables GaAs semiconductor devices to operate at higher frequencies than silicon devices. The hole mobility of GaAs is much lower than its electron mobility. Since GaAs is mainly used for high frequency applications, p-type devices are not normally encountered.

The energy gap of GaAs is higher than that of silicon. This relatively high energy gap makes the intrinsic material semi-insulating. The high substrate resistance and fast operation make GaAs a very suitable device for the integration of complete microwave circuits.

In GaAs a low energy state exists at low velocities in all directions in the conduction band that makes photo emission and photo ionisation very efficient processes. This phenomenon is called direct recombination. On the other hand, in silicon due to indirect recombination the process is not as efficient.

GaAs devices are more radiation tolerant than silicon MOS devices. This is due to the fact that the higher energy gap of GaAs compared to silicon leads to lower noise from thermal ionisation in the bulk and a greater resilience to ionisation from external radiation sources.

Finally, many GaAs MESFET processes have quite simple fabrication requirements compared to silicon based fabrication.

2.2.2 Passive Devices

In an MMIC circuit there is usually a need for passive components. The passive components include resistors, capacitors, inductors, interconnections and transmission lines. These elements can be realised either in distributed or lumped form. Physical dimensions of distributed elements are quite large and, therefore, their functions have a strong dependence on the transmission line characteristics. On the other hand since the physical dimensions of the lumped elements are quite small, i.e. less than 0.1 wavelength in size, the transmission line effects can usually be ignored.

Having discussed some of the properties of passive elements we will next look at these elements in more detail.

Resistors

There are two kinds of resistors in a typical GaAs process. One kind is formed by lengths of nichrome metalisation. This kind of resistor is suitable for values up to 1 kΩ. The other kind of resistor is the mesa resistor. They are formed from channels of FETs lacking gate metalisation. The range of mesa resistor values is 100 Ω-10 kΩ.

Capacitors

The two most common kinds of capacitor in an MMIC process are the metal insulator metal (MIM) capacitor and the interdigital capacitor. MIM capacitors are used for higher values of capacitance and interdigital capacitors are used for very small values of capacitance. The capacitance value of the MIM capacitor depends on the plate area, plate spacing from each other and the dielectric between the plates. For MIM capacitors with smaller values there is a significant stray inductance to the ground plane.

Inductors

In an MMIC process the inductors are generally formed by planar spirals which are laid on a substrate. Their typical values range between 3-15 nH. These inductors have a large series resistance associated with them. This is due to the thin track making the spiral. Inductors have significant stray capacitance both between the turns and to ground. This leads to spurious resonances and limits the self resonant frequency of an inductor.

Interconnections

There are two types of processes for the formation of interconnections. These are 2-level metal (e.g. MMT process) and air bridge (e.g. University of Glasgow process). In most processes electrical connection between the layers of the 2-level metal can be achieved using through dielectric vias or contacts.

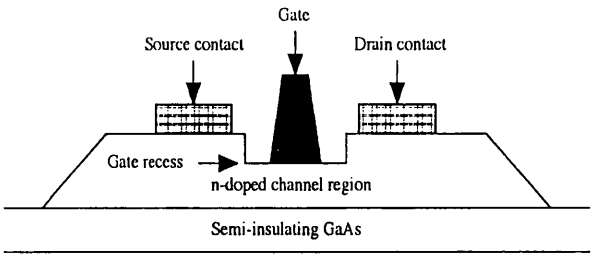


Figure 2.1: The cross section of a typical GaAs MESFET.

Transmission Lines

The most common types of transmission lines are microstrip line, thin film microstrip line, slot line and coplanar line.

The microstrip line has a metal strip and a ground plane. These are separated by an insulating substrate. The characteristic impedance is determined by the track width, the dielectric constant and the substrate thickness.

A variation of microstrip line is the thin film microstrip line. This is only available in double-level metal process. In this case the dielectric layer between the top two metalisation forms the substrate. One of the metalisation layers is used to form the ground plane. The advantages of thin film compared to conventional microstrip lines include having less stray fields and more compact layout.

The slot line is a uniplanar technique and it consists of two large conductive sheets. The characteristic impedance is determined by the slot width.

The coplanar waveguide line (CPW) is also a uniplanar structure and it consists of a track and two ground planes. The characteristic impedance is determined by the central track width and the spacing between the ground planes. The CPW has superior performance at higher frequencies than the microstrip. Another advantage of CPW is that since wafer probes are coplanar the circuits which are implemented in CPW technology are readily compatible with the wafer probes for measurement purposes.

2.2.3 Active Devices

GaAs MESFETs are extremely simple in their construction. In Figure 2.1 we present the cross section of a typical GaAs MESFET.

The FET is constructed on a semi-insulating GaAs substrate. The active n-doped layer on top of the semi-insulating layer is produced by either epitaxial growth or ion implantation. For low cost and high volume processes ion implantation is preferred. The active region for each FET needs to be separated from

that of the other FETs. This is achieved by either wet chemical etching to define mesa structures or by implant isolation which facilitates the option of a planar device. There are different orders in which the gate and the ohmic contacts are fabricated. In order to fabricate high density digital circuits with low cost, it is common to initially fabricate a high temperature stable refractory metal gate. Then the ohmic regions can be self aligned to the gate, and fired in to produce the source and drain contacts. The source and drain contacts are usually produced by photolithography and float-off techniques. The gate metal will also be defined by float-off techniques. The first task in gate processing is to define a narrow opening in a layer of resist with a suitable cross section for float-off to occur, i.e. an overhang. For gate lengths down to about 0.5 μm, this opening can be achieved by photolithography techniques. For gate lengths smaller than this, electron beam lithography or X-ray lithography can be used. Mushroom shape gates (T-gates) are quite common for short gate lengths due to the fact that they have reduced metal resistance.

The active channel thickness can be defined by etching the mesa under the gate region. This removes the need for narrow tolerance in thickness of the epitaxial layer when the channel region is not etched. A recess produces a fairly dramatic reduction in the field distribution in the channel. Once the depletion region reaches the drain side edge of the recess as the drain-gate voltage is increased, further increases in the drain-gate voltage give rise to only a very slow extension of the depletion edge toward the drain, i.e. the high field region becomes trapped by the recess edge. In power FETs, for example, the breakdown voltage between drain and gate is of great importance in determining the RF power handling capability. This breakdown voltage is improved by the recessed channel structure.

The basic structure of the High Electron Mobility Transistor (HEMT) is shown in Figure 2.2. The HEMT has superior transport properties provided by electrons moving along the two dimensional electron gas (2DEG) formed at the hetero-junction interface between two compound semiconductor materials. The spatial separation of the conduction electrons from their donor impurities reduces ionised impurity scattering. The coupling of this with low defect material produces high electron mobility and, therefore, high speed and low noise transistors are obtained. The mechanism is as follows. In a HEMT use is made of a buried quantum well running along the length of the channel. This structure allows the use of a high mobility semiconductor separated from its donor region to give high carrier velocity with minimum scattering. This gives a device with a high transconductance and very low noise. The quantum well can only hold a certain quantity of charge.

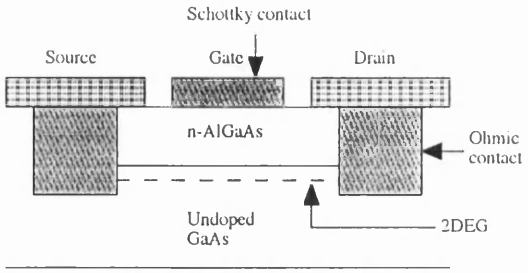


Figure 2.2: Conventional HEMT structure.

When the quantum well is full, the carriers spill over into the donor region. In this region, the carriers have a much lower velocity and have significantly higher scattering, leading to lower transconductance and higher noise. This effect is commonly referred to as the parasitic MESFET effect. For low noise, high frequency operation, mushroom or T-gate cross sections are usually used. A popular variation of a HEMT is the pseudomorphic HEMT (PHEMT). The advantage of the PHEMT is that it achieves better confinement of carriers in the channel. This gives a better noise figure and gain compared to the conventional HEMT. The noise figures of the HEMT and PHEMT are both lower than MESFETs which make them very suitable for realising low noise amplifiers.

In Section 2.2 we have presented an overview of GaAs technology. Some of the advantages of GaAs compared to silicon were outlined. Some of the passive and active GaAs devices have also been discussed. Next, we will discuss some of the issues encountered in nonlinear circuit analysis.

2.3 Nonlinear Analysis

2.3.1 Terminology

In the following sections we will give a brief description of some of the most frequently used terms in nonlinear analysis.

2.3.1.1 Concepts of Linearity and Nonlinearity

All electronic circuits suffer from nonlinearity. This nonlinear behaviour is often unwanted except for circuits such as mixers and frequency multipliers or in special cases where the nonlinearity can be exploited for specific function requirements. Simple passive elements such as resistors, inductors and capacitors are nonlinear when operated with large signals. For example the value of a resistor can change

as a result of thermal effects.

Linear circuits can be defined by the fact that they obey the superposition principle. The superposition principle states that if $x_1 \rightarrow y_1$ and $x_2 \rightarrow y_2$ then $ax_1 + bx_2 \rightarrow ay_1 + by_2$; where x_1 and x_2 are excitations to a system and y_1 and y_2 are corresponding responses and a and b are arbitrary constants.

An advantageous feature of linear time-invariant circuits is that they do not generate new frequency components, whereas nonlinear circuits usually generate a large number of new frequency components which can cause inter-channel interference in multi-channel communication systems.

The nonlinearity of circuits can either be a weak or a strong nonlinearity. The weakly nonlinear circuits can be described with sufficient accuracy by a power series expansion.

The circuits which are not fully linear but can be treated as linear for most purposes are referred to as quasi-linear circuits. These kind of circuits may include weak nonlinearity. Examples of this kind of circuit include small signal transistor amplifiers and a class A power amplifier that is not driven into saturation.

There are generally two kinds of linear component, the first one of which is a linear 1-port (e.g. a resistor). In this case we use Ohm's law $V = RI$ where R is the resistance, V is the voltage and I is the current. The other kind of linear component is a linear 2-port (e.g. a transconductance). In this case we use $I = VG$ where G is the transconductance. Since V is at a separate port it does not take any current. An example of this is a voltage controlled current source.

In general, there are three categories of nonlinear component. These include nonlinear conductance, nonlinear capacitance and nonlinear transconductance. The simplest possible nonlinear component is the 2 terminal nonlinear conductance. This is a circuit element whose terminal current is a nonlinear function of the voltage across its terminals. A practical example of such a device is the diode under forward conduction. This nonlinearity can be expressed as a Maclaurin series of the following form.

$$i(t) = g_0 + g_1 v(t) + g_2 v^2(t) + g_3 v^3(t) + ... \tag{2.1}$$

where $v(t)$ is the set of AC voltages across the element, $i(t)$ is the set of AC currents flowing through the device, and g_0 represents the DC bias current and g_1 the incremental conductance. In general g_1, g_2 and g_3 are all strong functions of the bias condition. g_0 is only important for DC analysis.

The nonlinear capacitance is normally associated with a voltage dependent capacitor such as varactor diode, where a reverse bias alters the small signal ca-

pacitance. It is usual to consider the nonlinear capacitor as a voltage dependent charge storage element as follows.

$$q(t) = c_0 + c_1 v(t) + c_2 v^2(t) + c_3 v^3(t) + ... \tag{2.2}$$

where $v(t)$ is the set of AC voltages across the capacitor, $q(t)$ is the charge stored in the capacitor, c_0 represents the stored static charge and c_1 is the incremental or small signal capacitance.

Differentiating Eq. 2.2 with respect to time gives the I-V relationship as follows.

$$i(t) = \frac{dq(t)}{dt} = \frac{dq(t)}{dv(t)}.\frac{dv(t)}{dt} = (c_1 + 2c_2 v(t) + 3c_3 v^2(t) + ...).\frac{dv(t)}{dt} \tag{2.3}$$

In order to describe the simplest possible model of a FET some assumptions should be made. These assume that the output conductance is zero and the gate source capacitance is purely linear. Therefore, the current flowing between the drain and the source (i_{ds}) due to the AC voltage across the gate source port can be expressed as follows.

$$i_{ds} = g_0 + g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ... \tag{2.4}$$

where g_0 is the DC current flowing due to the bias, and g_1 is the small signal transconductance.

This nonlinear description is identical to that of the 2 terminal nonlinear conductance explained previously, except that the control voltage and the output current exist at different terminals of the nonlinear element.

2.3.1.2 Fundamental Definitions

In this section we explain some basic definitions with respect to nonlinearity which will be discussed in due course. These include dBm, 1 dB compression point, harmonic distortion, intermodulation distortion, second and third order intercept points, distortion saturation, spectral regrowth, adjacent channel power ratio and AM/PM conversion.

dBm

The term dBm is frequently used for representing power measurements. 0 dBm is equivalent to 1 mW of power (P) into a 50 Ω load. Therefore, it can be shown that 0 dBm is equivalent to $\sqrt{P \times 50} = 223.6 mV_{pp}$ across a 50 Ω load.

1 dB Compression Point

In a system with a single sinusoid input, as the input amplitude is increased from a very low value the gain stays constant. As the input amplitude is increased further there will be a point at which the fundamental component of the wanted signal becomes 1 dB lower than that of a perfectly linear system. This point is referred to as the 1 dB gain compression point. The 1 dB gain compression point is usually used to specify the linearity of the RF port.

Harmonic and Intermodulation Distortion

When a sinusoid passes through a nonlinear network new frequency components are generated.

To show how new frequencies are generated in nonlinear circuits it is best to describe the I-V characteristics of the component via a power series and to assume a multi-tone excitation voltage. Consider the following expression

$$I = aV_s + bV_s^2 + cV_s^3 \tag{2.5}$$

where a, b and c are constant, real coefficients. Assuming that V_s is a two tone excitation of the following form.

$$V_s = v_s(t) = V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t) \tag{2.6}$$

By substituting Eq. 2.6 into Eq. 2.5 and carrying out some mathematical manipulation, we can obtain the three terms in Eq. 2.5 as follows.

$$i_a(t) = av_s(t) = aV_1\cos(\omega_1 t) + aV_2\cos(\omega_2 t) \tag{2.7}$$

$$\begin{aligned} i_b(t) &= bv_s^2(t) = \frac{1}{2}b\{V_1^2 + V_2^2 + V_1^2\cos(2\omega_1 t) + V_2^2\cos(2\omega_2 t) \\ &\quad +2V_1V_2[\cos((\omega_1+\omega_2)t) + \cos((\omega_1-\omega_2)t)]\} \end{aligned} \tag{2.8}$$

and

$$\begin{aligned} i_c(t) &= cv_s^3(t) = \frac{1}{2}c\{V_1^3\cos(3\omega_1 t) + V_2^3\cos(3\omega_2 t) \\ &\quad +3V_1^2V_2[\cos((2\omega_1+\omega_2)t) + \cos((2\omega_1-\omega_2)t] \\ &\quad +3V_1V_2^2[\cos((2\omega_2+\omega_1)t + \cos((2\omega_2-\omega_1)t)] \\ &\quad +3(V_1^3+2V_1V_2^2)\cos(\omega_1 t) + 3(V_2^3+2V_1^2V_2)\cos(\omega_2 t)\} \end{aligned} \tag{2.9}$$

The total current is the sum of the above currents which has a large number of new frequency components. These new frequency components are called distortion products. These distortion products are shown in Figure 2.3.

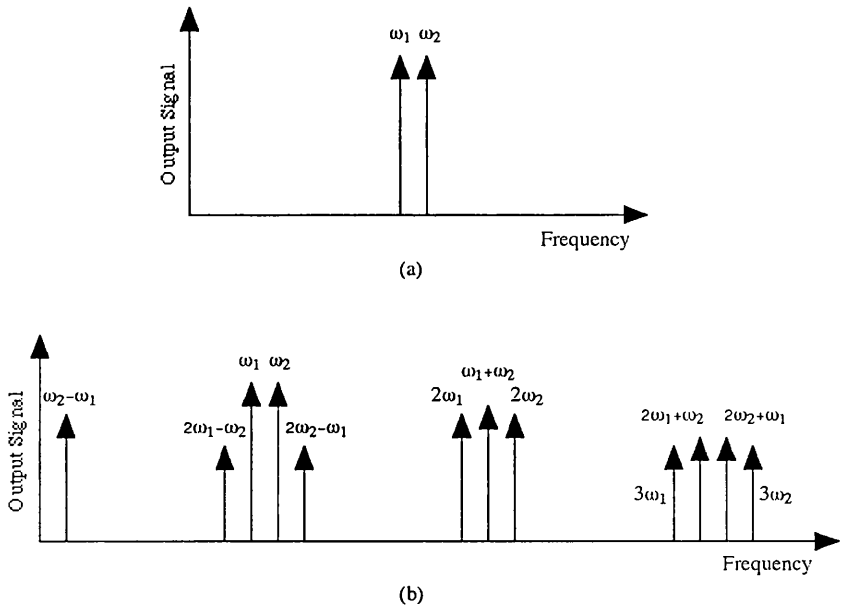


Figure 2.3: Harmonic and intermodulation distortion products. (a) Two tone excitation signals at the input and (b) two tone excitation signals plus harmonic and intermodulation distortion products at the output.

If a single tone is applied, the distortion products are integer multiples of the input frequency and they are referred to as harmonic distortion (e.g. $2\omega_1$). If multiple tones are applied to a nonlinear network, apart from the generation of the harmonics, other distortion components are generated that consist of a sum or difference of integer multiples of the applied tones (e.g. $2\omega_1$-ω_2). These are called the intermodulation distortion products.

Intercept Points

In the characterisation of nonlinear systems, such as low noise amplifiers, a point of interest is the second and third order intercept points. The intercept points are both applicable to harmonic and intermodulation distortion products. The point on a plot of output power versus input power, where a linear extrapolation to the fundamental component, intercepts the second tangent component is referred to as the second order intercept point and where it intercepts the third tangent component is called the third order intercept point. The intercept points are shown in Figure 2.4. These interceptions are due to the fact that in the small signal case, the rate of increase of power in the second order harmonic is two times (see Eq. 2.8) and the rate of increase of power in the third order harmonic is three times (see Eq. 2.9) the rate of that for the fundamental component provided the two input amplitudes have the same magnitude.

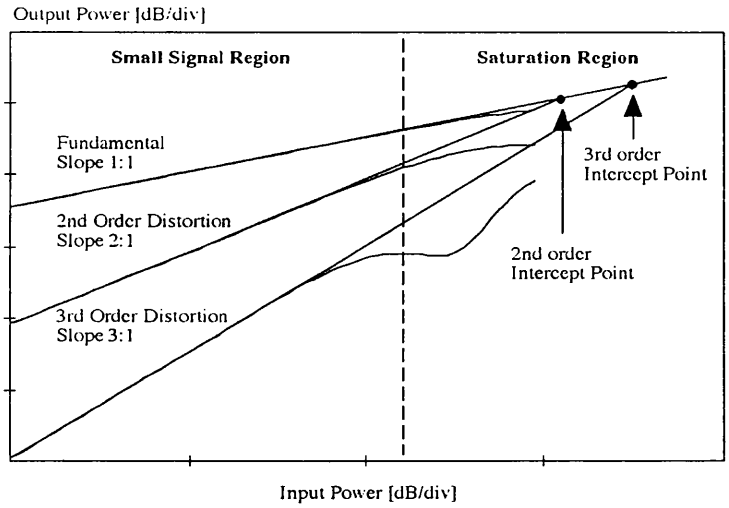


Figure 2.4: Intercept points.

Distortion Saturation

The amplitudes of distortion products change as the amplitude of the excitation signals are changed as shown in Figure 2.4. As mentioned previously, in the small signal case, the amplitude of the distortion products are related to the excitation amplitude by power law relationship defined by the order of the product (e.g. 3rd order has a power of 3). At larger signal levels the distortion products no longer obey these simple power laws and can rise sharply or even null (see Figure 2.4). This effect is referred to as distortion saturation and is due to the contribution of higher order nonlinear terms to lower order terms.

Spectral Regrowth and Adjacent Channel Power Ratio [3]

In both analogue and digital systems, in-band interference is mostly due to signal transmission from other base stations or units using the same frequency channel, and by other units using adjacent and next to adjacent channels. Therefore, the transmitted intermodulation levels in the adjacent and next to adjacent channels are to be limited in order not to cause interference to other units operating in the nearby channels. The adjacent channel interference levels increase by the generation of the out of band components in the nonlinear amplifier chain. This process of increasing adjacent channel interference with increasing transmitted power is called spectral regrowth. In order to characterise the interference produced in the adjacent channels a measure is employed which is called the adjacent channel power ratio (ACPR). This is the power in the main channel divided by the power in the lower plus upper adjacent channels (ACPR_{Lower} and ACPR_{Upper}, respectively).

AM/PM Conversion

In a power amplifier, the fundamental frequency can be affected by the distortion from higher order products (e.g. contribution from 3rd order nonlinearity to fundamental). These contributions from higher order products have an arbitrary phase relationship with respect to the input signal and their amplitude depends on the magnitude of the input power. This causes a phase modulation that varies with signal amplitude. This is referred to as AM/PM conversion.

2.3.2 Nonlinear Analysis Techniques

There are several ways of analysing a nonlinear circuit. The most common ones are the following.

Time Domain Techniques [4], [5]

This method is practical for low frequency analogue and digital designs. Circuit theory can be used to obtain the time domain differential equations that describe a nonlinear circuit. These equations can then be solved numerically. Time domain techniques are most practical for analysing circuits that include only lumped elements. They can also be used with a limited variety of distributed elements such as the ideal transmission lines. Lossy or dispersive transmission lines can not be easily modelled in the time domain. One of the problems with this method is that it can not handle frequency domain quantities, e.g. impedances. Other drawbacks include lengthy simulation times, considerable memory requirement and lengthy settling times. On a steady state response of a FET, the inclusion of settling time is due to the finite impulse response of the system and the need for appointing a dead period for the response (e.g. omission of a couple of cycles at the beginning of the response) in order to obtain a noise free response.

Harmonic Balance Analysis [6], [7], [8]

This is an interactive numerical method in which the network is split into linear and nonlinear subnetworks. The linear subnetwork contains only linear elements and the nonlinear subnetwork contains all of the nonlinear elements. The linear subnetwork is solved in the frequency domain and the nonlinear subnetwork is solved in the time domain. Solving the linear parts in the frequency domain has the advantage of being computationally fast and also it requires little memory. The discrete Fourier transform is employed to convert the resulting waveform from the time domain analysis into its frequency spectrum. The harmonic balance technique is used to match the harmonic amplitudes of current or voltage in the set of branches joining the linear and nonlinear subnetworks.

The harmonic balance technique is primarily applicable to strongly nonlinear

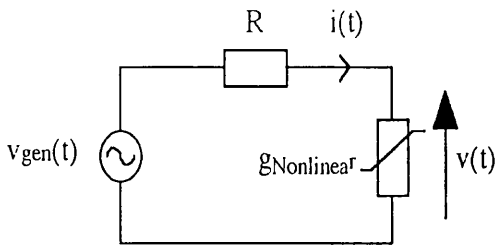


Figure 2.5: Circuit with a nonlinear conductance.

circuits that are excited by a single large-signal excitation source. These include circuits such as transistor power amplifiers, mixers, local oscillator circuits and frequency multipliers. This technique has a significant speed advantage over the time domain techniques but is slow compared to a Volterra based simulator.

Volterra Series Analysis [7], [9], [10]

This technique is only suitable for weakly nonlinear systems at low excitation levels. A popular approach to Volterra series analysis is called the method of nonlinear currents [7]. This technique enables the calculation of current components from voltage components of lower order. Then the voltage components of the same order are found from those currents, and enables the higher order currents to be determined. As an example, consider Figure 2.5 which is a simple nonlinear circuit consisting of a voltage source, $v_{gen}(t)$, a linear resistor, R, and a nonlinear conductance, $g_{Nonlinear}$. We have the following expression for the current flowing through the nonlinear conductance.

$$i(t) = g_1 v(t) + g_2 v^2(t) + g_3 v^3(t) + ... \tag{2.10}$$

where $i(t)$ and $v(t)$ represent the small-signal current and voltage in the nonlinear conductance, respectively. It should be noted that the voltage, $v(t)$, consists of all orders of mixing products. These are shown in the following expression.

$$v(t) = v_1(t) + v_2(t) + v_3(t) + ... \tag{2.11}$$

The circuit of Figure 2.5 can be redrawn as shown in Figure 2.6 by using the substitution theorem [7], which allows the nonlinear conductance to be replaced by a linear conductance and several current sources.

The linear conductance represents the linear part of Eq. 2.10, and each current source represents a nonlinear term in Eq. 2.10. By limiting the Eq. 2.10 to the third degree we can obtain the following relationships.

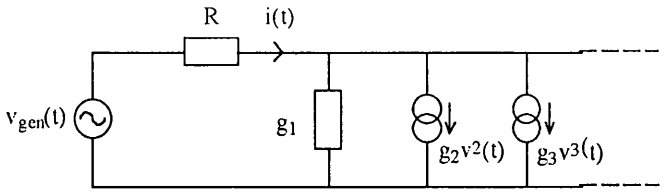


Figure 2.6: The circuit of Figure 2.5 in which the nonlinear conductance has been replaced by a linear conductance and a set of current sources.

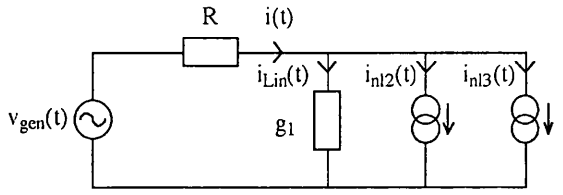


Figure 2.7: The circuit of Figure 2.6 in which each current source represents a single order of mixing products. Note that the circuit represents the mixing products only up to the 3rd degree.

$$v(t) = v_1(t) + v_2(t) + v_3(t) \tag{2.12}$$

$$v^2(t) = v_1^2(t) + 2v_1(t)v_2(t) \tag{2.13}$$

$$v^3(t) = v_1^3(t) \tag{2.14}$$

The $v_1^2(t)$ term on the right hand side of Eq. 2.13 can only generate second-order mixing products. The second term of Eq. 2.13, $2v_1(t)v_2(t)$, shows third-order products. For simplicity, the circuit of Figure 2.6 can be rearranged as shown in Figure 2.7, in order to have current sources which represent the same order of mixing frequency.

Therefor, we have the following relationships.

$$i(t) = i_{lin}(t) + i_2(t) + i_3(t) \tag{2.15}$$

where

$$i_{lin}(t) = g_1 v(t) = g_1[v_1(t) + v_2(t) + v_3(t)] \tag{2.16}$$

$$i_{nl2}(t) = g_2 v_1^2(t) \tag{2.17}$$

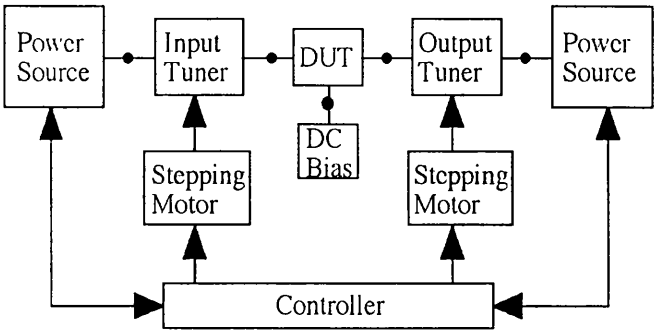


Figure 2.8: The block diagram of a typical load pull measurement set-up.

$$i_{nl3}(t) = 2g_2v_1(t)v_2(t) + g_3v_1^3(t) \tag{2.18}$$

The $i_{lin}(t)$ in Figure 2.7 represents the linear part of Eq. 2.10. The current sources $i_{nl2}(t)$ and $i_{nl3}(t)$ in Figure 2.7 represent all the second and third order current components of Eq. 2.10.

The expressions obtained for the linear and nonlinear terms using Volterra series analysis can be incorporated into various computer programs (e.g. "C") for high speed small-signal distortion simulation purposes.

Having discussed some of the definitions and analysis methods concerned with nonlinear circuits, we will next describe some of the most popular characterisation techniques used in nonlinear applications.

2.4 Nonlinearity Characterisation Techniques

Some of the most popular characterisation techniques are discussed below.

2.4.1 Load Pull Method

A large signal circuit such as a power amplifier can be characterised by plotting the contours of its load impedances that result in prescribed values of gain and output power on a Smith chart. This technique is referred to as the load pull method [11], [12]. The block diagram of a load pull measurement set-up is shown in Figure 2.8.

The contours are generated by connecting various complex loads to the amplifier and measuring the gain and the output power at each value of load impedance.

It should be noted that active load pull techniques also exist, in which a test signal is applied to the output of the device, and tuning effects are simulated by

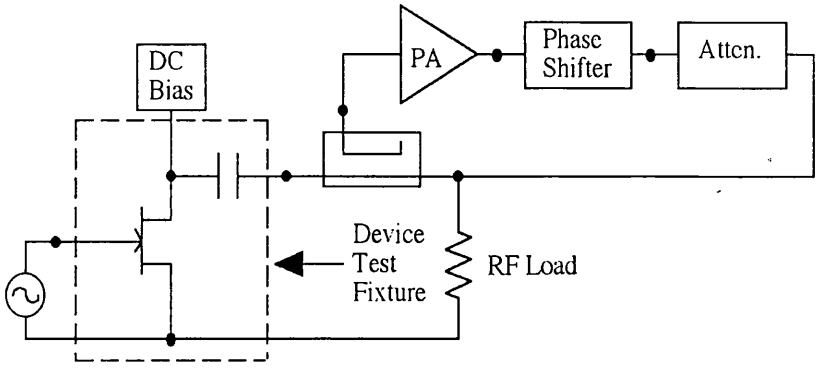


Figure 2.9: Active load pull measurement set-up.

varying the amplitude and phase of the applied signal. A typical implementation is shown in Figure 2.9.

Active tuners are more advantageous at higher frequencies where the design of the mechanical tuners become more difficult.

The load pull method has some difficulties associated with it which are namely as follow. Measuring the load impedances at the device terminals can be difficult. This method defines only the load impedance at the fundamental frequency. The load impedance at the harmonics can significantly affect circuit performance.

2.4.2 Measuring S-parameters

Another method for characterising a large signal nonlinear circuit is to measure a set of two-port parameters, usually S-parameters at a large signal excitation level [13]. This method is good for linear circuits but when it is applied to strongly nonlinear circuits it gives problems. These problems are caused due to the fact that the response of a nonlinear circuit changes with amplitude. For instance, a class AB amplifier with a sufficiently small input signal acts as a poor class A amplifier.

2.4.3 Pulsed I-V Measurement

The I-V nonlinearity of a short channel FET changes with frequency [14], [15]. Effects such as self heating and trapping at low frequencies (below 1MHz); which will be discussed in more detail in Section 2.5.8; lead to a different I-V nonlinear behaviour than that at high frequencies. This has led to the development of the pulsed I-V characterisation technique to measure the dynamic nonlinear I-V behaviour [16], [17], [18], [19]. A block diagram of the pulsed I-V measurement

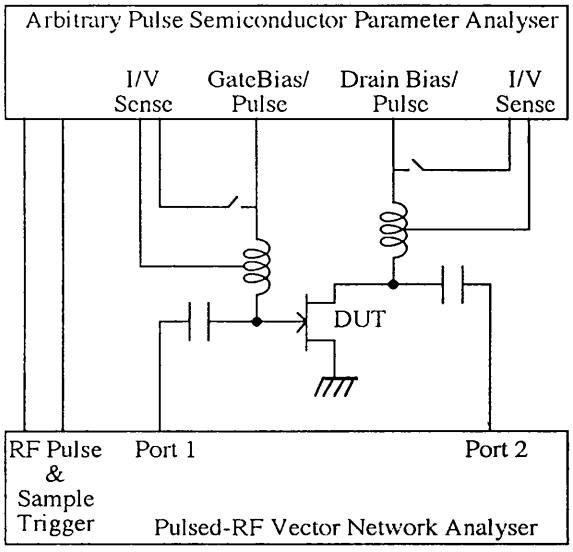


Figure 2.10: Schematic diagram of a typical pulsed I-V measurement set-up.

system is shown in Figure 2.10.

In this technique spot values of current over a grid of v_{gs} and v_{ds} points are obtained. The measurements are obtained during a pulse period that is shorter than the time constant associated with the device and, therefore, are a reliable representative of the high-frequency behaviour of the device. The pulse width is of great importance and it should be chosen sufficiently small (e.g. 0.5 μs) in order to ensure accurate measurement.

Pulsed I-V measurement overcomes a number of problems such as frequency dependent anomalies (self heating and trapping effects), rate dependence anomalies and history dependence anomalies. One of the major disadvantages is the high cost of a pulsed I-V measurement set-up.

2.4.4 Maas RF Harmonic Distortion Measurement Method

A technique for measuring the nonlinear derivatives of a FET (see Eq. 2.10) was proposed by Maas and Crosmun [20]. The block diagram of the modified version [21] of this technique which has improved sensitivity and accuracy, is shown in Figure 2.11. The filter is tuned to the harmonics and only the harmonic distortion products are measured. One of the advantages of this set-up is that it uses a diplexing filter to prevent the generation of harmonics in the amplifier or spectrum analyser which might interfere with the measurement. The attenuator is used to provide a good VSWR at the FET's gate. The low noise amplifier is used to improve the sensitivity of the spectrum analyser.

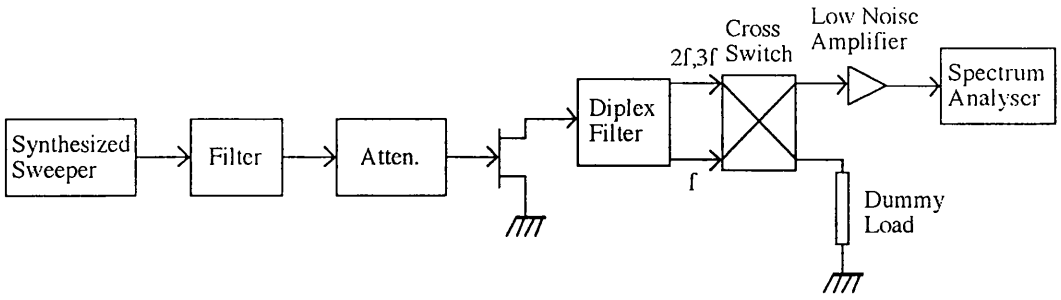


Figure 2.11: Maas RF harmonic distortion measurement set-up.

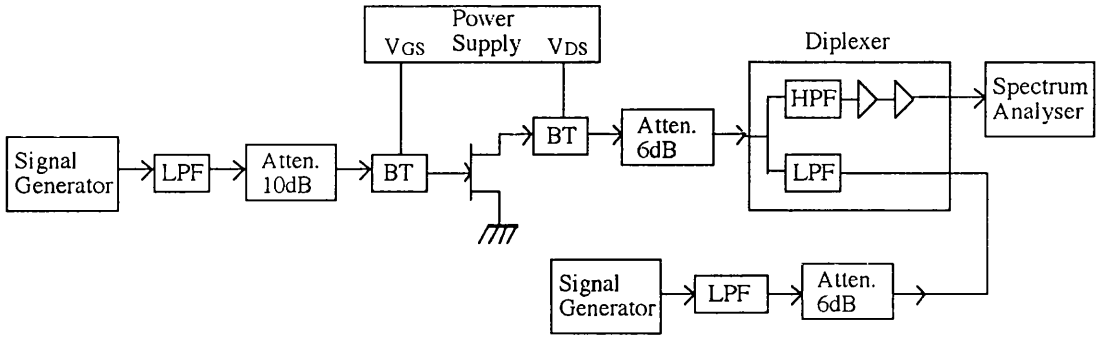


Figure 2.12: Pedro and Perez distortion measurement set-up.

2.4.5 Pedro and Perez Distortion Measurement Method

In this method [22] the excitation signals are injected at the gate and the drain terminals of the FET as shown in the test set-up shown in Figure 2.12.

In this measurement set-up the intermodulation distortion products are measured. The diplexer in Figure 2.12 consists of two elliptic filters, a low pass and a high pass connected in parallel. This provides good input match at all fundamental and harmonic output frequencies, when optimised. The attenuators are used for obtaining good VSWR over the entire band.

2.4.6 FET Resistance Measurement

In Figure 2.13 we show the small signal equivalent circuit of a field effect transistor. This equivalent circuit can be divided into two sections.

The intrinsic elements g_m, g_{ds}, C_{gs}, C_{gd} , C_{ds}, R_i and τ which are functions of the biasing conditions and the extrinsic elements R_g, R_s, R_d, L_g, L_s, L_d, C_{pg} and C_{pd} which are independent of the biasing conditions. FET source resistance, R_s, drain resistance, R_d, and channel resistance, R_{CH}, have a significant effect on the device performance such as frequency response, noise figure and nonlinear-

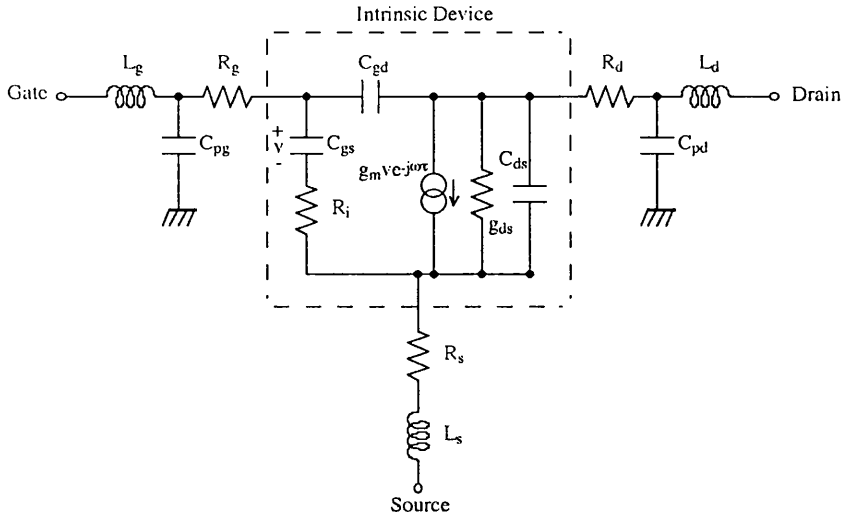


Figure 2.13: Small signal equivalent circuit of a field effect transistor.

ity. Therefore, it is important to characterise these resistances in order to obtain reliable CAD models for circuit design and also to calibrate physical device models for device optimisation. The characterisation techniques for obtaining source and drain resistance can be done either by DC measurement or by S -parameter measurement.

There have been many publications on this work. Fukui [23] uses the extrinsic drain source resistance of the cold FET (i.e. zero drain bias) with gate bias together with a physics based equation describing intrinsic channel resistance, R_{CH}, with gate bias to determine $R_s + R_d$.

Fukui, Goyal [24] and Zhu [25] apply gate current to a cold FET to separate the voltage drops across different combinations of R_s and R_d and the series gate resistance R_g from the voltage drop across the gate diode. They use a 3 measurement topology to differentiate between R_s, R_d and R_g. Goyal uses a simple diode model and Zhu uses a planar diode model. However, neither Goyal nor Zhu use the physical relationship of Fukui. Lee [26] injects current at the gate and uses the drain terminal as a probe to measure the voltage at the source side of the channel to determine R_s. This technique requires the calculation of a correction factor to eliminate contamination of the R_s from the channel resistance, R_{CH}.

Z-parameters derived from cold FET S-parameters are also used for determining R_s and R_d. Since $Z_{12} = Z_{21}$, only 3 unknowns can be found, whereas in practice 4 unknowns are present, R_s, R_d, R_g and R_{CH}. Diamand [27] overcomes this by using Grebene's physical based model of R_{CH} with gate bias to determine $R_s + R_d$. Anholt [28] further develops the work of Dambrine [29] and Lee, providing two

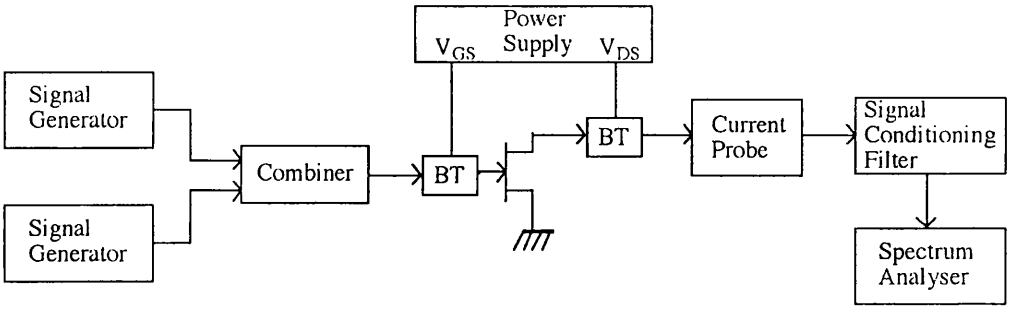


Figure 2.14: Block diagram of the TDFD measurement set-up.

equivalent circuits that depend on the gate current. He questions the relevance of the Grebene and Fukui model for ion implanted FETs. Also he explores the possibility of bias dependence of R_s and R_d neglected by many other authors.

Osgood [30] uses DC Z-parameters, and by using a combination of positive and negative drain biases, is able to steer the gate current either into the source or drain terminal and thus, determine R_s , R_d and R_g without having to determine R_{CH}.

Sommer [31] uses the feedback through R_s and R_g in y_{12} under positive drain bias to determine the ratio of R_s to R_g and is able to observe bias dependence.

The most convenient technique seem to be the one carried out by DC measurements but any of the above measurement techniques can be used for the determination of the R_s, R_d and R_{CH}.

2.4.7 TDFD Measurement

The total difference frequency distortion (TDFD) method [32], [33], [34], can be used to measure intermodulation distortion of wideband systems.

In this method shown in Figure 2.14 the excitation signals are both applied to the gate terminal of the device under test and their frequencies are chosen to be in, approximately, a ratio of 2:3. This results in a pair of 2nd and 3rd order difference products which have a maximum separation from the excitation signals. This gives rise to enhanced dynamic range in the distortion measurement.

In this method it is important to remove the residual level of intermodulation distortion generated by the interaction of the signal generators for accurate distortion measurements. This can be achieved by using a combination of wideband isolating combiners and notch filters.

Having discussed some of the nonlinearity characterisation techniques we will next present a description of some of the popular HEMT and MESFET models.

2.5 MESFET and HEMT Models

Some nonlinear models for MESFETs and HEMTs will be discussed in the following sections. Then, we will discuss frequency dispersion effects seen in MESFETs and HEMTs and comment on the effectiveness of these models in describing them.

2.5.1 The Schichmann-Hodges Model

In this model [35], [36] the drain current equations are defined as

for $V_{GS} - V_{TO} < 0$

$$I_D = 0 \tag{2.19}$$

for $0 < V_{GS} - V_{TO} < V_{DS}$

$$I_D = \beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS}) \tag{2.20}$$

and for $0 < V_{DS} < V_{GS} - V_{TO}$

$$I_D = \beta V_{DS}\{2(V_{GS} - V_{TO}) - V_{DS}\}(1 + \lambda V_{DS}) \tag{2.21}$$

where V_{TO} is the pinch-off voltage and λ defines the DC value of R_{ds} . The square-law Schichmann-Hodges MOSFET model is the most basic of the models. This model is included in SPICE and it includes charge storage, channel-length modulation and pinch-off saturation effects which occur in long channel FETs. The Schichmann-Hodges MOSFET model incorporates two diodes to model gate-drain and gate-source junctions. Independent capacitances obeying an inverse half-power law of junction potential are used to model charge storage associated with each junction. This capacitance model fails to predict a reduction in capacitance when pinch-off occurs. The short channel GaAs MESFETs exhibit many more characteristics such as frequency dispersion, soft pinch-off and non-square law effects. In a model based on the square law the device never pinches-off whereas in reality devices do pinch-off. The conditions stated for the Schichmann-Hodges model are to ensure the device pinches-off but this gives discontinuity problems. Also, the shape of the I-V curves of a device away from pinch-off does not exactly follow a square law. The frequency dependent distortion includes impact ionisation, self heating (i.e. which results in a change of mobility) and trapping effects which cause bias dependant and frequency dependant pinch-off modulation. These must be considered for accurate circuit simulations.

2.5.2 The Curtice Quadratic Function MESFET Model

One of the most important characteristic which the short channel GaAs MESFETs exhibit is velocity saturation. In GaAs MESFETs an early drain current saturation is caused by electron velocity limiting. The saturation knee actually occurs at a lower drain potential than predicted by the Schichmann-Hodges model. This effect was modelled by Curtice with a hyperbolic tangent function [37]. This model assumes an analytical function as follows.

$$I_{ds} = \beta(V_{gs} + |V_P|)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{2.22}$$

where β is a transconductance scaling factor, V_p is pinch-off voltage, α adjusts the knee of I_{ds} versus V_{ds} and λ has the same function as the one in the Schichmann-Hodges model. The advantage of the quadratic model is its simplicity, which gives short computations times. A disadvantage associated with this model is that g_m nonlinearity can generate only second order harmonics. Therefore, there are no 3rd order harmonic and intermodulation distortion products. This model is also unable to fit the soft pinch-off behaviour of transistors. Also it has been shown that a square-law model approximation can lead to errors in relating the small-signal and large signal models [38].

2.5.3 Materka Model

The Materka model [39], [40] assumes an analytical function of the following form

$$I_{ds} = (1 + \frac{V_{gs}}{V_p'})^2 \tanh[\alpha \frac{V_{ds}}{(V_{gs} + V_p')}] \tag{2.23}$$

where $V_p' = |V_p| + \gamma V_{ds}$.

The coefficient γ gives adjustment of pinch-off voltage V_p' as a function of V_{ds} from a nominal $|V_p|$.

2.5.4 Statz Model

The Curtice quadratic model was extended by Statz et al. [41] to overcome the problems associated with a square-law approximation model. This was done by adding a doping tail extending parameter, b $[V^{-1}]$, to allow the deviation from the square law. This model uses a cubic approximation to the hyperbolic tangent function. It also offers an improved charge model representation of C_{gs} and C_{gd} as functions of both V_{gs} and V_{ds}. This is shown in the following expressions.

$$I_{ds} = [\frac{\beta(V_{gs} - V_{to})^2}{1 + b(V_{gs} - V_{to})}](1 + \lambda V_{ds})\{1 - (1 - \frac{\alpha}{3}V_{ds})^3\}; \text{for } V_{ds} \leq \frac{3}{\alpha} \tag{2.24}$$

and

$$I_{ds} = \frac{\beta(V_{gs} - V_{to})^2}{1 + b(V_{gs} - V_{to})}(1 + \lambda V_{ds}); \text{for } V_{ds} > \frac{3}{\alpha} \tag{2.25}$$

where β controls the change in pinch-off voltage.

The Statz model gives good fitting of the g_m nonlinearities near pinch-off. This feature makes the Statz model a good choice for simulating MESFET mixers, Class B and Class AB amplifiers.

The Statz et al. model uses the total charge under the gate rather than two independent quantities as in the case of Schichmann-Hodges model. The charge is shared symmetrically between source and drain so that device terminal reversal can be modelled. It also includes a reduction in gate-source capacitance at pinch-off.

A disadvantage of the Statz model is that it does not allow the freedom to adjust the fit for the third derivative. This freedom is available in Curtice Cubic model.

2.5.5 Curtice Cubic Model

The problems associated with the square-law based models were also acknowledged by Curtice and Ettenberg [42]. Therefore, they replaced the square law with a cubic polynomial with four fitting parameters. This model uses a third order polynomial and is often referred to as the Curtice cubic model. This model assumes the following.

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3)\tanh(\alpha V_{ds}) \tag{2.26}$$

where $V_1 = V_{gs}[1 + \beta(V_{ds0} - V_{ds})]$.

where β controls the change in pinch-off voltage with V_{ds}, and V_{ds0} is the drain-source voltage at which the A_i coefficients are evaluated. The cubic model is more capable of accurate simulation of 3rd order harmonic and intermodulation distortion in class A operation than the other popular models. The major disadvantage of the Curtice cubic model is that it never pinches off.

2.5.6 TOM Model

The TOM model [43] assumes an analytical function of the following form

$$\begin{aligned} I_{ds} &= \frac{I_{ds0}}{1 + \delta V_{ds} I_{ds0}} \\ I_{ds0} &= \beta\,(V_{gs} + \gamma(f)V_{ds} - V_{to})_g^Q\, K \tanh(\alpha V_{ds}) \end{aligned} \tag{2.27}$$

Some of the features of the TOM model are easy control for fitting g_m as a function of V_{gs}, an electrostatic feedback modulation (i.e. that is a pinch-off voltage whose magnitude increases with the increasing V_{ds}) and a simple way of modelling the dependence of R_{ds} on V_{gs}, V_{ds} and channel temperature.

The TOM model also includes the effect of drain feedback together with a reduction in drain conductance due to junction heating using the parameter δ.

2.5.7 Parker Skellern MESFET Model

The Parker Skellern (P-S) model is the most comprehensive empirical MESFET model available for circuit simulation [44], [45], [46], [47]. The P-S model can be considered as a major extension of the McCammant et al. model (TOM) [43]. In the TOM model the electrostatic feedback was expressed in terms of V_{ds}. The P-S model has an extended version of the electrostatic effect and it is expressed in terms of V_{gs} and V_{gd}.

$$\begin{aligned} V_{gst} &= V_{gs} - V_{to} \\ &\quad - \left(\gamma_{lf} + \gamma_{lf1} V_{gs(dc)} + \gamma_{lf2} V_{gd(dc)}\right) V_{gd(dc)} \\ &\quad - \left(\gamma_{hf} + \gamma_{hf1} V_{gs(dc)} + \gamma_{hf2} V_{gd(dc)}\right) V_{gd(ac)} \\ &\quad - \left(\eta_{hf} + \eta_{hf1} V_{gd(dc)} + \eta_{hf2} V_{gs(dc)}\right) V_{gs(ac)} \end{aligned} \tag{2.28}$$

The electrostatic effect representation at DC and frequencies higher than 10 MHz require different parameters. These are shown by V_{gs}(DC) and V_{gs}(AC). The frequency dependent distortion includes impact ionisation, self heating and trapping effects which cause bias dependant and frequency dependant pinch-off modulation. It is the frequency dependant distortion effects of a device which causes its DC and RF characteristics to be different from each other. Apart from the P-S model which takes into account the frequency dependant distortion, the Angelov model [48] also includes this effect. The TOM model includes a partial frequency dependant distortion effect as a nonlinear resistor in parallel with a current source (see Section 2.5.6) .

In the P-S model in order to get the soft pinch-off effect, V_{gt} is transformed by the following expression

$$V_{gt} = V_{st}\left(1 + m_{vst} V_{dst}\right) \ln\left[\exp\left(\frac{V_{gst}}{V_{st}\left(1 + m_{vst} V_{dst}\right)}\right) + 1\right] \tag{2.29}$$

The V_{st} term in the above equation controls the softness of pinch-off. The above expression tends to zero when $V_{gst} < 0$ and tends to V_{gst} when $V_{gst} > 0$. The sharpness of this transition is controlled by V_{st}. This continuous transformation

between the two regions results in convergence during simulation. The result of this soft pinch-off is a zero crossing in the 3rd derivative of the drain current which is always observed in real devices and not predicted by models which do not implement soft pinch-off.

For the prediction of the behaviour of MESFETs in the saturated region, the P-S model uses the same power law as in the TOM model

$$I_{ds0} = \beta V_{gt}^{Q} - (V_{gt} - V_{dt})^{Q} \tag{2.30}$$

The self heating effect of the channel and the resulting electron mobility reduction is modelled by an effective reduction in β with power dissipation.

In the P-S model the triode region is described by a separate arbitrary power law. This is different from the power law used in the TOM model (TOM model uses the same power law for the saturation and triode regions).

$$V_{dp} = \frac{P}{Q}\left(\frac{V_{gt}}{\phi_b - V_{to}}\right)^{P-Q} V_{ds} \tag{2.31}$$

The following equations handle the transition between the triode and the saturation regions.

$$V_{sat} = \frac{V_{gt}(M_\xi V_{gt} + \xi(\phi_b - V_{to}))}{(M_\xi + 1)V_{gt} + \xi(\phi_b - V_{to})} \tag{2.32}$$

and

$$\begin{aligned} V_{dt} &= \frac{1}{2}\sqrt{\left(V_{dp}\sqrt{1+z} + V_{sat}\right)^2 + zV_{sat}^2} \\ &\quad -\frac{1}{2}\sqrt{\left(V_{dp}\sqrt{1+z} - V_{sat}\right)^2 + zV_{sat}^2} \end{aligned} \tag{2.33}$$

The location of the transition between the triode and saturated region with respect to V_{ds} as V_{gs} is varied is controlled by Eq. 2.32. The positions are controlled by ξ and M_ξ offers a fine tune to the V_{gs} dependence. The built-in potential of the Schottky contact is represented by ϕ_b. Eq. 2.33 controls the sharpness of the transition. Lower z values result in more abrupt transition between triode and saturated region. Eq. 2.33 presents a smooth transition between V_{dp} and V_{sat}, with V_{dt} being equal to the smaller of the two variables. This smooth transition guarantees convergence in time domain simulations.

Some of the overall features of the DC part of the Parker Skellern model are independent triode power law, knee sharpness control, LF self heating, control of knee locus, bias dependent LF electrostatic feedback and bias dependent soft pinch-off with adjustable softness factor.

The Parker Skellern model has an excellent description of frequency dispersion effects, which have a substantial effect on the RF behaviour of short channel MESFETs and InGaAs based HEMTs.

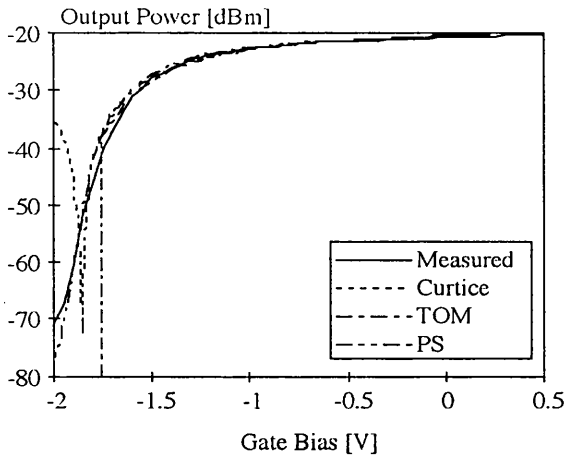
The P-S model can also be used for the modelling of HEMTs. This is possible by the addition of terms to implement g_m compression for increase in V_{gs} [49].

The P-S model has been implemented in several simulators such as SPICE3f4 (UC Berkeley) and UCL-SPICE (HEMT compression).

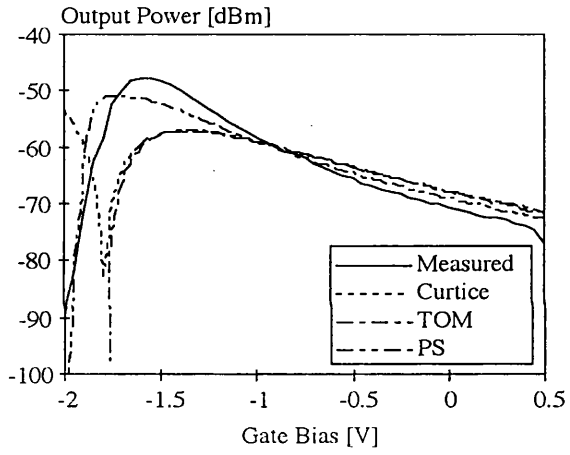
In Figure 2.15 we show a comparison of the prediction of distortion of a common-source MGF1400 GaAs MESFET using the P-S model and other standard models with measured results as the gate bias is varied. It can be seen from Figure 2.15(c) that although the P-S model does not predict the position of the 3rd order distortion minimum accurately, it does predict the general feature including the minimum and is much more accurate than any other model. Therefore, for the simulations which will follow in this thesis extensive use will be made of the Parker Skellern model. One of the most popular ways of obtaining a P-S model is as follows. The values for R_S and R_D (see Section 2.4.6) should be obtained. Then, DC fits for the triode and saturated regions should be carried out. After that RF g_{ds} and RF g_m fits to the S-parameter equivalent circuits should be performed. These can alternatively be obtained by pulsed I-V measurement (see Section 2.4.3). C_{gs} and C_{gd} should also be fitted to the S-parameter equivalent circuits. Following these procedures, the bias dependant small signal P-S model can be obtained.

2.5.8 Frequency Dispersion in MESFETs and HEMTs

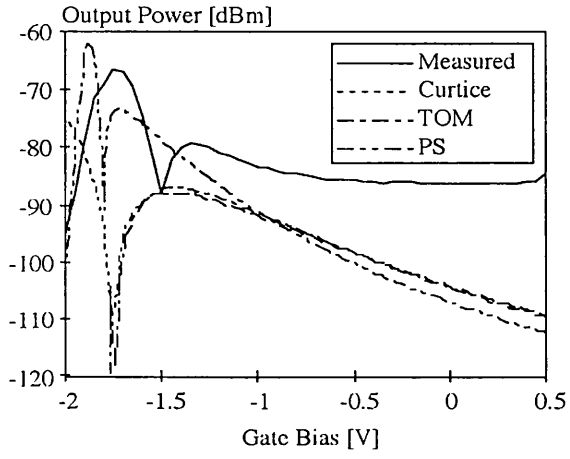
Frequency dispersion effects are better known as discrepancies between static output conductance of a device at DC and dynamic output conductance at RF frequencies [50]. The origin of frequency dispersion in the small signal behaviour has been considered to be a combination of self heating and trapping effects [15]. In a large signal scenario it is necessary to use pulsed I-V measurements for frequency dispersion interpretation [14]. This has led to the discovery of a large signal dispersion effect in pseudomorphic HEMTs [51]. In [52] the authors use a base model to explore the changes with bias that occur in the pulsed I-V behaviour of GaAs MESFETs and AlGaAs/InGaAs/GaAs HEMTs and compare this behaviour with the DC behaviour. The authors in [52] have identified changes in maximum current and dynamic output conductance, and for the first time, changes in knee voltage. Other well known frequency dispersion effects such as self heating and pinch off modulation have also been observed [52]. In the following we will give brief descriptions of three main possible mechanisms which cause frequency dis-



(a)



(b)



(c)

Figure 2.15: Comparison of the prediction of distortion by various models; (a) Fundamental, (b) 2nd order distortion and (c) 3rd order distortion.

persion in short channel MESFETs and HEMTs. These are self heating, trapping effects and impact ionisation.

Self Heating

At low device power dissipation the properties of the FETs are determined by the ambient temperature. Increase of the power dissipation results in a channel temperature which is above ambient temperature. Since electron mobility in GaAs and Silicon fall with temperature [53], there will be a drop in transconductance, and as a result, a drop in output conductance. Due to the thermal complexity of the thermal equivalent circuit, there may be several thermal time constants. The most important one is associated with the channel region and is around 10 μs.

Trapping Effects

The presence of donor atoms in the device channel cause a slight disruption in the crystal structure. These defects result in isolated energy states between the conduction and valance bands. The capture and release process has a time constant of around 100 μs. The occupancy or vacancy of a trap site affects the way the depletion region changes shape as the gate and drain bias changes. If the gate and drain bias change slowly, carriers can be trapped or released from the defects. On the other hand, if the change is fast, there is not enough time for capture and release. Since the way the depletion region changes shape is now frequency dependent, the transconductance and output conductance will also vary.

Impact Ionisation

Short channel devices have large gate drain voltages. This leads to high electric field strengths in certain regions. If the field strength is high enough, impact ionisation can occur. This is where electrons collide with the atoms in the channel dislodging further electrons and creating holes. This process causes the transconductance and output conductance to vary.

None of the models discussed above is fully capable of accounting for all the frequency dispersion effects mentioned. These dispersion effects have important implications for FET models. Failure to correctly model these effects could lead to errors not only in simulating small signal performance of an amplifier, but also its large signal performance including 1 dB compression point, maximum output power and optimum load resistance for a power amplifier. Therefore, in the design of FETs effort should be made to minimise these effects as much as possible.

2.6 Summary

In this chapter we have presented the concept of linear and nonlinear circuits. We have also presented some of the basic definitions which will be used extensively throughout this thesis. These included 1dB compression point, 2nd and 3rd order intercept points, harmonic and intermodulation distortion, spectral regrowth, adjacent channel power ratio and AM/PM conversion. Then, we presented some of the most popular nonlinear analysis techniques together with their advantages and disadvantages. These techniques included time domain and harmonic balance techniques. The Volterra analysis technique suitable for weakly nonlinear circuits was also discussed in some detail.

Various nonlinear characterisation methods were discussed. These include load pull method, S- parameter measurement, pulsed I-V measurement, Maas RF harmonic distortion measurement, Pedro and Perez distortion measurement, FET resistance measurement and TDFD measurement. Due to good dynamic range achievable in TDFD method and ease of design of scrubbing filters, the TDFD method will be used in the characterisation and distortion measurements which will follow in this thesis .

Various nonlinear FET models were reviewed. These included the Schichmann-Hodges model, the Curtice quadratic model, the Materka model, the Statz model, the Curtice cubic model, the TOM model and the Parker Skellern model. Most models use a hyperbolic tangent function to describe the triode region except the Parker Skellern model which uses an independent power law to handle this region. Most of the above models use power laws to describe the saturated region except Curtice cubic which uses a cubic polynomial. The knee region is the region between the saturated and the triode region. In a MESFET this region has the highest nonlinearity. All the models have difficulties describing this region. FETs have a soft turn off characteristic which is generally referred to as sub-threshold conduction. This is a region of low V_{gs} and low conductance. The Parker Skellern model has a description of this region and this model will be used extensively throughout this work. Some of the frequency dispersion effects seen in MESFETs and HEMTs were also discussed. These effects have important implications on the performance of FETs and, therefor, in designing circuits they should be accounted for as much as possible.

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Chapter 3

Review of Linear and Nonlinear Circuit Design

3.1 General

In this chapter we will look at some general requirements for linear and nonlinear circuits which arise in practical systems. We will examine the structure of a common-source FET amplifier paying attention to its distortion generation mechanism and some of the factors influencing its distortion characteristics and then, the distributed amplifier will be discussed. The derivative superposition technique based on common-source amplifiers as a mean of linearisation will be discussed and a derivative superposition amplifier using high-pass transmission lines will be described and some measured results will be presented. A comparison of linearisation techniques for small and medium signal applications and nonlinear applications will be presented and some of the most frequently used linearisation techniques for power amplifiers will be discussed.

3.2 Survey of Requirements

3.2.1 Linear Amplifiers

There are various kinds of linear amplifiers which have different features depending upon the requirements. The most common ones are the low noise small signal amplifier and the power amplifier. These amplifiers are used in practically all communication systems. In Figure 3.1 we show a block diagram of a typical digital communication system indicating the positions of low noise and power amplifiers. In the following we will give a brief discussion of each type of amplifiers.

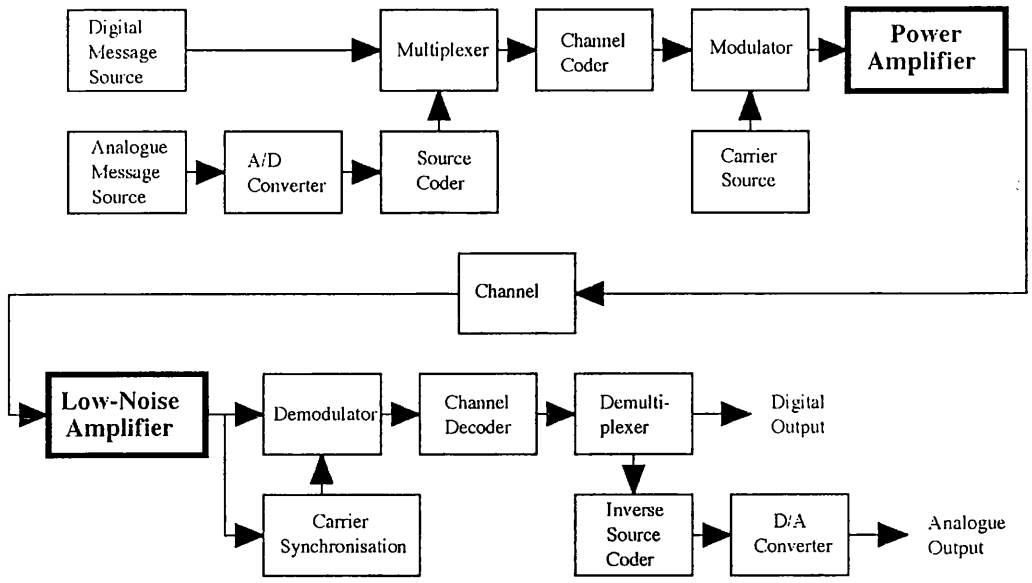

Figure 3.1: Block diagram of a typical digital communication system.

3.2.1.1 Small Signal Amplifiers

In the case of a small signal amplifier, an important issue is the noise figure. In order to achieve the desired noise performance, the input port is usually deliberately mismatched, in order to cause a higher voltage to be developed across the gate terminal due to its high impedance and hence, obtain a better noise performance. In the design of low noise amplifiers it is common to use the idea of constant noise and gain circles on a Smith chart. For a desired gain performance, the minimum noise figure point on the required gain circle is selected. The output port is then conjugately matched. Changing the load impedance will move the gain circles and also the stability criteria will be changed as a result. To overcome this problem additional reactive components can be used to move the constant noise circles on the Smith chart in order to obtain a better noise figure for a desired gain [1]. S and Y parameters together with design equations [2] are used in the design of small signal amplifiers.

3.2.1.2 Power Amplifiers

When a transistor is used with large signals, the S and Y parameters can no longer be valid as linear models are not capable of describing the terminal behaviour of the transistors which varies with power level [1], [2]. Hence, in a power amplifier emphasis is given more to the maximum ratings of the device and choosing a load line. These ratings include the maximum power dissipation and gate drain

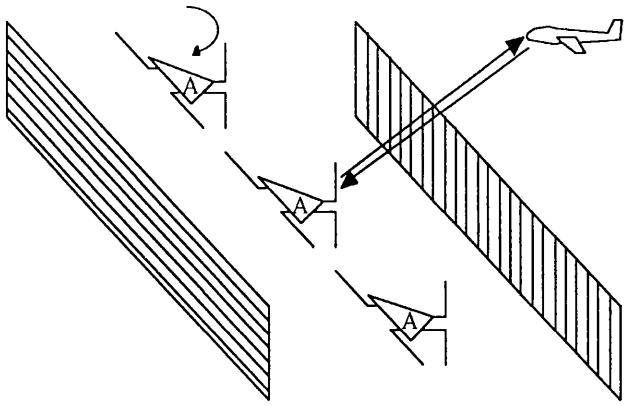

Figure 3.2: Block diagram of the complete quasi-optical tracking system.

breakdown of the device. In the power amplifier case special devices are used which have good heat sinking properties and have a better resilience against gate drain breakdown.

3.2.2 Amplifiers with Prescribed Nonlinearity

Amplifiers which have a linear gain component together with a controlled nonlinear component are required in various situations. A case of requirement for an amplifier with prescribed nonlinearity occurs in the quasi-optical tracking system [3]. A block diagram of the complete system is shown in Figure 3.2. The system consists of a linear array of transceivers between two polarising mirrors of different polarity. Each transceiver cell consists of a quarter wave dipole at both the input and the output. The input and output antennas are arranged orthogonally in order to inhibit cross coupling between the output and input of the amplifiers.

The objective is to rotate the transceiver array so that oscillation commences. This provides self pumping operation. A reflector is introduced and this leads to the generation of a conjugate beam that illuminates the reflector. A precisely controlled component of 3rd order nonlinearity of the amplifiers in each transceiver can be used to generate this conjugate beam. This system will be discussed in detail in Chapter 6 of this thesis.

3.2.3 Nonlinear Circuit Requirements

Frequency multipliers [4], in the past, were used to generate high levels of microwave RF power. Nowadays, due to solid-state power amplification at microwave frequency they are used less frequently. Today, frequency multipliers are usually

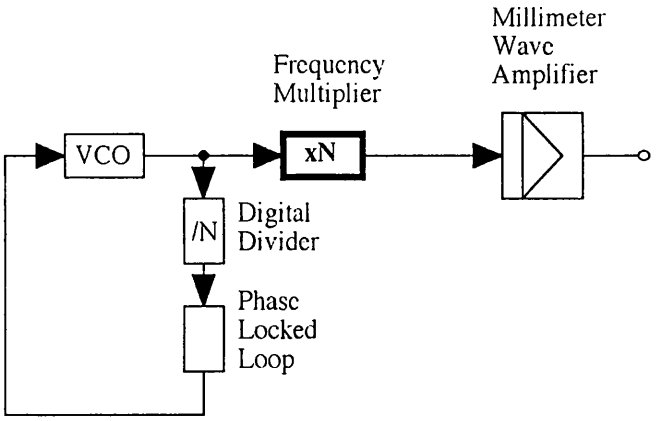

Figure 3.3: Block diagram of a millimetre wave signal source indicating the usage of frequency multipliers.

used for extreme frequency (e.g. THz) applications. For instance in mixers if the system level clock frequency is low, frequency multipliers can be used to boost the frequency. In Figure 3.3 we show a block diagram of a millimetre wave signal source indicating the occurrence of a frequency multiplier.

Diode circuits used for frequency multiplication can be based on the conductive or reactive effect. The reactive multipliers make use of the nonlinear capacitance characteristic of the diode. For harmonic generation at microwave frequencies diode circuits that use varactors or step recovery diodes (SRDs) are usually used. For the multiplication of microwave signals, for low harmonics, varactors are used and for high harmonic purposes SRDs are used. The reactive multipliers are narrowband. Diodes, such as Schottky barrier diodes, are usually used for low order frequency multiplication purposes. Although resistive multipliers are less efficient than reactive counterparts, they have advantages such as being broadband, easier to develop and are less sensitive to mistuning.

FET frequency multipliers have considerable advantages over diode frequency multipliers. These include conversion gain greater than unity, broader bandwidth, low DC power consumption and low heat dissipation.

The two most common types of frequency multipliers are the frequency doublers and frequency triplers. If the input signal is ω_1 the outputs produced will be $2\omega_1$ or $3\omega_1$ for a frequency doubler and a frequency tripler, respectively.

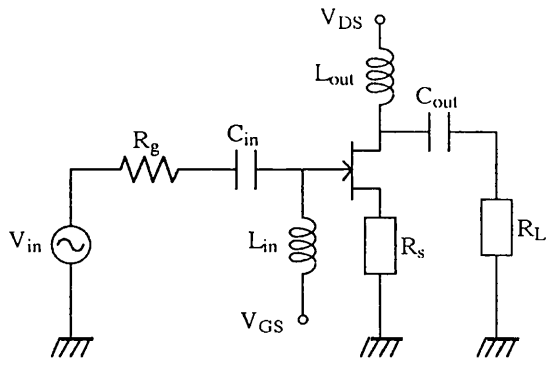

Figure 3.4: Schematic diagram of a common source amplifier.

3.3 The Common-Source Amplifier

The common-source FET amplifier is a very important circuit since it provides the basic building block for many linear and nonlinear RF circuits. In linear applications the 2nd order nonlinearity is generally higher than 3rd order nonlinearity but the second order nonlinearity can be reduced by using filtering strategies and balanced structures since they are usually out of band. Some nonlinear applications of the common-source FET amplifier depend on its 2nd order nonlinearity (e.g. frequency doublers). Below we discuss the basic architecture of a common-source FET amplifier and some of the factors which influence its distortion behaviour.

3.3.1 Basic Circuit Configuration

In Figure 3.4 we show the common-source FET amplifier configuration. The source resistance, R_s, represents the FET source parasitic contact resistance. The gate resistance, R_g, represents the combination of the generator resistance and the gate metalisation resistance.

3.3.2 Distortion Generation Mechanism

In order to understand the distortion mechanism in a common-source amplifier we reproduce the analysis of [5]. Consider the 2-D Maclauren series description of a FET which is given by the following expression.

$$\begin{aligned} i_d &= g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + g_{ds1} v_{ds} + g_{ds2} v_{ds}^2 + g_{ds3} v_{ds}^3 \\ &\quad + m_{11} v_{ds} v_{gs} + m_{12} v_{ds} v_{gs}^2 + m_{21} v_{ds}^2 v_{gs} \end{aligned} \tag{3.1}$$

where i_d is the drain current, the g_1, g_2 and g_3 terms represent transconductance, the g_{ds1}, g_{ds2} and g_{ds3} terms represent output conductance and the m_{11},

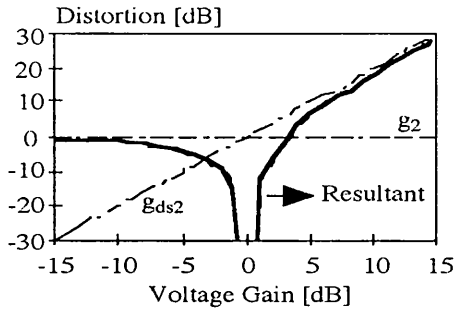

Figure 3.5: Input referred distortion versus arbitrary voltage gain with two dominant terms.

m_{12} and m_{21} terms represent the cross coupling terms. The terms in the above series will vary linearly, on a log scale, with voltage gain (v_{ds}/v_{gs}), which in turn varies with load resistance. The gradients will depend on the power of v_{ds} in each term. Distortion is generated by the combination of these terms. Let us now give examples of the generation of 2nd and 3rd order distortions.

2nd Order Distortion Generation

The distortion behaviour of a FET is critically a function of the magnitude and sign of the device parameters and of voltage gain [6]. There are three terms in Eq. 3.1 which give rise to 2nd order distortion. These terms are $g_2 v_{gs}^2$, $g_{ds2} v_{ds}^2$ and $m_{11} v_{ds} v_{gs}$. As an example, consider the g_2 and g_{ds2} terms. If the g_2 and g_{ds2} terms have the same sign (i.e. in phase), no distortion null is produced. On the other hand if the two terms have opposite sign (i.e. anti phase), a distortion null is possible provided the voltage gain is such that the two terms have equal and opposite magnitudes. This is shown in Figure 3.5.

3rd Order Distortion Generation

Considering Eq. 3.1 the most significant terms which contribute to 3rd order distortion are g_3, m_{21} and m_{12}. The g_3 and m_{21} terms usually have the same sign, so no null is observed. Now if we add the m_{12} term, which has a sign opposite to that of the resultant of g_3 and m_{21} terms, we get different kinds of nulls depending on the relative position of m_{12} term to the resultant. Graphically, the two in phase terms, g_3 and m_{21}, form a meniscus to which the out of phase term, m_{12}, forms a tangent. When the tangent is below the meniscus, the cancellation is incomplete and a shallow null forms. This null deepens as the tangent approaches the meniscus. When the tangent touches the meniscus a wide deep null is formed. If the tangent cuts the meniscus in two places, two narrow deep nulls are produced. These three scenarios are shown in Figure 3.6(a), (b) and (c).

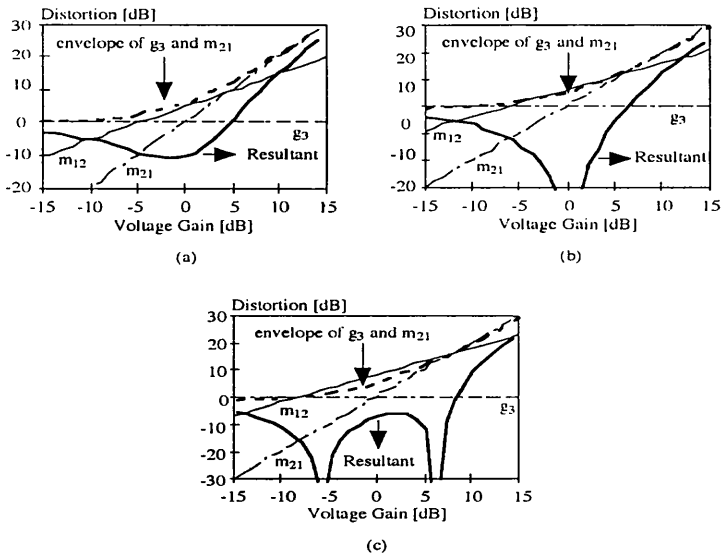

Figure 3.6: Input referred distortion versus arbitrary voltage gain with three dominant terms, (a) m_{12} close to the resultant, (b) m_{12} touching the resultant and (c) m_{12} crossing the resultant.

The resultant distortion behaviour is very sensitive to the relative magnitudes of the coefficients. Other situations are possible and can be considered as combinations of these basic forms.

3.3.3 Matching Networks

In order to obtain the maximum possible power transfer, matching networks must be used to match the input and output ports of an amplifier [7]. In certain circumstances the ports can be deliberately mismatched. For instance in the case of a low noise amplifier in order to obtain a better noise performance the input port is deliberately mismatched.

3.3.4 Effect of Bias and Load on Distortion

There are various factors which influence the distortion behaviour of a FET. These will be discussed in detail in the context of a new study in Chapter 5. Here, we will briefly describe only two such factors. These are the bias and load conditions. It has been shown [6] that the position of the minimum 3rd order intermodulation distortion when plotted against DC gate bias, can be altered by changing the biasing conditions and load resistance. The authors in [6] have shown that it is possible to simultaneously minimise the 2nd and 3rd order distortion products and

still have substantial gain.

3.3.5 Effect of Filtering for Nonlinear Applications

In some cases it is possible to reduce distortion by filtering strategies. However, this has very limited usage. Very high Q factor filters are required since a significant portion of the 3rd order intermodulation distortion is in band. It is expensive and often impractical to realise a high Q filter in the microwave frequency range. On the other hand, filtering the 2nd order distortion can contribute to better 3rd order distortion behaviour in some cases [8].

3.4 Extensions to the Common-Source Amplifier

3.4.1 The Distributed Amplifier

The circuit diagram of a distributed amplifier [9] , [10] is presented in Figure 3.7. In the distributed amplifier the input transmission line and the output transmission line are called the gate and drain lines, respectively. The input signal travels down the gate line exciting each FET in turn, before being absorbed by a terminating resistor. The transconductance of the FETs amplifies the signal and feeds it into the drain line.

The main performance advantage of the distributed amplifier topology compared with the other methods is that it enables much wider bandwidth amplifiers to be produced. This is due to the fact that the input and output capacitances of the transistors are incorporated into the artificial transmission line structures which have very wide bandwidths. The result of this arrangement is that the amplifier can operate over a very broad frequency range, from very low frequencies up to close to the cut-off frequency of the artificial transmission lines.

The high frequency response is limited by a cut-off frequency ω_l defined by

$$\omega_l = 1/\sqrt{LC} \tag{3.2}$$

where L is inductance per unit length and C is capacitance per unit length.

The physical cause of this limitation is due to the transit time limitation. In practice parasitic resistors and capacitors associated with the FETs contribute to determining the cut-off frequency.

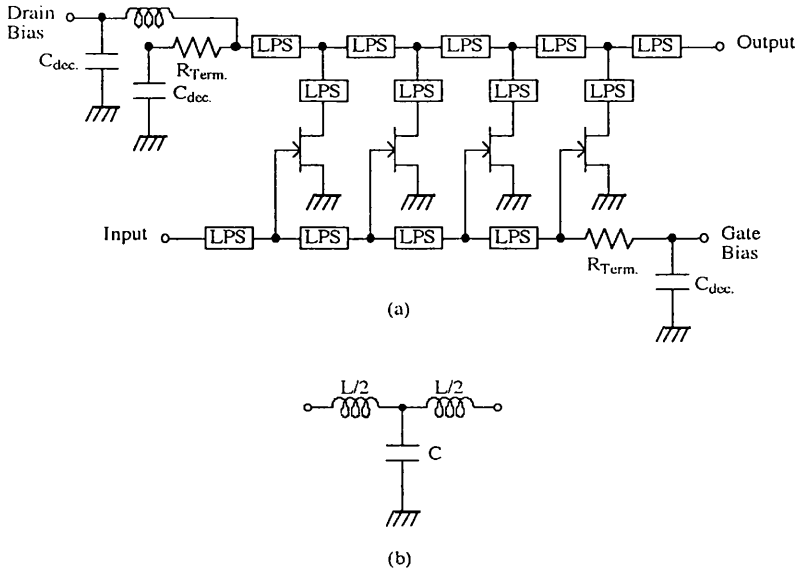

Figure 3.7: The schematic diagrams of (a) a conventional distributed amplifier and (b) a single low pass T-section.

The characteristic impedance of the transmission lines is given by

$$Z_0 = \sqrt{L/C} \tag{3.3}$$

where L is inductance per unit length and C is capacitance per unit length.

The high frequency response is limited by the parasitic capacitance of the inductor and the input capacitance of the FET, which cause high frequency roll off. In practice the gate and drain lines will have losses associated with them. As far as the gate line is concerned, the objective is to ensure that the gate-source capacitance associated with each FET has the same magnitude of AC voltage dropped across it despite the presence of gate line loss. There are two ways to deal with this, the first method is to insert a capacitor in parallel with each FET. The second method is to insert a capacitor in series with each FET. Unlike gate line loss, drain line loss can not be compensated for, it can only be minimised. The distributed amplifier has reduction in gain due to the loss in the dummy loads and resistive elements in the transmission lines [9].

3.4.2 The Derivative Superposition Approach

Derivative superposition [11] is a very general design method which can be used to design linear circuits with reduced distortion or nonlinear circuits with prescribed nonlinear characteristics. In this section we will discuss the principle operation

of this technique. Then, we will present results for a derivative superposition amplifier using high pass transmission lines to distribute the input and output signals.

3.4.2.1 Derivatives of a FET

At a very simple level a FET can be considered as a voltage controlled current source, where the controlling voltage and output current are at different ports of a 2-port element. Below a critical value of the input voltage, called the pinch-off voltage, v_{off}, the device output current is zero. Above this voltage the device has a current that rises with the control voltage. The controlling voltage is normally called the gate-source voltage (v_{gs}), and the output current is normally called the drain current (i_d). At a given point on this device characteristic it is possible to determine 1st, 2nd and 3rd order derivatives of the drain current with respect to signal voltage (v_{gs}) corresponding to small signal transconductance g_1, g_2 and g_3, respectively. By defining $v_{off} = 0$ such that at this voltage the second derivative of g_1, (g_3), tends to zero, the 1st derivative of transconductance (g_2) and the transconductance itself (g_1) are related as follow.

$$i_d = f\left(v_{gs} - v_{off}\right) \tag{3.4}$$

$$g_1 = \frac{d}{dv_{gs}} i_d \tag{3.5}$$

$$g_2 = \frac{d^2}{dv_{gs}^2} i_d \tag{3.6}$$

$$g_3 = \frac{d^3}{dv_{gs}^3} i_d \tag{3.7}$$

where f is a function describing the v_{gs} dependency of drain current.

A typical simulated plot of these derivatives against bias point for an idealised HEMT is shown in Figure 3.8. It can be seen that below the pinch-off voltage (v_{off}) all the derivatives tend to zero. Above v_{off}, the transconductance g_1 rises sharply reaching a peak and then begins to fall. It can also be seen that it takes a finite change in the controlling voltage v_{gs} to change from zero transconductance to maximum transconductance. This effect is called pinch-off. The pinch-off of a FET produces characteristic derivative features, consisting of a positive peak in g_2 and a positive and negative peak in g_3. The distortion in this region is considerably higher than in the high transconductance region. Another region of high distortion is associated with the change of mode due to the parasitic MESFET effect (see Section 2.2.3).

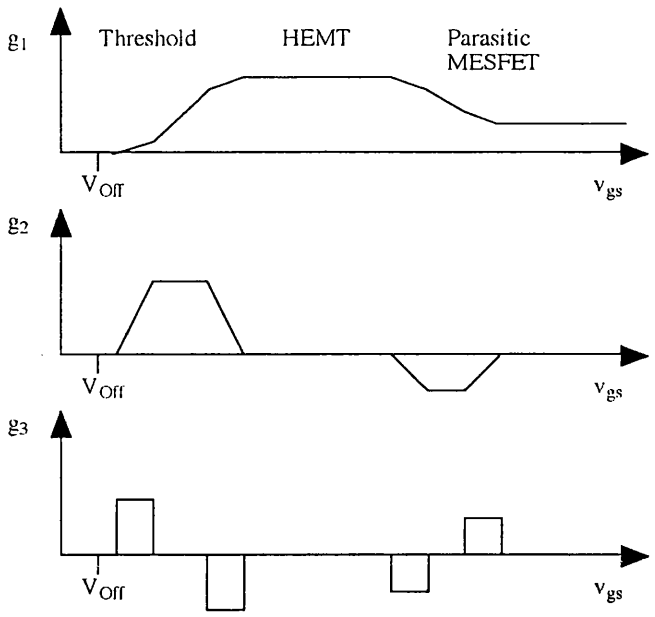

Figure 3.8: Derivatives of an idealised HEMT.

In Figure 3.9, the bias dependent derivatives for a real HEMT are shown. It can be seen that for the HEMT the 3rd order nonlinearity remains high in the region of high transconductance and low noise. This is because two regions of high distortion have merged into one another. The maximum and minimum of each of the derivatives, which can clearly be seen in Figure 3.9, produce nulls in the next highest derivative.

In Figure 3.10, the bias dependent derivatives for a real MESFET are shown. It can be seen that the derivatives of a MESFET have a similar signature to that of the HEMT derivatives except that, the gain keeps on rising with increasing gate-source voltage.

3.4.2.2 Derivative Superposition Topology

Superposition has many traditional applications in electronics. Superposition forms the core of Fourier waveform analysis. The important parameters are the relative amplitude and phase of each of the harmonic components. In order to create an arbitrary response the component functions must have peaks. The adjustment of the spacing between the peaks controls the level of the ripple and the adjustment of the amplitudes of the peaks controls the curvature of the response.

As we have seen in the previous section, a FET has peaks in its transconductance derivatives g_2 and g_3, and a sign reversal in g_3 as a function of V_{GS}. Now by combining these derivatives with the correct amplitude it is possible to achieve

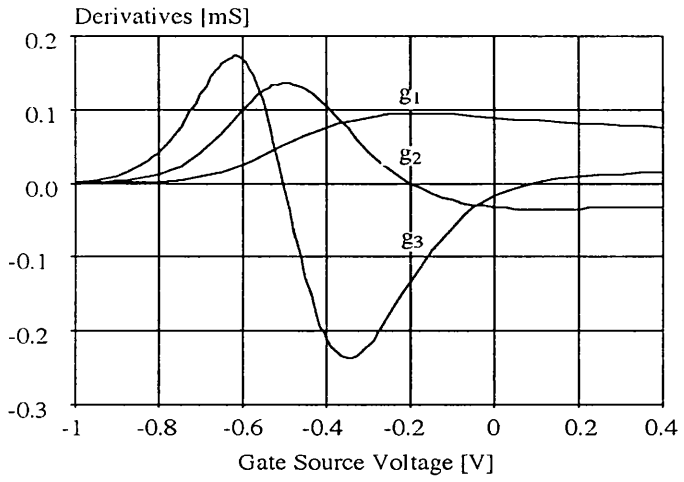

Figure 3.9: The bias dependent derivatives for a real HEMT (NE32684).

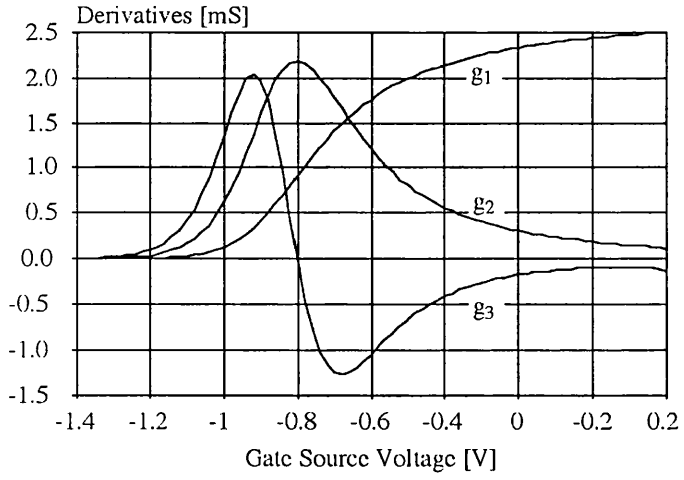

Figure 3.10: The bias dependent derivatives for a real MESFET (MGF1400).

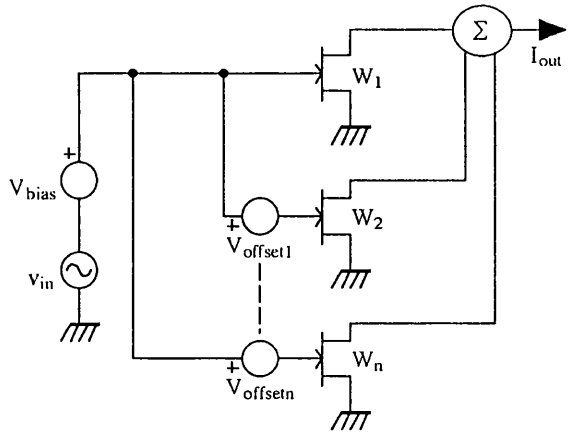

Figure 3.11: The schematic diagram of the derivative superposition topology.

a significant reduction of both 2nd and 3rd order distortion over a range of gate bias. We assume at this stage that all components are either in phase or anti phase with respect to each other. A simple generic topology for derivative superposition has been proposed for implementing this idea [12], [13] which is shown in Figure 3.11.

The structure consists of a set of FETs connected in parallel at their inputs and outputs with different gate widths and with different DC gate bias offsets from a common bias voltage. The same RF drive is applied to each device. The distortion products from each FET must be arranged to be reasonably well amplitude and phase matched across the frequency band of interest.

Having discussed the principles of the derivative superposition approach we will next review an example of a distributed derivative superposition amplifier based on high-pass transmission lines capable of providing low distortion.

3.4.2.3 Derivative Superposition Amplifier Based on High-pass Transmission Lines

In this section we will review the implementation of a derivative superposition amplifier which uses high-pass lumped element transmission lines in order to distribute the signals [14], [15]. A high-pass transmission line can be achieved by performing the low pass to high-pass transformation on the classic low pass lumped element transmission line. In Figure 3.12(a) we show a single ideal high-pass transmission line section.

In practice, real inductors have parasitic parallel capacitance (C_{PP}), and real capacitors have parasitic series inductance (L_{PS}). This leads to an equivalent

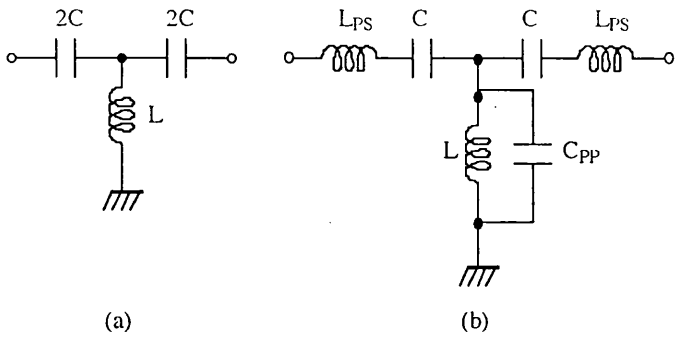

Figure 3.12: Lumped-element high-pass transmission line sections. (a) Ideal model and (b) realistic model.

circuit for the high-pass T section of 3.12(b). At low frequencies, it can be argued that L and C are the dominant components, and the structure behaves as a high-pass transmission line. However, at high frequencies, L_{PS} and C_{PP} are now the dominant components within the circuit, and subsequently form a parasitic low pass transmission line. Thus, the overall structure has a bandpass response. If both lines do not have the same characteristic impedance (i.e. within 10 % of Z_o), significant passband ripple will occur.

In order to minimise the passband ripple, L and C must be chosen (or designed), such that their parasitic components satisfy the following relationship.

$$Z_o = \sqrt{\frac{2L}{C}} \approx Z_{op} = \sqrt{\frac{2L_{PS}}{C_{PP}}} \tag{3.8}$$

where Z_o is the characteristic impedance of the high-pass transmission line, and Z_{op} is the characteristic impedance of the parasitic low pass transmission line. For low group delay across the centre of the passband and maximum bandwidth, it is necessary for L to be much larger than L_{PS}. A possible advantage of the high-pass structure is that the relatively lossy inductor is now in the high impedance shunt branch rather than in the low impedance series branch, reducing the loss of the line. There is also some scope for absorbing FET intrinsic capacitance into the parasitic capacitance C_{PP} of the inductor L.

High-pass transmission lines have a number of useful advantages over the classic low pass transmission lines. These include DC isolation between sections, lower loss per section, and a much higher maximum frequency of operation, far beyond the natural self-resonant frequencies of the passive components used. The authors in [14] have constructed a five-section high-pass transmission line which has a very broad bandwidth, good insertion loss and low phase shifting problems. In Figure

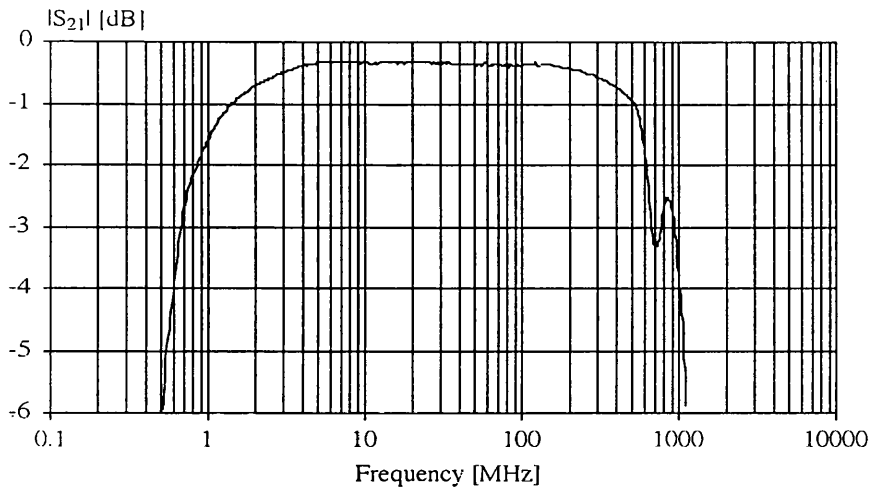

Figure 3.13: Measured $|S_{21}|$ of a five-section surface mount lumped-element high-pass transmission line.

3.13 we show the $|S_{21}|$ response of this line.

It can be seen that the design has a bandwidth of about 3 decades spanning from 700 kHz to 700 MHz despite of an inductor self-resonant frequency as low as 10 MHz. In Figure 3.14 we show the return loss characteristics of the high-pass transmission line.

It can be seen that the line has a good return loss up to about 1 GHz showing a good approximation to a 50 Ω match over its working bandwidth. In Figure 3.15 we show the phase shift of this line with frequency.

It can be seen from Figure 3.15 that the circuit has a low rate of change of phase shift with frequency in the mid band region (circa $\pm 60^o$ between 4-100 MHz).

These results confirm the attractiveness of high-pass transmission lines for distribution of input and output signals in derivative superposition circuits.

3.4.2.4 Super Deriv Software

Super Deriv is a CAD tool previously developed at UCL for the design of derivative superposition circuits [16]. This software facilitates the design of derivative superposition circuits and is capable of giving a very quick assessment of circuit performance. The tool is still under development, but the current version (4.1) is able to explore the variation of derivatives with respect to bias for different load resistances. It is also capable of providing simulations of output signal amplitude and distortion versus input signal level. It can also perform spectral regrowth simulations. Super Deriv also allows the use of measured distortion data for the

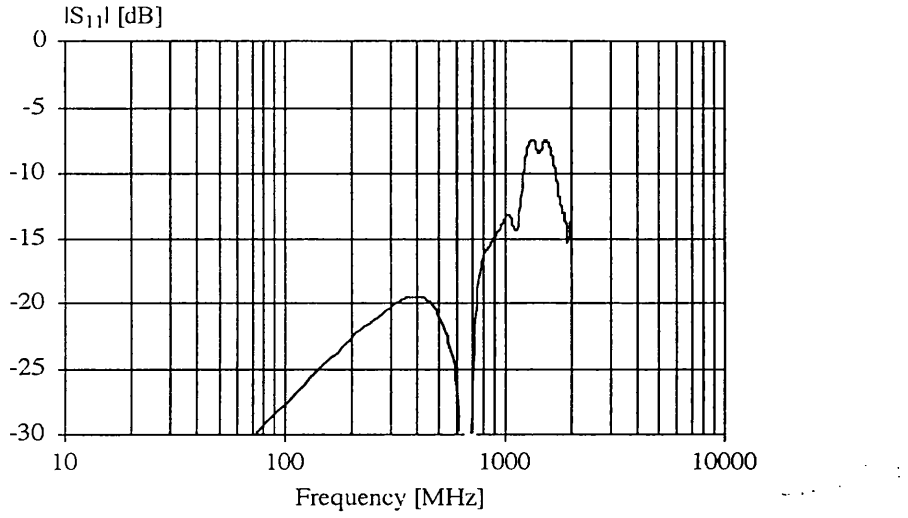

Figure 3.14: Measured $|S_{11}|$ of a five-section surface mount lumped-element high-pass transmission line.

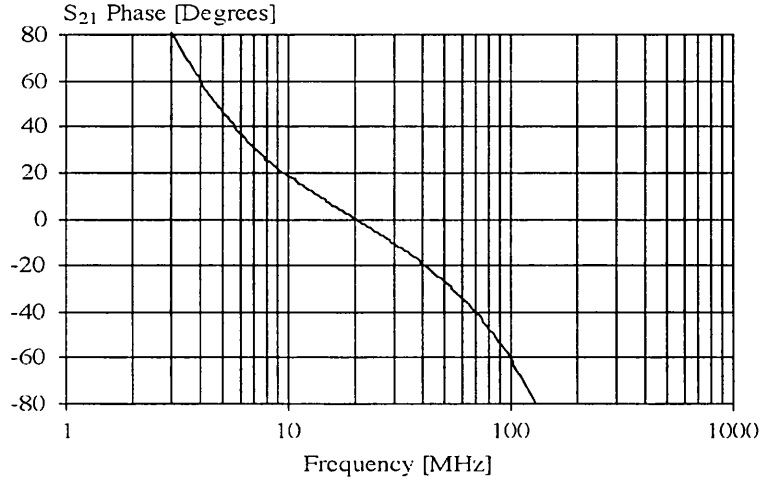

Figure 3.15: Measured phase of S_{21} of a five-section surface mount lumped-element high-pass transmission line.

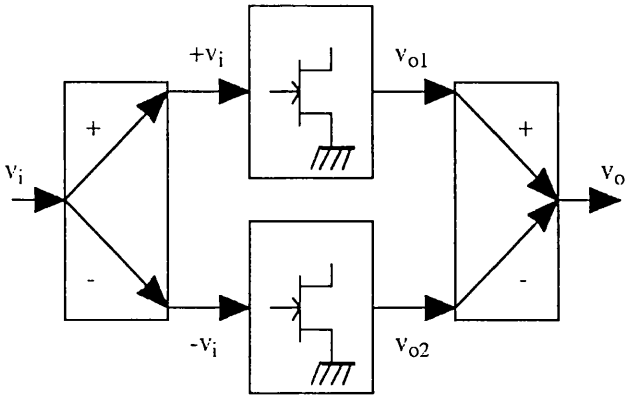

Figure 3.16: Schematic diagram of a balanced structure suitable for linear applications.

design of small signal amplifiers.

Examples of the use of the derivative superposition method in various applications will be given in Sections 3.5.6, 3.6.5 and 3.7.3.

3.5 Comparison of Circuit Linearisation Design Techniques for Small and Medium Signal Applications

3.5.1 Balanced Amplifier with Passive Splitter/Combiner

One of the most popular linearisation techniques involves the use of balanced circuits [17]. Balanced systems consist of two paths through a circuit, which have anti-phase signals as shown in Figure 3.16.

In balanced systems it is common to use power-combining components to combine the outputs of solid state devices together [7], [9]. These include hybrids and power dividers. These components isolate the individual devices from each other and maintain input and output impedance levels. Since these networks are reciprocal, the same network can be used as a combiner or a divider. The simplest type of power combiner/divider is the two way splitter. Two way splitters can be categorised according to the phase relationship between the two output signals. The outputs of the splitter/combiner can be either in-phase or quadrature splitters [7], [9] (e.g. Lange and Branch-Line quadrature couplers) or they can be in anti-phase with each other (e.g. Ring hybrid or Magic-T). The outputs of the splitters/combiners shown in Figure 3.16 are in anti-phase.

Considering a polynomial representation of transconductance nonlinearity of an active device, for v_{o1} and v_{o2} of Figure 3.16 we have the following expressions.

$$v_{o1} = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + ... \tag{3.9}$$

$$v_{o2} = a_0 - a_1 v_i + a_2 v_i^2 - a_3 v_i^3 + ... \tag{3.10}$$

where v_i is the input signal.

Combining the v_{o1} and v_{o2} yields the following expression for the output signal of Figure 3.16.

$$v_o = v_{01} - v_{02} = 2a_1 v_i + 2a_3 v_i^3 + ... \tag{3.11}$$

It can be seen from Eq. 3.11 that the even order distortion products are cancelled.

The balanced technique has the advantage of being broadband. The problems associated with this technique include low efficiency due to the losses that can occur in the hybrids and the output conductance effects.

3.5.2 Multi-tanh Technique

The multi-tanh technique [18] is a method for linearising the transconductance of a Bipolar Junction Transistor (BJT) using a number N of emitter-coupled pairs. This technique has many applications in small and medium signal applications as well as nonlinear applications.

The relation between the collector current, I_C, and the base emitter voltage, V_{BE}, in a BJT is given by the following expression.

$$I_C = I_0 \exp(\frac{V_{BE}}{V_t}) \tag{3.12}$$

where I_0 is the saturation current and V_t is the threshold voltage.

The differential pair based on BJTs, shown in Figure 3.17 interested researchers for nonlinear function synthesis purposes [19].

The transfer characteristic of a differential pair can be expressed as

$$\frac{I_x - I_y}{I_0} = \tanh \frac{v_{in}}{v_t} \tag{3.13}$$

The main problem with this approach was the fact that the tanh function does not have a zero derivative at the peak value whereas the sine function has zero derivative at $\pm\pi/2$.

Gilbert [20] proposed a more comprehensive implementation to overcome this problem. In this configuration multiple differential pairs were used. Hence, the

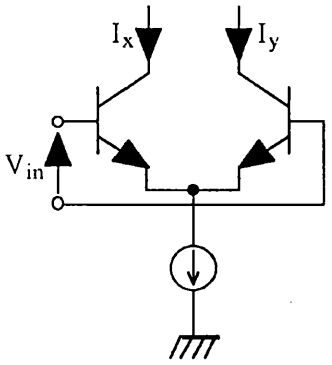

Figure 3.17: Schematic diagram of a single BJT differential pair.

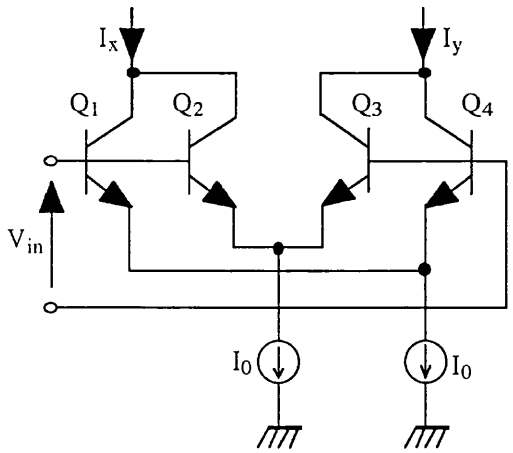

Figure 3.18: The multi-tanh doublet.

name multi-tanh. The basic multi-tanh doublet uses two differential pairs. This is shown in Figure 3.18.

The transistors used have different emitter-area ratios of A, which introduce equal offset voltages with different polarities. The offsets split the two tanh functions apart (when plotted against instantaneous input voltage). By a correct choice of A, the resulting transfer function can produce a region close to $V_{RF} = 0$ over which the incremental gain is almost flat (constant g_m), with a resulting improvement in linearity.

Multi-tanh doublets have been used in various applications such as mixers. The multi-tanh triplet is also a very useful cell which is capable of providing further extension in the linear range at the expense of complexity. It should also be noted that none of these variants readily match to a 50 Ω system and require impedance transformation at the input. Also since the transconductance of a BJT is temperature sensitive temperature compensation techniques have to be incorporated.

This technique is not entirely suitable for low noise amplifiers due to noise of current sources and since emitter is not grounded, this reduces gain and for power amplifiers reduces output voltage swing and efficiency.

3.5.3 Translinear Technique

Translinear circuit theory was first proposed by Gilbert [21]. These circuits are based on the fact that the transconductance of a bipolar junction transistor (BJT) is linearly proportional to its collector current. Translinear circuits can be used to design both linear and nonlinear circuits. In this section we will consider the linear translinear circuits. The nonlinear behaviour will be discussed in Section 3.6.3.

The behaviour of translinear circuits is entirely described in terms of current ratios within the circuit and voltages are of much less significance. In the translinear technique the nonlinearity of transistors are exploited to obtain a linear current transfer function for the circuit. In Figure 3.19 we show a very simple example of a translinear circuit employing a single loop.

It is apparent that in this circuit the output current will be scaled by the emitter area. The key to the translinear principle is the logarithmic relationship between I_C and V_{BE} (see Eq. 3.12) which provides a linear operating region. The main problem with this technique is the fact that it suffers from frequency dependant distortion effects [5].

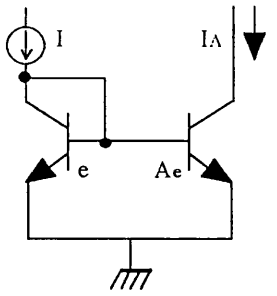

Figure 3.19: Current mirror, an example of translinear circuit.

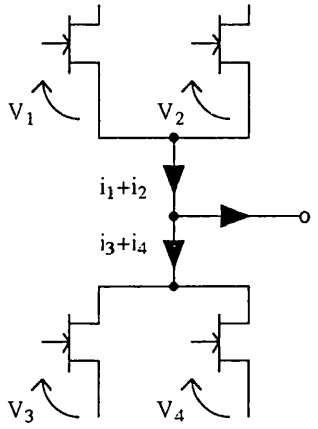

Figure 3.20: The push-pull architecture suitable for combiner realisation.

3.5.4 Balanced Amplifier with Active Splitter/Combiner

Balanced amplifiers using passive dividers and combiners were discussed in Section 3.5.1. In this section we will describe balanced structures using active splitters and combiners. This kind of configuration can be used for both linear and nonlinear applications. We will first describe the linear applications and then, in Section 3.6.4 we will treat the nonlinear applications.

The output combiner of Figure 3.16, can be realised using active techniques. These include the use of differential pairs or push-pull structures. The differential pair implementation is not suitable for power output stages and it is more suitable for downconverters. The push-pull architecture is shown in Figure 3.20.

The push-pull is used to implement a balanced system in which the currents (i.e. outputs) are subtracted from each other. This set-up offers a number of advantages which include being MMIC compatible and being broadband. In this configuration it is necessary to generate the non-grounded voltages V_1 and V_2 using active circuits. There are various ways of achieving this with inverting and non-

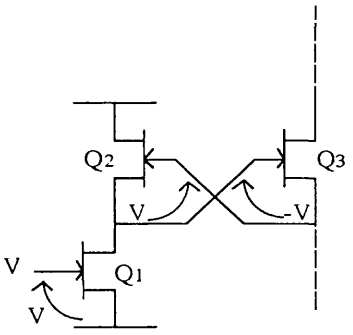

Figure 3.21: An inverting voltage floatation building block.

inverting voltage floatation structures [22]. Figure 3.21 shows a typical voltage floatation building block.

The voltage V in Figure 3.21 on the gate-source port of MESFET Q_1 generates a drain current which flows into Q_2. Therefore, the gate-source voltage of Q_2 is also equal to V. MESFET's Q_2 and Q_3 make up an inverting current mirror which can be regarded as a perfect inverter of the gate-source voltage of Q_2. Therefore, the gate-source voltage of Q_3 is $-V$. Hence the $+V$ and $-V$ voltages required for the operation of the balanced amplifier are obtained by using active devices.

This technique is quite powerful since it provides a linear relationship even though the devices are nonlinear. The main problem with this technique is the frequency dependant distortion effects due to the parasitics present in the circuit [5].

3.5.5 Doherty Amplifier

The Doherty amplifier was first proposed in [23]. The circuit topology is shown in Figure 3.22.

The circuit consists of two amplifiers, a carrier amplifier and a peak amplifier. The carrier amplifier is a class B amplifier whereas the peak amplifier is designed to amplify only those signals which exceed some minimum threshold. This can be achieved by biasing the peak amplifier below its pinch off voltage, providing a class C amplifier operation. This causes the peak amplifier to turn on when the carrier amplifier starts to compress. The output power from the two amplifiers is combined using a $\lambda/4$ impedance transformer. At low output powers the carrier amplifier operates linearly, reaching saturation (and maximum efficiency) at some transition voltage below the system peak output voltage. At high output powers the carrier amplifier remains saturated and the peak amplifier operates linearly.

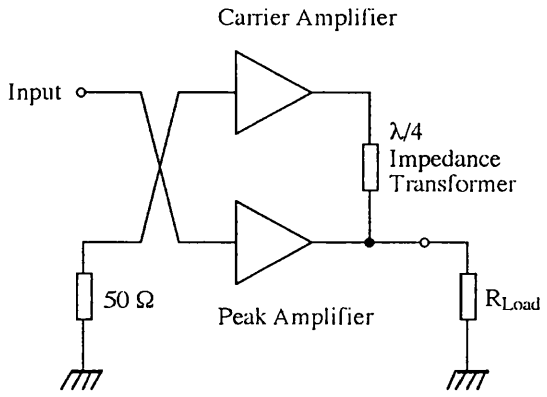

Figure 3.22: Doherty amplifier topology.

This arrangement enables the Doherty system to produce a significant increase in efficiency [24]. The first fully integrated PHEMT Doherty amplifier MMIC at ku-band was reported in [25].

3.5.6 Derivative Superposition

It has been shown that it is possible to use the principle of derivative superposition to simultaneously achieve 2nd and 3rd order distortion reduction [11]. The overall schematic of the demonstration board is shown in Figure 3.23. In this circuit 2 MESFETs were used. Since the devices used were discrete, a Pi-section attenuator has been used to scale the current of the secondary device. Bias tees have been used to bias each FET individually and a transformer hybrid has been used to subtract the output currents. Due to this subtraction, the overall gain level of the circuit was low. It has been shown [11] that distortion reductions of 10 dB for the 2nd order distortion and 8 dB for the 3rd order distortion have been achieved.

In [13] the authors have implemented an amplifier based on four HEMTs in order to achieve low IMD3 with maximum gain over a wide range of input powers. The circuit diagram is shown in Figure 3.24.

The circuit has been optimised to produce low 3rd order intermodulation distortion across a wide input voltage variation, rather than a single notch. The aim of this was to extend the dynamic range of the improvement. Since discrete devices were used, Pi-section attenuators were used at the drains of the FETs to realise the effect of the width scaling of the transistors. A gain improvement of 8 dB compared to a single FET amplifier has been reported. This was due to the fact that the authors were able to operate in the high g_m region. An improvement of 20-25 dB in IMD3 (for -15 dBm to -11 dBm input power range) has been mea-

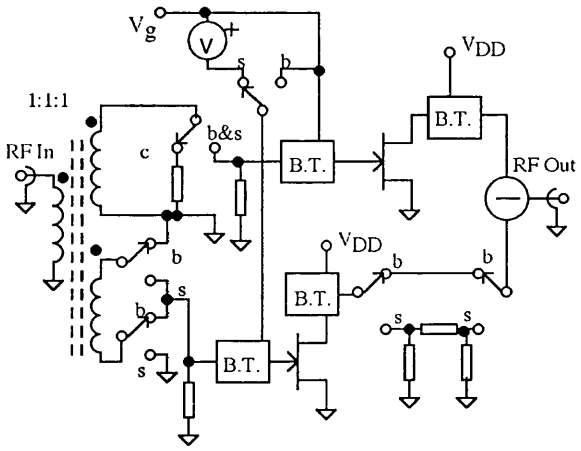

Figure 3.23: Schematic of the Linear Law Demonstrator Board. The board allows the comparison of the Linear Law design, a single common source FET and a balanced FET amplifier. The switch positions are denoted by balanced (b), common source (c) and synthesised (s).

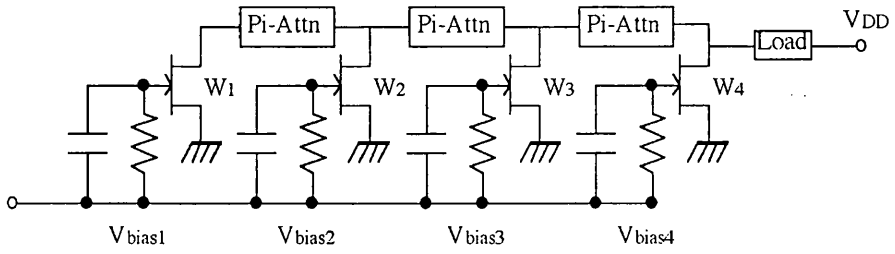

Figure 3.24: Schematic circuit diagram suitable for a gain stage with desired distortion characteristics fixed by the derivative superposition method.

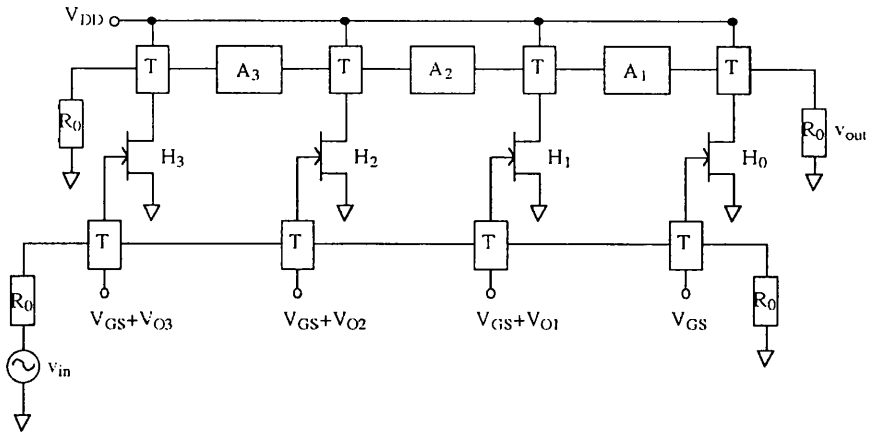

Figure 3.25: Schematic diagram of a DS amplifier. T's are the high-pass transmission line sections and A's are the pi-section attenuators. Devices are NE42484C HEMTs.

sured. The IMD2 was shown to be 5 dB lower than the case of a single device biased for minimum IMD3 (i.e. for -15 dBm input power).

A derivative superposition amplifier using high-pass transmission lines has been implemented [26]. The amplifier incorporated four discrete HEMT's. The circuit diagram is shown in Figure 3.25.

The devices are arranged in parallel with each other with different DC gate bias voltages. Attenuators (A_i) are used to implement device width scaling. High-pass transmission lines have been used for feeding the input and output signals. The measured bias dependant distortion of the design is shown in Figure 3.26.

It can be seen that the 3rd order distortion has been reduced by about 15-20 dB over a gate bias range of 300 mV. This is anticipated to lead to good suppression of 3rd order intermodulation distortion up to an input level of 5 dBm. The comparison of how the distortion varies with input power for both the DS amplifier and for a single device is shown in Figure 3.27.

It can be seen that significant 3rd order intermodulation distortion reduction (circa -20 dB) occurs up to an input power of 5 dBm, and then the distortion rises more rapidly. The 2nd order distortion has increased by a small amount but since it introduces products which are out of band, it is of much less concern. It can also be seen that the derivative superposition amplifier has a higher 1 dB compression point than the single HEMT case. This is due to the fact that the outputs of the derivative superposition amplifier circuit have been added together which results in a higher overall gain level. Although the DS amplifier uses four FETs, the power consumption is little more than that for a single FET due to the

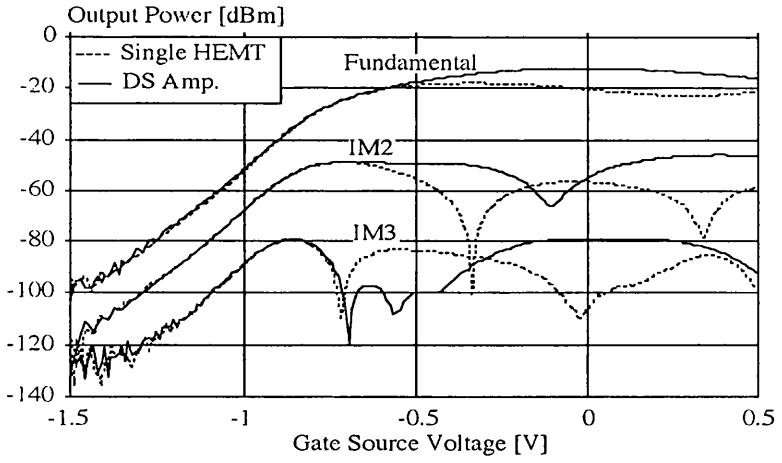

Figure 3.26: Comparison of the intermodulation distortion versus gate bias for both a single HEMT and the derivative superposition amplifier.

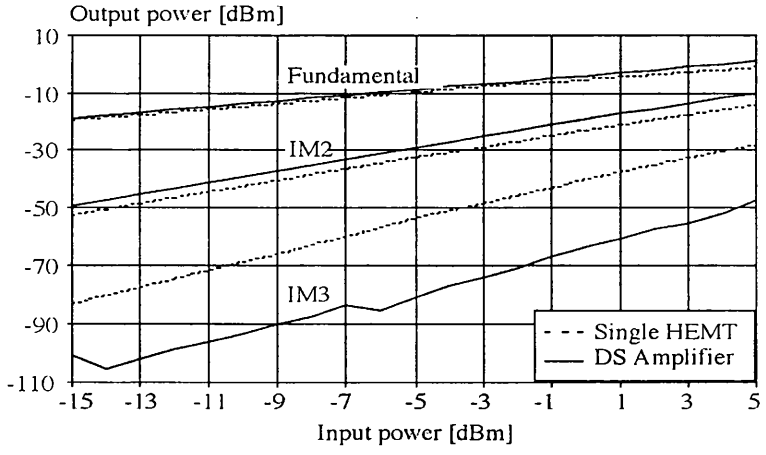

Figure 3.27: Comparison of the intermodulation distortion versus input power for both a single HEMT and the derivative superposition amplifier; $V_{GS} = -0.55V$.

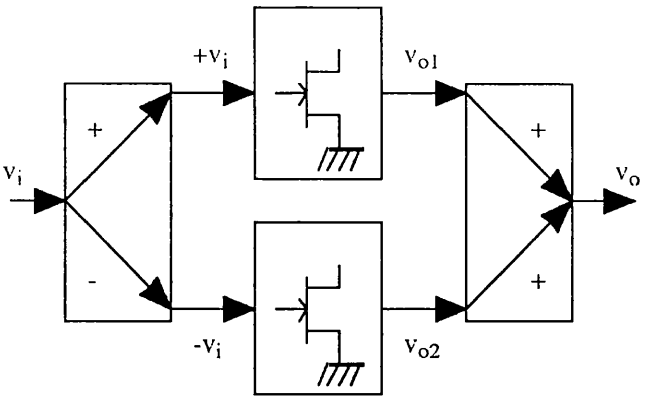

Figure 3.28: Schematic diagram of a balanced structure suitable for nonlinear applications.

fact that the secondary devices are biased close to the pinch-off.

Having reviewed some of the circuit linearisation design techniques for small and medium signal applications we will next review some of these techniques for nonlinear applications.

3.6 Comparison of Design Techniques for Nonlinear Applications

3.6.1 Balanced Amplifier with Passive Splitter/Combiner

The schematic diagram for a balanced structure suitable for nonlinear applications is shown in Figure 3.28.

The schematic diagram shown in Figure 3.28 is the same as the one shown in Figure 3.16, except that the outputs at the combiner are in phase. Therefore, v_{o1} and v_{o2} signals, given by Eq. 3.9 and Eq. 3.10, respectively, are added together in this application. So, the output is as follows.

$$v_o = v_{o1} + v_{o2} = 2a_0 + 2a_2 v_i^2 + 2a_4 v_i^4 + ... \tag{3.14}$$

where v_i is the input signal.

It can be seen from Eq. 3.14 that the odd order harmonics have been cancelled.

In practical situations 180 degrees balanced structures do not entirely eliminate the unwanted harmonic terms. This is due to the mismatches in the splitting and combing circuits.

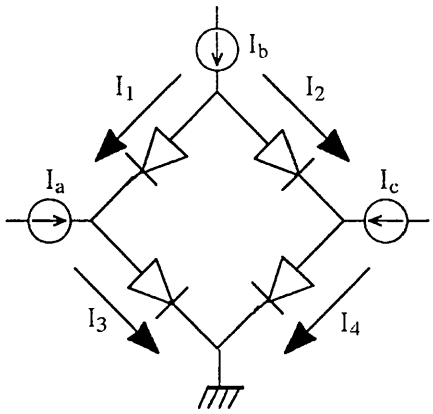

Figure 3.29: The translinear principle; a diode bridge loop.

3.6.2 Multi-tanh Technique

The multi-tanh linearisation technique for small and medium signal applications was discussed in Section 3.5.2. However, it is also possible to make use of this technique in nonlinear applications. There is a region on the characteristic of a BJT where g_m rises linearly with bias. By using several BJTs in a multi-tanh configuration, it is possible to superimpose the linear parts of g_m's next to each other and obtain a wide signal span where g_m is linear with bias. Therefore, differentiating this to get g_2, will result in a high and constant g_2 with bias. Thus, the g_3 (differentiating g_2), is minimised. This corresponds to a very low 3rd order distortion product.

The BJT multi-tanh technique has been successfully used in implementing high performance mixers [27]. This technique suffers from frequency dependant distortion effects [5].

3.6.3 Translinear Technique

In Section 3.5.3 we discussed the linear aspects of translinear circuits. In this section we will discuss the nonlinear concept of translinear circuits.

The principle of this kind of circuit is the idea of a set of forward biased diodes which are integrated on the same substrate. The temperature is an important issue and must be identical for all the elements involved in the loop. An example of this kind of translinear loop is a diode bridge shown in Figure 3.29.

The fundamental assumptions and conditions for this loop are the following. The voltage across each diode is assumed to be defined by the exponential diode law. There must be an even number of diodes (at least two) in the loop. The

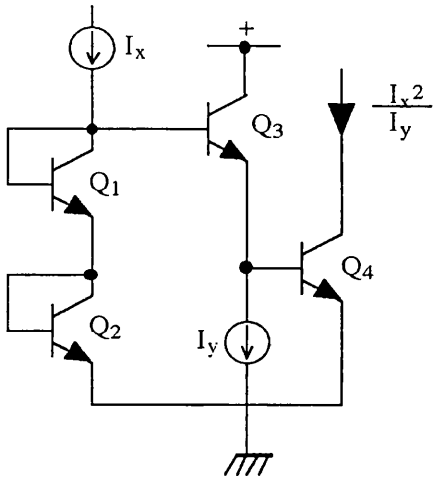

Figure 3.30: A simple one-quadrant translinear squarer.

number of clockwise-facing junctions must equal the number of counter clockwise-facing junctions and the sum of voltages around the loop is assumed to be zero. Therefore, the product of currents in the clock-facing and counter clock-facing diodes are equal. This principle is applied to Bipolar Junction Transistors (BJTs) since it can be assumed that the common-emitter current gain (β) is constant with collector current and also the fact that β is quite large. This idea has led to the development of a lot of analogue computational circuits. Examples include Triangle to Sine wave conversion circuits and RMS-DC converters.

The simplest one-quadrant translinear squarer circuit uses four transistors. The circuit diagram of this is shown in Figure 3.30.

Multiple squarers can be used to form other kinds of frequency multipliers such as frequency triplers. An advantage of the translinear technique compared to the multi-tanh technique is the fact that it does not suffer from temperature drift problems since performance depends on current ratios only. The problems associated with this technique include, frequency dependant distortion effects [5] due to base-emitter capacitance and existence of emitter resistance which causes deviation from ideal translinear operation.

It has been shown that it is possible to extend the translinear loop principle to MOSFETs in order to realise various algebraic functions [28].

3.6.4 Balanced Amplifier with Active Splitter/Combiner

In Section 3.5.4 balanced amplifiers with active splitters and combiners for linear applications were discussed. In this section we will describe some of the applica-

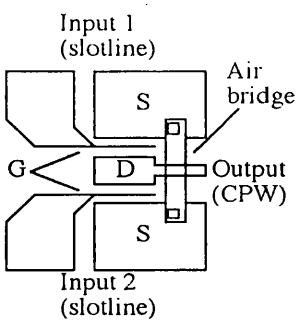

Figure 3.31: Realisation of an active in-phase power combiner (referred to as line unified or LU-FETs).

tions of this technique for nonlinear purposes.

Figure 3.31 shows an active implementation of the in-phase power combiner block of Figure 3.28 using two common-source FETs.

The source stripes act as the common electrode and are connected through an air bridge. This results in two input slotlines (G-S) and an output CPW (S-D-S). The slotlines and the CPW are related to each other through unilateral FETs. Therefore, when the slotlines and the CPW are used for input ports and output port, respectively, an in phase combiner is achieved. The realisation of active splitters have also been discussed in the literature [29], [30].

3.6.5 Derivative Superposition

The use of derivative superposition topology in the linearisation of small and medium signal applications was discussed in Section 3.5.6. In this section we will show that it is possible to use derivative superposition in the design of nonlinear applications such as frequency doublers and frequency triplers.

A frequency doubler using derivative superposition has been proposed [11]. A photograph of the prototype MMIC DS frequency doubler design is shown in Figure 3.32. The technology used is the MMT F20 MESFET process.

The response of this frequency doubler is shown in Figure 3.33.

It can be seen that a maximum suppression of unwanted products of 18 dB has been achieved for the prototype frequency doubler. The dominant unwanted product is the 4th harmonic.

A frequency tripler using derivative superposition has been demonstrated [11]. A photograph of the prototype MMIC DS frequency tripler design is shown in Figure 3.34. The technology used is the MMT F20 MESFET process.

The response of this frequency tripler is shown in Figure 3.35.

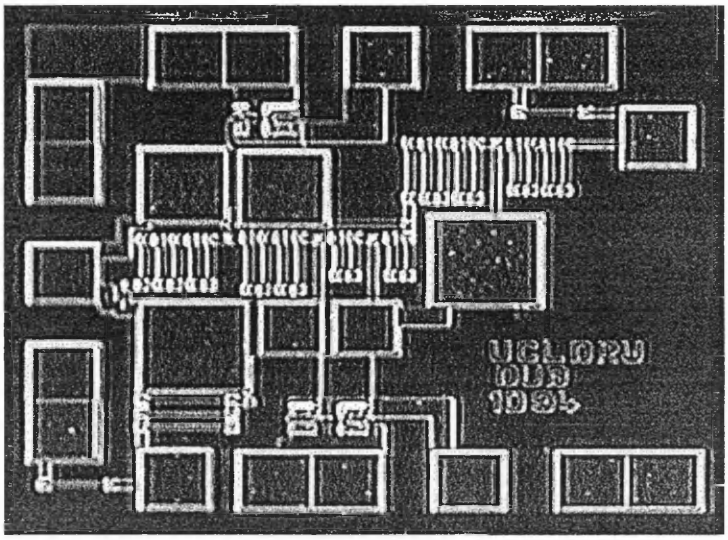

Figure 3.32: Photograph of the MMIC DS frequency doubler.

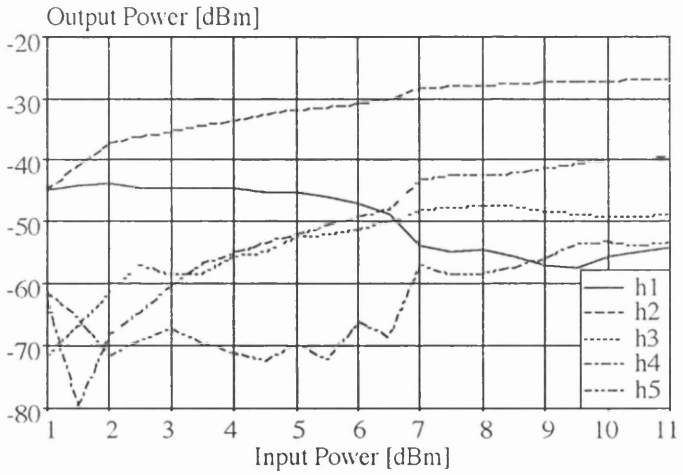

Figure 3.33: Measured performance of the derivative superposition frequency doubler.

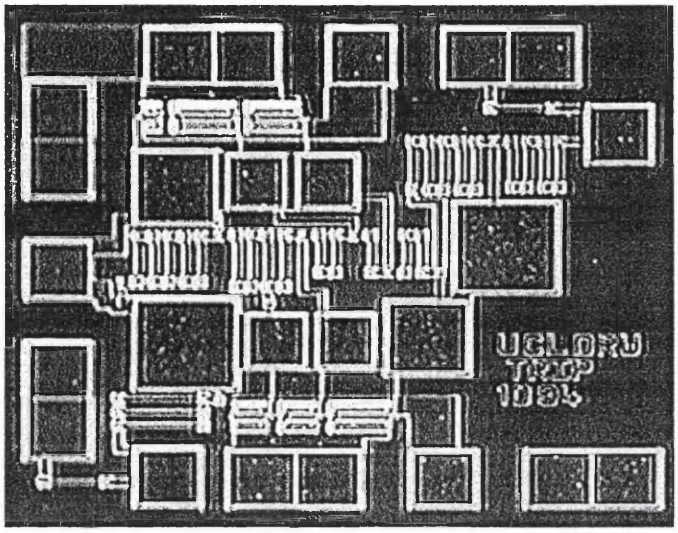

Figure 3.34: Photograph of the MMIC DS frequency tripler.

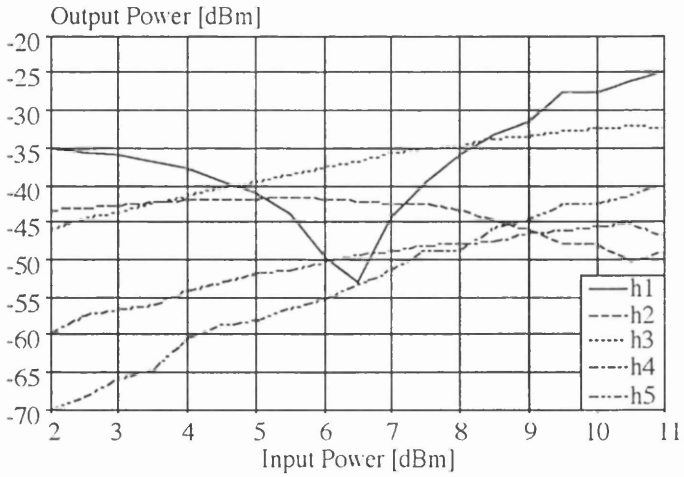

Figure 3.35: Measured performance of the derivative superposition frequency tripler.

It can be seen that a maximum suppression of unwanted products of 7 dB has been achieved for the prototype frequency tripler. The dominant unwanted product is the 2nd harmonic.

Having reviewed some of the design techniques for nonlinear applications we will next review some of the most popular techniques for power amplifier design.

3.7 Techniques for Power Amplifier Design

3.7.1 Discussion of Some of the Amplifier Configurations

There are various terms which are used to specify the performance of a power amplifier. These include the following. The output power level (P_{out}) of a power amplifier is given by the following expression.

$$P_{out} = \frac{(V_{ds} - V_{sat})^2}{2R_L} \tag{3.15}$$

where V_{sat} is the saturation voltage of the transistor, V_{ds} is the drain-source voltage and R_L is the load resistance. Another frequently used parameter is the power-added efficiency (η_{PAE}), which is given by the following expression.

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{V_{ds} I_d} \times 100 \tag{3.16}$$

where P_{in} is the input power and I_d is the mean drain current. Since the gain (G) is given by

$$G = \frac{P_{out}}{P_{in}} \tag{3.17}$$

and the applied DC power is

$$P_{dc} = V_{ds} I_d \tag{3.18}$$

therefore, the Eq. 3.16 can be arranged to yield the following.

$$\eta_{PAE} = \frac{P_{out}}{P_{dc}}(1 - \frac{1}{G}) \times 100 \tag{3.19}$$

where the drain efficiency is defined as the following ratio.

$$\eta_d = (\frac{P_{out}}{P_{dc}}) \times 100 \tag{3.20}$$

The class of an amplifier is determined by the bias applied to the transistor. There are many different classes of amplification. The most popular classes of

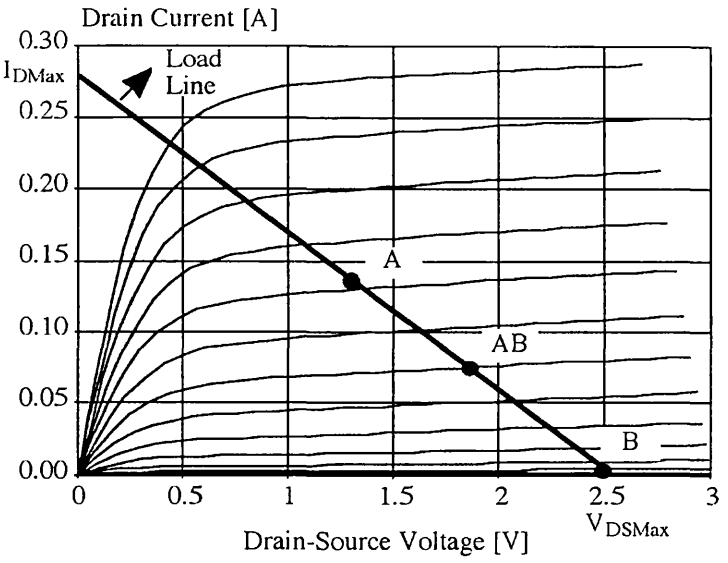

Figure 3.36: Possible bias points for class A, B and AB amplifiers.

amplifiers include class A, B, AB, C, D and E. These will be discussed in this section.

Class A, B and AB Amplifiers [1], [2]

In a class A amplifier, the bias conditions allow the output current to flow at all times corresponding to a conduction angle of the transistor of 360 degrees. The class A amplifier is the most linear amplifier type. The maximum efficiency of a class A amplifier is 50 %.

In a class B amplifier the conduction angle for the transistor is about 180 degrees. The maximum efficiency in a class B amplifier is 78.5 %, which makes it more efficient than class A amplifiers. However the class B amplifier is less linear than the class A amplifier and, therefore, it produces a considerable amount of distortion.

In class AB amplifiers [31] the collector current flows for a conduction angle between 180 and 360 degrees of the input signal. The efficiency of this class is between 50 to 78.5 %.

In Figure 3.36 we show typical bias points for class A, B and AB operation of a FET amplifier.

Class C Amplifiers [32]

The conduction angle in a class C amplifier is significantly less than 180 degrees. The transistor is biased in such a way that under steady state conditions no drain current flows. The linearity of a class C amplifier is very poor but its efficiency is about 85 %. In order to bias a bipolar transistor for class C operation, it is

necessary to reverse bias the base-emitter junction.

Class D and E Amplifiers [33], [34]

These are usually characterised as high efficiency modes of operation. Both are so called switch-mode systems. Theoretical efficiencies can be 100 %. In practice only 90 % to 95 % efficiency is possible due to effects such as finite switching times and device output capacitance. There are two types of class D amplifiers, a current switching amplifier which must be driven with a square wave signal and a voltage switching amplifier which can be driven with either a square wave or sine wave input. The sine wave is more common.

Class E amplifier is basically a variation of class D amplifier with an LC network at its output port. Class E amplifier is a relatively narrow band system due to the LC network whereas, class D amplifier is a broad band system. Class E amplifier is about 5-10 % more efficient than class D amplifier.

3.7.2 System Level Linearisation Techniques

In general transistor amplifiers with adequate efficiency and output power have distortion which is unacceptably high. System level techniques are used to reduce distortion to an acceptable level.

There exist a number of system level distortion reduction techniques. These include feedforward, feedback, predistortion, and balanced amplifiers. In the following sections we will give a general overview of these techniques together with their drawbacks.

Feedforward

In feedforward technique [9], [35], [36], [37] the input signal is split into two paths as shown in Figure 3.37. The main channel provides most of the power gain and the lower power reference channel provides the inverse of all distortion products present within the main channel. The recombination of the channels ideally results in distortion cancellation at the output.

The main disadvantage of this technique is the loss in the couplers and the need for two well matched amplifiers (the second amplifier does not contribute to output power), which gives rise to lower efficiency and increased weight. Feedforward also requires a considerable increase in RF hardware complexity and phase tracking in the cancellation loop over frequency and temperature which can be very challenging.

Feedback

The feedback technique [38], [39] is the oldest method of linearisation of amplifiers. This technique can be implemented at baseband, IF or RF. The circuit

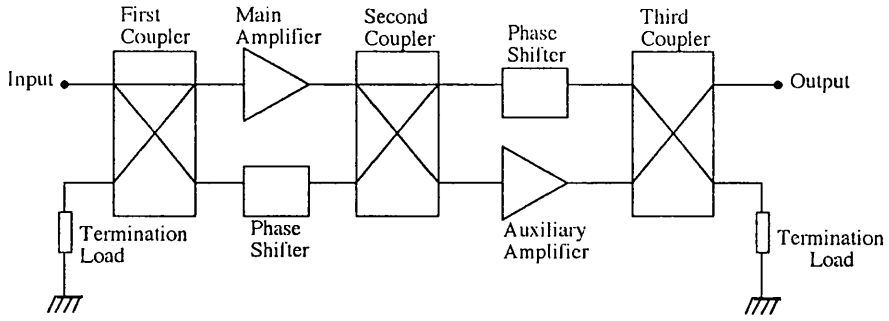

Figure 3.37: Schematic diagram of the feedforward linearisation technique.

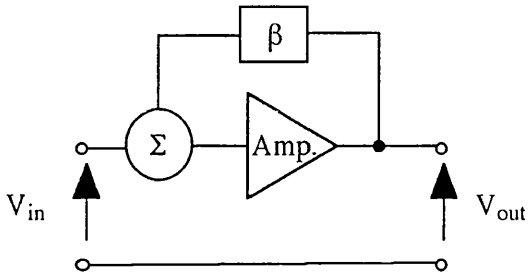

Figure 3.38: Schematic diagram of the feedback linearisation technique.

diagram of a feedback system is shown in Figure 3.38.

This technique is very simple to implement. However, narrow bandwidth and oscillation problems associated with this technique are the two major problems. Also, due mainly to low open loop gain, the feedback technique is not very useful for RF power amplification at microwave frequencies.

Predistortion

In the predistortion approach [40], [41], [42] nonlinear elements such as diodes and low power FETs or DSP are used to deliberately generate amplitude and phase distortion at the amplifier input varying with input drive level. This controlled inverse distortion, which can be either analogue or digital, is used to compensate for the amplifier's nonlinear transfer characteristic; hence linearisation is obtained. A typical adaptive digital predistortion system is shown in Figure 3.39.

The I-Q output pair are provided by the look up table for each input envelope sample. The I-Q output pair contains the required phase and amplitude correction for compensating the amplifier nonlinearity at the current signal level.

This technique provides considerable efficiency and bandwidth and it also offers the widest flexibility of design and application. The major drawback of this technique is the low speed of the operation and also the fact that the DSP circuitry can consume a lot of power for lower power PA applications.

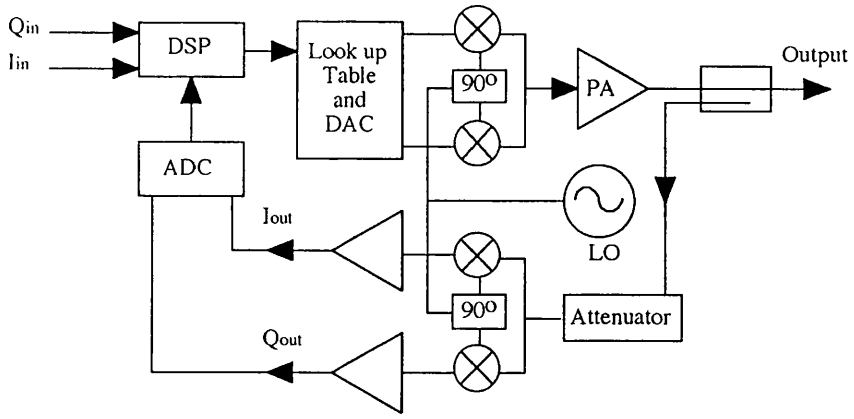

Figure 3.39: Adaptive digital predistortion system.

Balanced Systems

Another very popular system level linearisation technique for power amplifiers is the balanced structure. This technique has already been discussed in detail in Sections 3.5.1 and 3.5.4.

Other Linearisation Techniques

There exist a number of other linearisation technique which we will discuss very briefly in the following.

Polar and Cartesian correction techniques are two forms of indirect feedback strategy [42]. They use the detected or downconverted input and output envelope amplitude and phase responses in order to generate the required error correcting functions. One of the drawbacks of the polar correction method is the fact that phase detection and correction is quite a complicated function to perform. In the Cartesian correction technique since the modulating signal is split into two quadrature channels the tracking of amplitude and phase variations can be performed more easily. Therefore, the resulting I and Q channels can be processed in well-matched paths and the problems of signal processing requirements for magnitude and phase paths present in the polar loop can be avoided. The main drawback associated with the Cartesian correction technique is its limited bandwidth.

Another linearisation technique is the one proposed in [43]. In this technique the level of the 3rd order intermodulation product is shown to be reduced by feeding in the generated 2nd order harmonics at the output of the amplifier to its input. The level of reduction of the 3rd order intermodulation distortion reported by this technique was 16 dB. The drawback with this technique is the fact that the cancellation will only occur at a specific drive level.

3.7.3 Application of Derivative Superposition to Power Amplifiers

The idea of using derivative superposition in power amplifiers was first proposed in [12]. The authors have shown simulated results in which by minimising the g_3 derivative over a wide range of gate bias voltages a low 3rd order distortion for large signals has been achieved at the cost of an increase by a few dBs in the 2nd order distortion. In [12] the load resistance was chosen to be unrealistically small in order to stabilise the shape of the derivatives. This low load resistance caused the gain of the circuit to be very low. High load resistances affected the shape of the derivatives and the derivative superposition principle could no longer be held properly and as a result distortion reduction was reduced significantly. This problem of design of derivative superposition power amplifiers is one which will be addressed in this thesis.

3.8 Discussion and Conclusions

Most of the techniques described in this chapter have serious problems associated with them. Some suffer from frequency dependant distortion [5] (e.g. translinear technique) some are very lossy (e.g. balanced amplifiers) and some can not be used in some specific applications. It has been shown that the derivative superposition technique does not suffer from frequency dependant distortion [5] due to the fact that it is based on common-source FETs. This technique has low losses associated with it due to the fact that it does not use splitters and combiners. Some of the techniques discussed are narrowband whereas the derivative superposition technique is broadband. It has also been shown that the derivative superposition technique can be successfully used in small and medium signal applications, in nonlinear applications (e.g. frequency doublers and triplers) and in power amplifiers. Due to the potential advantages of the derivative superposition technique, this technique has been chosen to be the subject of the work in this thesis.

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Chapter 4

Measurement of Intermodulation Distortion of FETs

4.1 General

In this chapter we will first discuss some of the problems involved in the measurement of intermodulation distortion (IMD) in more detail. These include the problems of residual distortion and use of a high impedance probe to provide a load to a device under test other than 50 Ω. We will then discuss ways of reducing residual distortion and ways of avoiding the use of a high impedance probe by a load resistance configuration which avoids the introduction of associated distortion and noise. Then, we will present a way of improving intermodulation distortion measurement results obtained by on-wafer measurement of IC chip devices. Finally, we will discuss the development of a high frequency distortion measurement set-up for operating frequencies of around 0.5 GHz which uses a rat race coupler.

4.2 Problems in IMD Measurement

4.2.1 Residual Distortion

The TDFD intermodulation distortion measurement set-up previously developed at UCL is shown in Figure 4.1.

The arrangement consists of two signal generators which are fed into a resistive combiner. The two signal generators are set to $f_1 = 20MHz$ and $f_2 = 29.3MHz$. For the above frequencies the products of interest are the second order product, $(f_2 - f_1)$ which is equal to 9.3 MHz and the third order product $(2f_1 - f_2)$ which is 10.7 MHz. The other frequency components are well separated from these

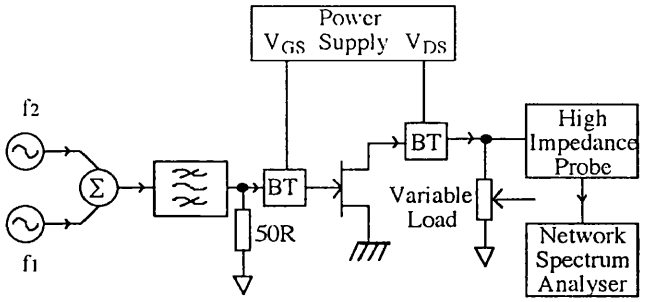

Figure 4.1: TDFD intermodulation distortion measurement set-up.

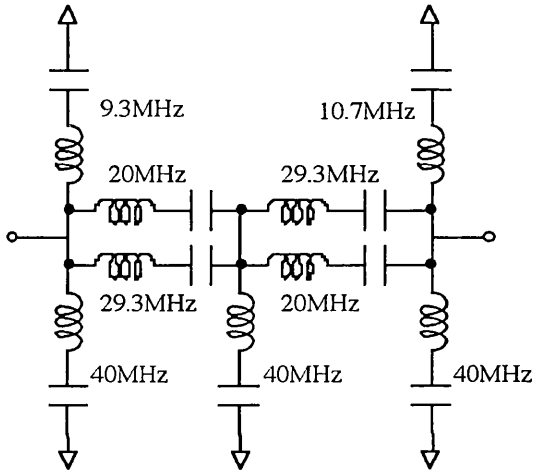

Figure 4.2: Schematic diagram of the scrubbing filter.

frequencies and therefore, are of no importance as far as intermodulation distortion is concerned for this set-up.

The main source of residual distortion in the test set is caused by the interaction between the two signal generators through the resistive combiner. This residual distortion can interfere with the distortion measurement results of the device under test and, therefore, must be removed from the system. A scrubbing filter whose circuit is shown in Figure 4.2 removes these unwanted interferences.

The scrubbing filter was tuned in order to reject the frequency components at 9.3 MHz, 10.7 MHz and 40 MHz, but to allow the frequency components at 20 MHz and 29.3 MHz to pass through. The measured response of the scrubbing filter, using HP 4195A network/spectrum analyser, is shown in Figure 4.3.

The filter design is based on the Foster reactance theorem [1] . In our measurement set-up the filter is inserted between the combiner and the device under test. In some other cases [2] the filter is inserted between the two signal generators and the combiner. A possible problem with this configuration is the impedance

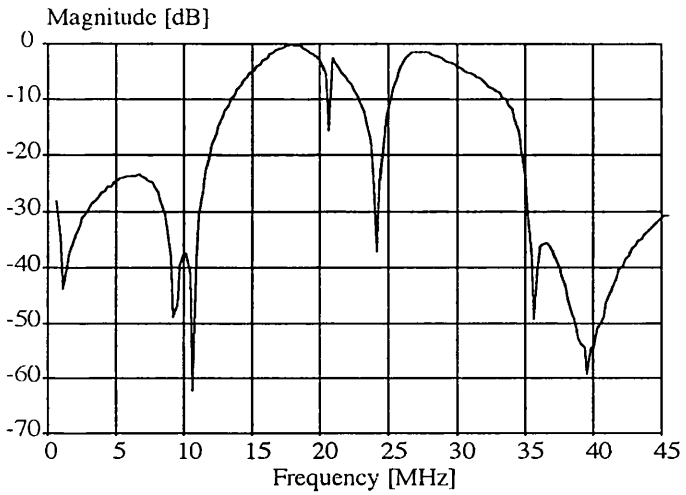

Figure 4.3: Measured response of the scrubbing filter.

instabilities at the input port of the device that may occur.

There are also problems with the noise floor of the spectrum analyser and the distortion at the input of the analyser which must be avoided by ensuring the input signal is high enough to be above the noise floor.

Another kind of residual distortion is that generated within the spectrum analyser. There are various ways of removing this kind of distortion. The most common method is the use of diplexing filters [3], [4] in order to separate the input signals from the distortion products.

4.2.2 High Impedance Probe

Signal measurement of a device with load resistances other than 50 Ω normally requires the use of a high impedance probe. Unfortunately, the high impedance probe usage introduces a 20 dB attenuation to the measurement system. This can give rise to the reduction of the dynamic range of the measurement. This extra 20 dB attenuation will also make the measurement of small signals more difficult; i.e. measurement of the higher order intermodulation distortion products. These problems suggest that a new way of measurement should be introduced for the measurement of signals in systems other than a 50 Ω system. A technique will be suggested later on in Section 4.3.1 in order to overcome the problems associated with the use of a high impedance probe.

4.2.3 RBW Setting Effects of Network/Spectrum Analyser

Since the resolution bandwidth setting of the network/spectrum analyser (HP4195A) affects the settling time and hence, the time a measurement takes to perform, a study was carried out in order to find an optimum value for the resolution bandwidth which gives acceptable noise with the shortest possible time for the measurement. In Figure 4.4(a), (b) and (c) we show the measured intermodulation distortion results for fundamental, 2nd order intermodulation distortion (IMD2) and 3rd order intermodulation distortion (IMD3), respectively, for a range of resolution bandwidth settings.

The curves in Figure 4.4 have been shifted vertically for clarity. It can be seen from the plots in Figure 4.4 that the setting of resolution bandwidth up to 1 kHz has little or no effect on the fundamental and IMD2 results. On the other hand the resolution bandwidth setting has considerable effect on the IMD3 results. It can be seen that a resolution bandwidth of more that 30 Hz can cause fluctuations in the measured 3rd order intermodulation distortion. However, a resolution bandwidth of 100 Hz is perhaps a reasonable compromise between speed and accuracy.

4.3 Ways of Improving IMD Measurement

In the previous section we discussed the problems associated with using a high impedance probe in the distortion measurement set-up. In this section we will look at a configuration for load resistance which avoids the use of a high impedance probe. We will also discuss an improved set-up for on-wafer distortion measurement.

4.3.1 New Load Resistance Configuration

In order to avoid the use of a high impedance probe in the measurement systems other than 50 Ω a new load resistance configuration was developed. This new configuration has also been reported by Parker's group at Macquarie University, Sydney [2]. In this technique, we use the 50 Ω load of the spectrum analyser as part of the actual load. This suggests that there will be two load configurations. One configuration for loads less than 50 Ω and one configuration for loads more than 50 Ω. For loads less than 50 Ω an external load is connected in parallel with the 50 Ω load of the spectrum analyser in order to obtain the desired load. This is shown in Figure 4.5.

As can be seen this is a simple implementation and the external load required to make the desired load can be calculated from the following equation.

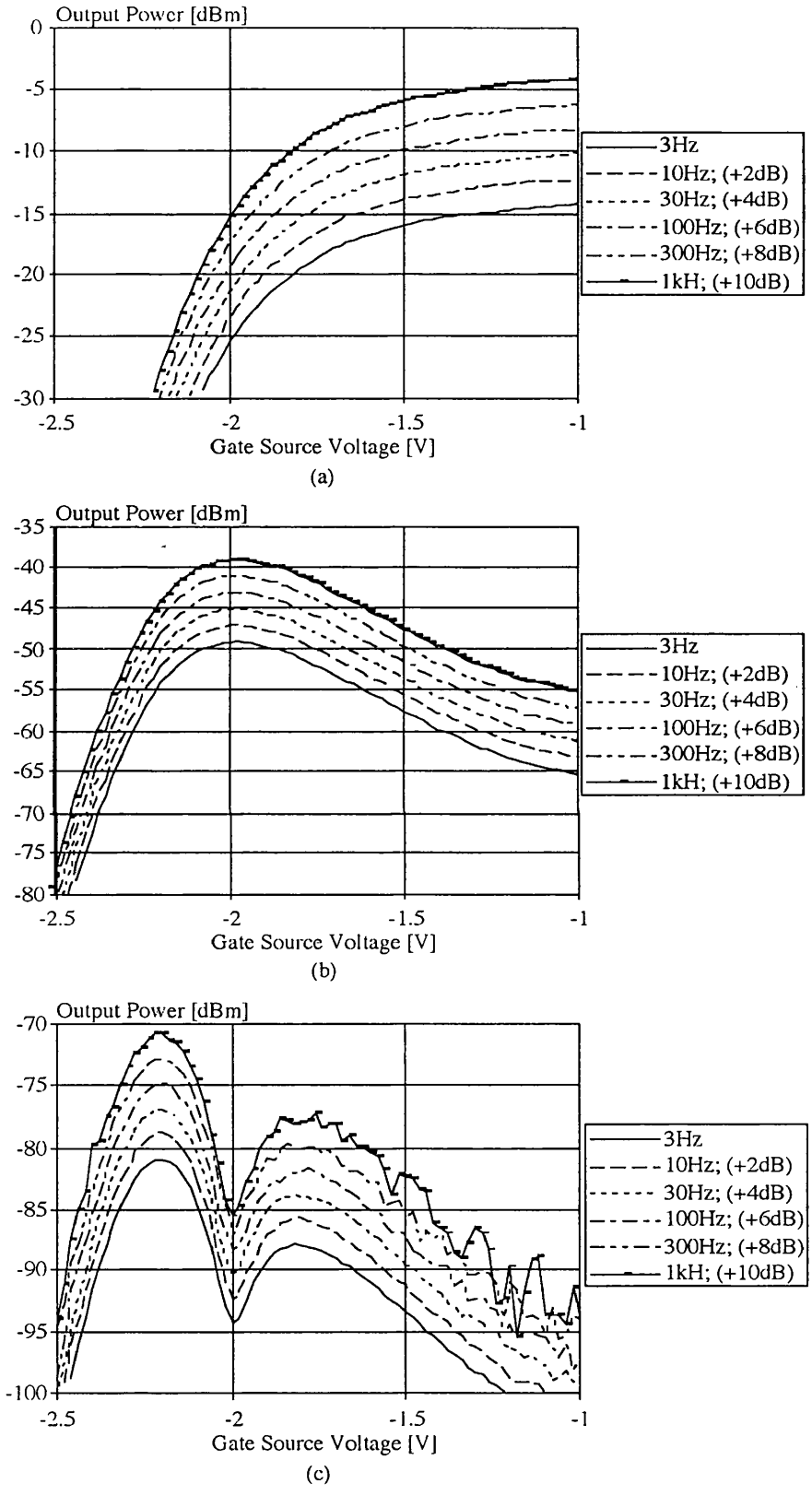

Figure 4.4: The effect of the resolution bandwidth of the network/spectrum analyser on distortion for a GaAs MESFET; (a) Fundamental, (b) IMD2 and (c) IMD3.

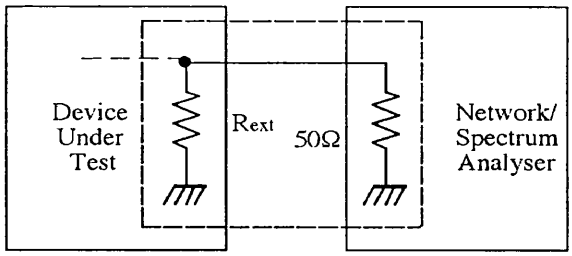

Figure 4.5: Load resistance configuration for desired loads less than 50 Ω.

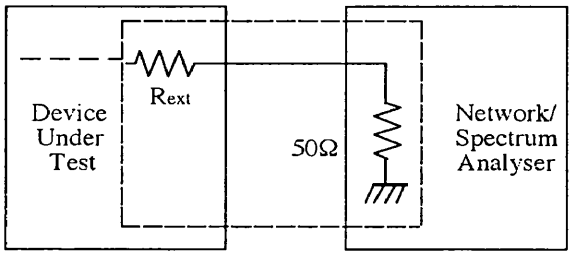

Figure 4.6: Load resistance configuration for desired loads more than 50 Ω.

$$R_{external} = \frac{50 * R_{desired}}{50 - R_{desired}} \tag{4.1}$$

On the other hand for loads more than 50 Ω an external load is connected in series with the 50 Ω load of the spectrum analyser in order to obtain the desired load. This is shown in Figure 4.6.

In this case the external load required to make the desired load can be calculated from the following equation.

$$R_{external} = R_{desired} - 50 \tag{4.2}$$

In the parallel load resistance configuration the spectrum analyser measures the same voltage as that existing across the desired load resistance. Therefore, if the signal is measured in Volts, there is no need for further data manipulation. However, if we are interested in power, the data should be scaled. With the assumption that the external load resistance is purely resistive, the measured data should be scaled by $\frac{50}{R_{Load}}$ to obtain an answer in Watts or a correction factor of $10 * Log(\frac{50}{R_{Load}})$ should be added to obtain an answer in dBm.

In the series resistor case of Figure 4.6, data should always be corrected (i.e. for voltage and power). The measured voltage should be scaled by $\frac{R_{Load}}{50}$ in the linear scale or by adding a value of $10 * Log(\frac{R_{Load}}{50})$ in the logarithmic case.

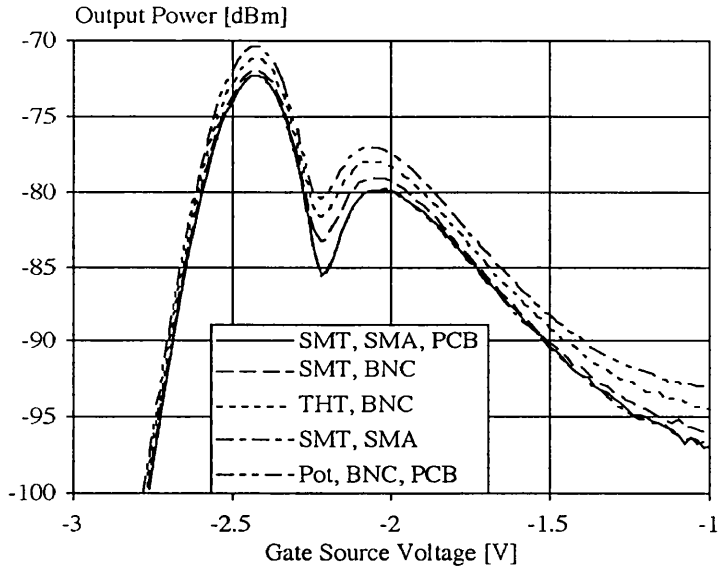

Figure 4.7: Comparison of the measured IMD3 for a CLY5 GaAs MESFET for various load resistance configurations.

4.3.2 Comparison of Various Types of Load Resistance

Different kinds of resistors and connectors used in load resistance configurations discussed previously can provide different results. Various kinds of load resistors including surface mount, through hole and variable resistors were considered. Two kinds of connectors were also studied which were BNC and SMA. The effect of the use of a PCB board in implementing the load resistors were also considered. In Figure 4.7 we show the measured 3rd order intermodulation distortion of a MESFET for various kinds of load resistances.

It can be seen from Figure 4.7 that the best result, i.e. deep noise free null, can be obtained by using surface mount resistors with SMA connectors on a PCB board. Therefore, this configuration was adopted for a range of values and used for all distortion measurements.

4.3.3 Improved On-wafer Distortion Measurement Set-up

In the on-wafer distortion measurements for DC biasing we need to use bias tees. Most of the lower frequency measurements carried out in this thesis are at 20 MHz. The bias tees available are presented in Table 4.1. It can be seen from Table 4.1 that the lower frequency of HP bias tee is 45 MHz and therefore, can not be used directly for the 20 MHz distortion measurements. The problem with the Mini-Circuit bias tee is that it has a high DC resistance associated with it

Table 4.1: Model and specification of the available bias tees.

	HP 11612A	Mini-Circuits ZFBT-4R2G-FT
f_{LC} [MHz]	45	10
f_{HC} [MHz]	26500	4200

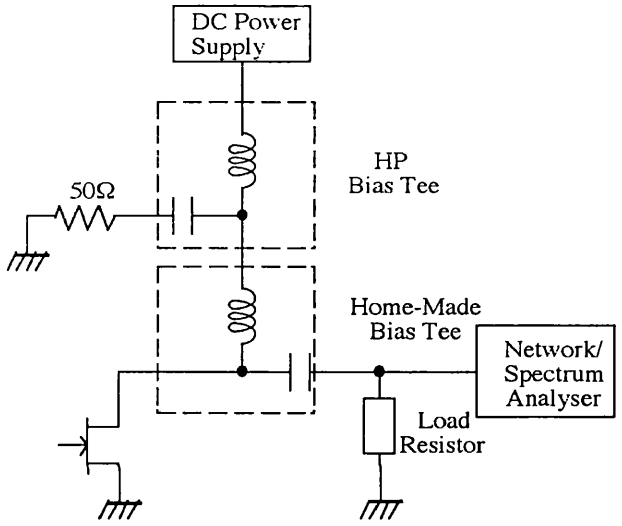

Figure 4.8: Schematic diagram of the improved bias tees arrangement.

(i.e. about 2.5 Ω). It is also desirable to have the bias tees physically as close as possible to the device under test. Therefore, it was decided to make our own bias tees on PCB boards, which have DC resistances of 1 Ω, and connect them in series with the commercial HP 11612A bias tees as shown in Figure 4.8.

In this set-up, at the measurement frequency of interest (i.e. 20 MHz) the device under test sees the load resistance. At self resonance the output of the device is capacitively coupled to the HP bias tee which represents a 50 Ω from 45 MHz to 26.5 GHz. Therefore, the arrangement allows the control of impedance at high frequencies and hence, avoids oscillation problems which leads to more reliable distortion results. Measured on-wafer distortion results with the improved set-up for a MMT F20 GaAs MESFET with two resistor values of 10 Ω and 50 Ω are shown in Figure 4.9. It can be seen from Figure 4.9 that for the two different load resistor values, the improved technique provides very stable responses in each case.

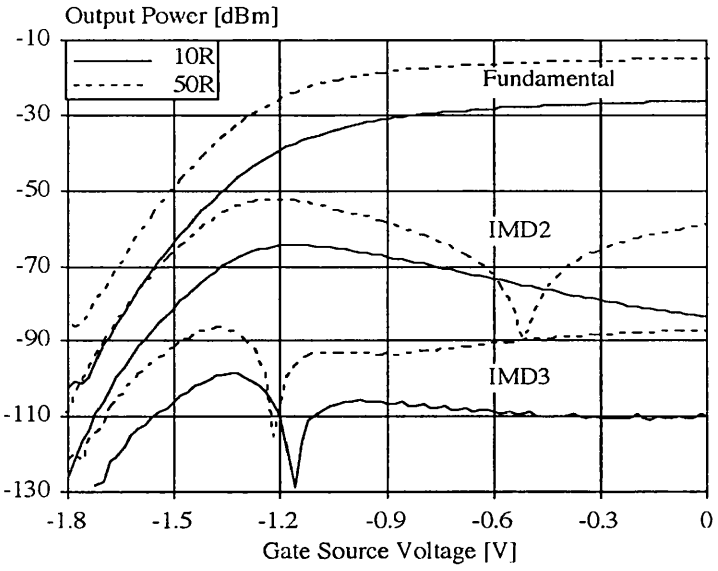

Figure 4.9: Measured on-wafer distortion results with the improved on-wafer measurement test set-up. Device measured is a 6x100 μm F20 GaAs MESFET with a load resistance of 10 Ω and 50 Ω; the input signal level is -15 dBm.

4.4 High Frequency Measurement Set-up

In this section we discuss the development of a high frequency measurement set-up suitable for operation around 0.5 GHz. We first discuss the choice of frequencies for the signal generators and the optimum frequency spacing of the signals. We then, describe the design and response of the rat race coupler which will be used instead of the resistive combiner previously used and then look at the responses of the stub filters required for the elimination of even order harmonics [5].

4.4.1 Schematic Diagram of the Measurement Set-up

The schematic diagram of the high frequency measurement set-up is presented in Figure 4.10. The $\lambda/4$ short circuited stubs at the outputs of the signal generators are used for even harmonic minimisation.

4.4.2 Choice of Signal Generators Frequency and Residual Distortion

In the intermodulation distortion measurements it is vital to have a thorough understanding of the residual distortion levels of the measurement system. This is due to the fact that a high residual distortion level can interfere with the actual

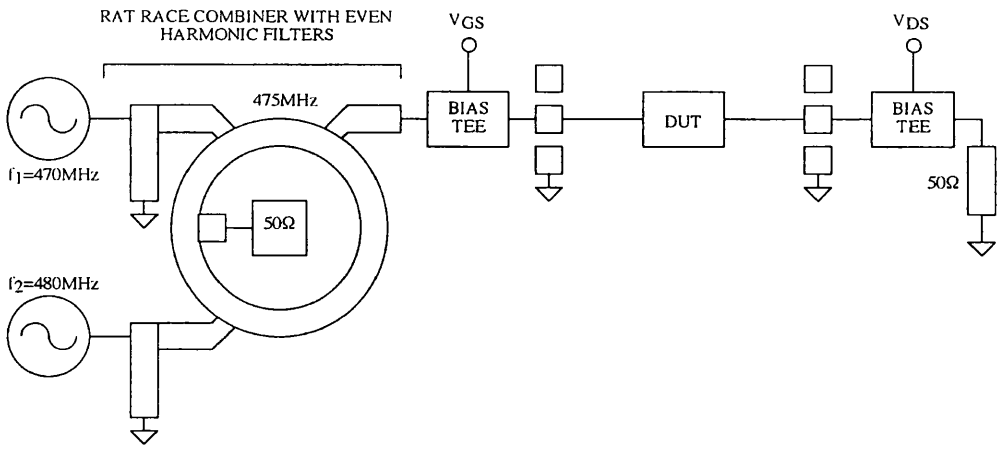

Figure 4.10: Schematic diagram of the high frequency measurement set-up.

intermodulation distortion performance of a device and hence, lead to misleading distortion measurements. Therefore, the first task was to have an almost residual distortion free measurement system. First, a centre frequency of 475 MHz was chosen. This was almost the highest available frequency in the system since the network/spectrum analyser (HP4195A) which was used for distortion measurement had a top frequency of 500 MHz. Several frequencies were studied for the two RF signal generators. The frequency spacing between the two RF signal generators studied were 0.5 MHz, 1 MHz, 2 MHz, 5 MHz and 10 MHz. Various input signal levels for the signal generators ranging from -15 dBm to +15 dBm were used for different attenuation settings of the network/spectrum analyser ranging from 0 dB to 50 dB. The magnitude of the 3rd order intermodulation distortion products for various input power levels and attenuation settings for the rat race were measured. It was concluded that the 10 MHz frequency separation between the two RF signal generators (i.e. $f_1 = 470MHz$ and $f_2 = 480MHz$) provided the best results. This was due to two reasons. First, the level of the 3rd order intermodulation distortion was not increased when the attenuation of the network/spectrum analyser was increased. This suggested that the level of the residual distortion of the system at these frequencies are low enough not to interfere with the measured distortion. It was also observed that the lowest level of the 3rd order intermodulation distortion was obtained with these frequencies.

4.4.3 Rat Race Design and Response

A rat race coupler was to be developed for combining the signals of the two signal generators operating at 470 MHz and 480 MHz required for the TDFD measure-

ment method described in Section 2.4.7. 75 Ω cables were used to implement the $\lambda/4$ and $3\lambda/4$ sections comprising the rat race coupler. The cable lengths were then calculated to give a good transmission at frequencies of interest. It was concluded that for the best matching for all ports the lower frequency (f_L) and higher frequency (f_H) should be 420 MHz and 485 MHz, respectively, which lead to 2nd harmonic of the f_L ($2f_L$) and 2nd harmonic of the f_H ($2f_H$) of 840 MHz and 970 MHz, respectively. The measured transmission and isolation between the ports of interest of the rat race are tabulated in Table 4.2.

Table 4.2: Measured transmission and isolation response of the rat race.

	Transmission [dB]		Isolation [dB]
	Port 1 to 2	Port 3 to 2	Port 1 to 3
f_L	-3.22	-3.80	-27.7
f_H	-3.49	-4.29	-30.05
$2f_L$	-14.99	-9.80	-17.0
$2f_H$	-9.30	-9.70	-15.0

It can be seen from Table 4.2 that respectable transmission and isolation are obtained from the rat race at the frequencies of interest.

4.4.4 Stub Filters Design and Response

In order to eliminate the unwanted even order harmonics two short circuited $\lambda/4$ stubs made from the same 75 Ω cables used in the rat race coupler design were designed for the intended frequencies of the signal generators and were employed at the outputs of the signal generators. The responses of the short circuited stubs at 470 MHz and 480 MHz are presented in Figure 4.11(a) and (b), respectively.

It can be seen from Figure 4.11(a) and (b) that respectable transmissions and good return losses are obtained at the frequencies of interest.

4.5 Summary

The interaction of the output signals of the signal generators give rise to residual distortion which can interfere with distortion measurement results of a device under test. This can be reduced considerably by a scrubbing filter for low frequency

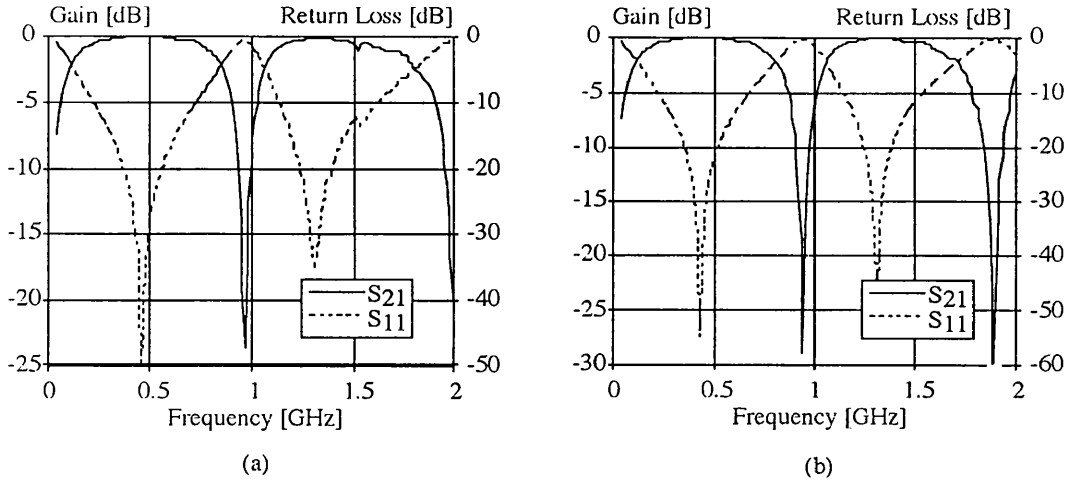

Figure 4.11: Measured responses of the short circuited stubs; (a) at 470 MHz and (b) at 480 MHz.

test signals of 20 MHz and 29.3 MHz. The resolution bandwidth setting of up to 100 Hz for the spectrum analyser gives acceptable intermodulation distortion measurement results. Use of a high impedance probe in the distortion measurement set-up introduces a 20 dB attenuation. This reduces the dynamic range of the measurement. A new load resistance configuration has been developed to overcome this problem. The on-wafer intermodulation distortion measurement set-up can be improved by introducing secondary sets of bias tees. A high frequency measurement set-up employing a rat race coupler and short circuited stubs for operating frequencies of around 0.5 GHz has also been developed.

Having explored new ways of obtaining more reliable results using the TDFD method, in Chapter 5 we present measured distortion results for various FETs using this technique.

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[2] Guoli Qu, "Characterising Intermodulation in High Electron Mobility Transistors", Ph.D. Thesis, 1998.

[3] S A Maas, A Crosmun, "Modelling the Gate I/V Characteristic of a GaAs MESFET for Volterra-Series Analysis", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 37, No. 7, July 1989.

[4] J C Pedro and J Perez, "Accurate Simulation of GaAs MESFET's Intermodulation Distortion Using a New Drain-Source Current Model," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 42, No. 1, pp. 25-33, January 1994.

[5] K C Gupta, R Garg, I Bahl, P Bhartia, "Microstrip Lines and Slotlines", Second edition, 1986, Artech House, ISBN 0-89006-766-X.

Chapter 5

Study of the Nonlinear Behaviour of Typical FETs

5.1 General

In Chapter 4 we reported the development of improved TDFD measurement set-ups. In the work carried out in this chapter we will use this technique in order to investigate the behaviour of some FETs in detail.

In this chapter we will first investigate some of the factors which influence the intermodulation distortion performance of a FET using SPICE. These factors include the gate and drain bias points, voltage gain and the effect of input power levels. Then, detailed measured intermodulation distortion performances of some sample FETs including MESFETs, HEMTs, MOSFETs and Si-JFETs will be compared and discussed. Finally, we will show that by using a nonlinear mapping technique with a suitable graphical interpretation, it is sometimes possible to identify low distortion regions of operation whilst still giving small signal matching.

The intermodulation distortion measurements will be based on the TDFD method described in Section 2.4.7.

5.2 Observations Using SPICE

Simulations were carried out using SPICE version 3f4 in order to study the distortion behaviour of a FET with various parameters such as bias point, voltage gain and input power levels. All the SPICE simulations are carried out using Parker Skellern model described in Section 2.5.7.

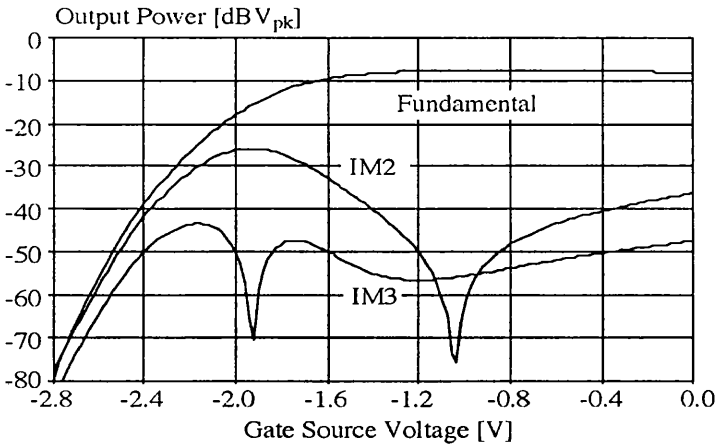


Figure 5.1: Simulated bias dependent intermodulation distortion for a CLY5 GaAs MESFET; $V_{DS} = 2V$ and $R_{Load} = 10\Omega$.

5.2.1 Effect of Gate Bias on Distortion

One of the ways of considering the nonlinearity of a FET is to plot the small signal distortion against the DC gate bias for a fixed drain bias and load resistance. For a drain bias of 2 V and load resistance of 10 Ω bias dependent distortion of a CLY5 GaAs MESFET was simulated. The result is shown in Figure 5.1.

It can be seen from Figure 5.1 that this device shows a peak in the 2nd order distortion near the pinch-off region. There is a null in the 3rd order distortion associated with this peak (zero gradient). Due to this null in the 3rd order distortion two peaks in the 3rd order distortion are also obtained [1]. It can also be seen that the gain increases above pinch-off. This causes a decrease in the 2nd order nonlinearity and a valley in the 3rd order distortion.

5.2.2 Effect of Drain Bias on Distortion

Another important factor which influences the distortion behaviour of a FET is the drain bias. Figure 5.2 shows the small signal distortion against DC gate bias for drain-source voltage values of 2 V and 5 V.

It can be seen from Figure 5.2 that increasing the drain bias from 2 V to 5 V causes a reduction in the 3rd order distortion by more than 10 dB for gate bias values higher than -0.5 V (class A operation mode) without any significant change in gain. The increase in drain bias also suppresses the 2nd order distortion for gate bias values higher than -0.5 V.

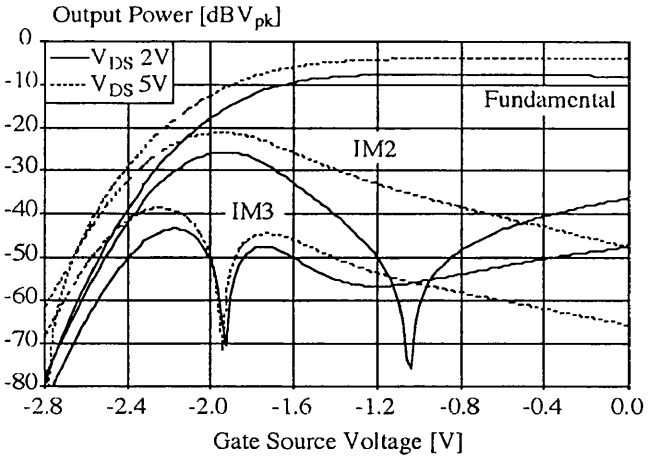


Figure 5.2: Simulated observation of the effect of drain bias on distortion. The device is a CLY5 GaAs MESFET with a load resistance of 10 Ω.

5.2.3 Effect of Load Resistance on Distortion

In Figure 5.3 we show the small signal distortion of a MESFET against the DC gate bias for 4 different load resistance values.

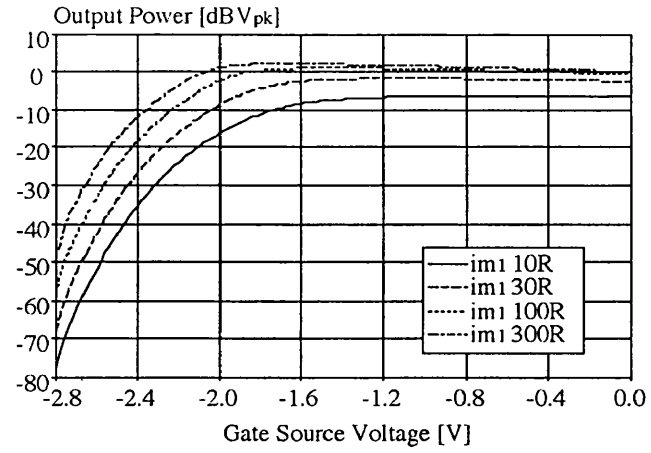
It can be seen from Figure 5.3 that increase of the load resistance moves the nulls in 2nd order and 3rd order distortion to a more negative gate bias. This null movement is more pronounced in the case of the 2nd order distortion. It can also be observed from Figure 5.3 that an increase in the load resistance value causes an increase in the distortion as well as an increase in gain.

5.2.4 Effect of Input Signal Amplitude on Distortion

The small signal distortion of a CLY5 GaAs MESFET was simulated against DC gate bias for different input signal amplitudes and the results are shown in Figure 5.4.

It can be seen from Figure 5.4 that for input power levels greater than -10 dBm the characteristic changes dramatically. This is referred to as the distortion saturation effect. This must be avoided since it will give incorrect results when small signal distortion products are required.

Having investigated some of the factors that influence the intermodulation distortion of a FET by simulation, we now present measured intermodulation distortion results for a number of FETs.



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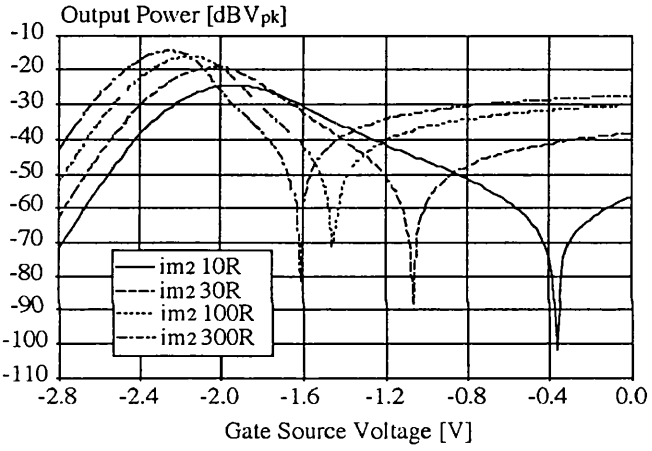

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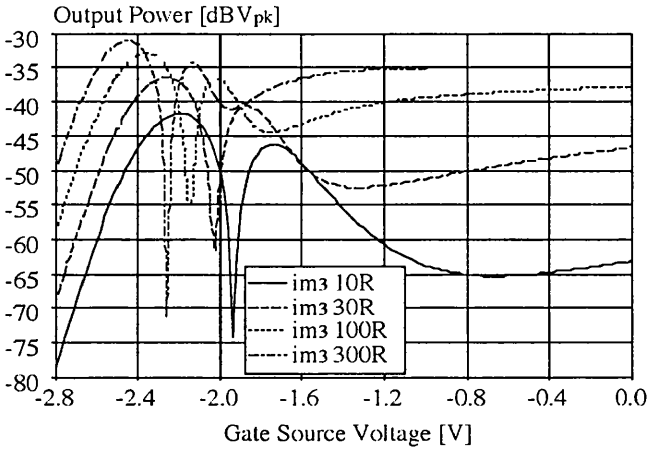
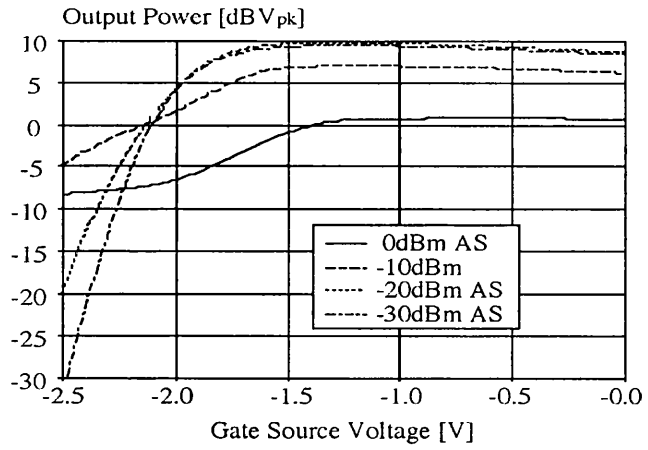


(c)

Figure 5.3: Simulated observation of load resistance on distortion; $V_{DS} = 3V$; (a) Fundamental, (b) IMD2 and (c) IMD3.



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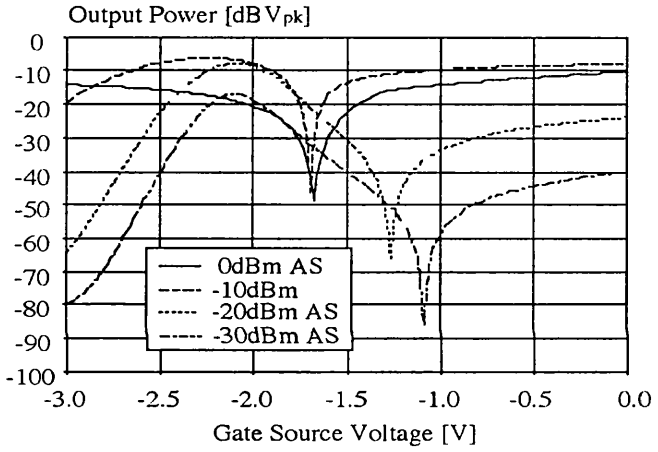

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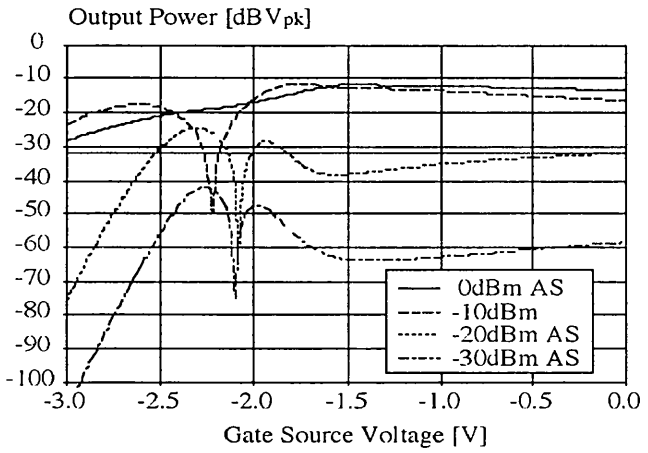


(c)

Figure 5.4: Simulated observation of input power levels on distortion for a CLY5 GaAs MESFET; AS indicates amplitude shifting. $V_{DS} = 3V$ and $R_{Load} = 50\Omega$; (a) Fundamental, (b) IMD2 and (c) IMD3.

5.3 CLY5 GaAs MESFET Measurements

There has been a lot of published work on intermodulation distortion in regard to the methods of characterisation such as [2] or model validation such as [3]. Such papers are generally restricted to one or two devices at either one operating point or one load impedance. In this section we will present some comprehensive measured performance data for a CLY5 GaAs MESFET device. Then, we will present measured intermodulation distortion performances for a number of other devices.

We will first determine the safe operating area for a CLY5 GaAs MESFET device. Then, we will calculate the transconductance, g_m, and output conductance, g_{ds}, for this device by carrying out measurements for two load resistances. Next we will consider the distortion saturation effect and determine the optimum input power level. After this we will present the measured contour plots of distortion against bias and load resistance. Finally, by carrying out DC measurements we will extract a Parker Skellern model for the device.

5.3.1 Characterisation and Measurement

In order not to exceed the allowed limits of the device its maximum power characteristics were considered. It was concluded that sweeping gate-source voltage from -3 V to -1 V with drain-source voltage ranging from 0 to 3 V will ensure that the device is in its safe operating area. These values take into account the heat sink uncertainties.

In order to obtain the transconductance, g_m, and output conductance of the device, g_{ds}, intermodulation distortion measurements were carried out for two load resistor values, $R_1 = 5.7\Omega$ and $R_2 = 50\Omega$. Using the following formulas and the two resistor values, g_m and g_{ds} values were calculated.

$$g_m = g_{R1} \times (\frac{1}{R_1} - \frac{1}{R_2})/(1 - \frac{g_{R1}}{g_{R2}}) \tag{5.1}$$

$$g_{ds} = (g_m - \frac{g_{R2}}{50})/g_{R2} \tag{5.2}$$

where g_{R1} and g_{R2} are the transconductance terms of the resistors R_1 and R_2, respectively. The g_m and g_{ds} plots are presented in Figure 5.5.

It can be seen from Figure 5.5 that the g_m of the CLY5 is about 0.375 S in the saturated region at $V_{DS} = 3V$. It can be seen that the g_{ds} of this device, is about 0.0325 S in the saturated region at $V_{DS} = 3V$. Since $g_{ds} = 1/R_{ds}$, therefore, for maximum power transfer (i.e. $R_{Load} = R_{ds}$) the load must be 30.77 Ω.

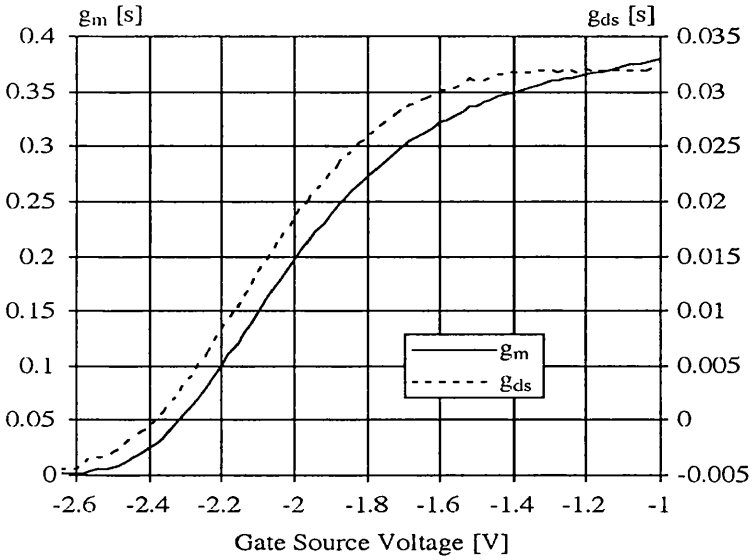


Figure 5.5: The measured plot of g_m and g_{ds} against gate-source voltage for a CLY5 GaAs MESFET; $V_{DS} = 3V$ and input power level is -10 dBm.

Another important issue which must be considered in distortion measurement is the distortion saturation effect which was explained in Section 2.3.1.2. This phenomena occurs for high input power levels. A comparison of the effect of three levels of input power on the fundamental amplitude, and the 2nd and 3rd order intermodulation distortion products are shown in Figure 5.6 and Figure 5.7, respectively.

It can be seen from Figure 5.6 and Figure 5.7 that for input power levels larger than -10 dBm the fundamental experiences some changes which in turn gives rise to movement of the levels of IMD2 and IMD3 products.

If the level of the input power level is too low, there will be problems associated with noise. In Figure 5.8 we show the plot for two resistor values with various signal levels.

It can be seen that the signal level of -5 dBm suffers from distortion saturation and the -20 dBm and -15 dBm have problems related to noise. The -10 dBm input signal level is high enough to provide a noise free output and low enough so that it would not cause distortion saturation problems. Therefore, the measurements for this device should be carried out with an input signal level of -10 dBm.

Having considered some of the fundamental issues involved in distortion measurement we are now able to investigate the measured behaviour of the intermodulation distortion performance of a CLY5 GaAs MESFET with gate and drain bias and also load resistance.

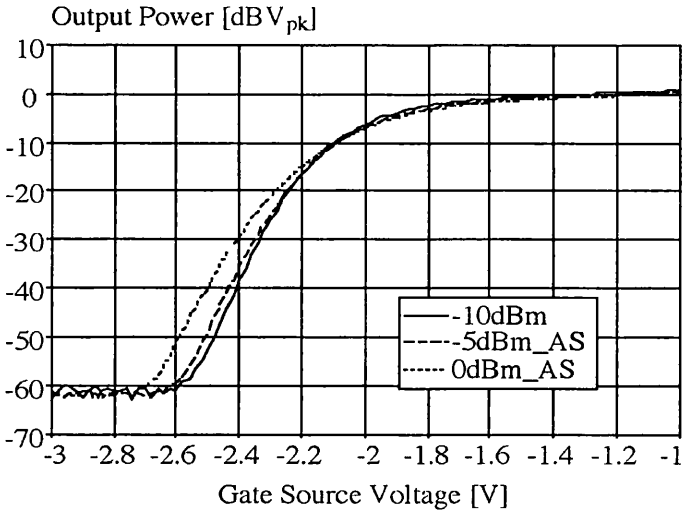


Figure 5.6: Measured fundamental saturation effect for a CLY5 GaAs MESFET; $V_{DS} = 3V$ and $R_{Load} = 50\Omega$. Note that amplitude shifting (AS) has been carried out.

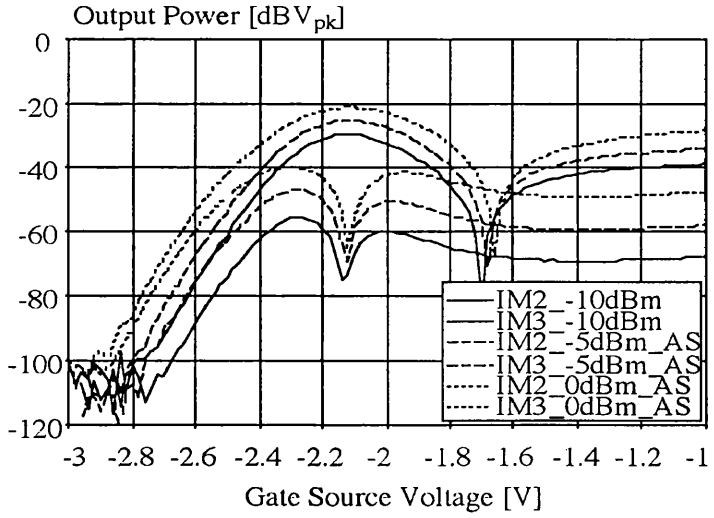


Figure 5.7: Measured 2nd and 3rd order intermodulation distortion saturation effect on a CLY5 GaAs MESFET; $V_{DS} = 3V$ and R_{Load}=50Ω. Note that amplitude shifting (AS) has been carried out.

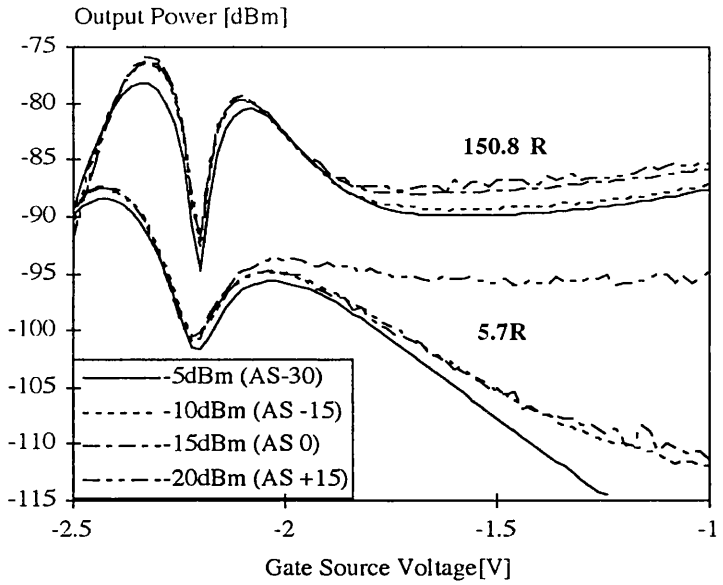


Figure 5.8: Measured IMD3 as a function of gate source voltage for various input power levels for two load resistance values. AS indicates amplitude shifting.

First we will look at the effect of load resistance and gate bias on distortion for fixed values of drain bias. As described previously in this section the R_{ds} of this device is about 30.77 Ω for $V_{DS} = 3V$. Therefore, load resistor values should be chosen to cover a range extending above and below this value. This suggested that a sensible range would be the load resistor values ranging from 5.7 Ω to 150.8 Ω. Figure 5.9, Figure 5.10 and Figure 5.11 show contour plots of distortion against load resistance and gate bias for fundamental, 2nd order intermodulation distortion and 3rd order intermodulation distortion, respectively. Figure 5.9 shows that maximum power gain occurs for load resistance value of about 32 Ω. Figure 5.10 and Figure 5.11 show that increasing load resistance moves the notches in IMD2 and IMD3 to a more negative V_{GS}. It can also be noted that the IMD2 notch movement with load resistance is more than the IMD3 notch movement as found previously in the simulations in Section 5.2.3. It can also be concluded that increasing load resistance, i.e. increasing voltage gain, generally increases the levels of 2nd and 3rd order intermodulation distortion.

Next we will look at the effect of gate and drain bias on distortion for fixed values of load resistances. This effect is shown for two load resistance values in Figure 5.12, Figure 5.13 and Figure 5.14 for fundamental, IMD2 and IMD3, respectively.

It can be seen from Figure 5.12 that the gain is increased for higher values of gate bias, as expected. The gain is also generally increased for higher values of

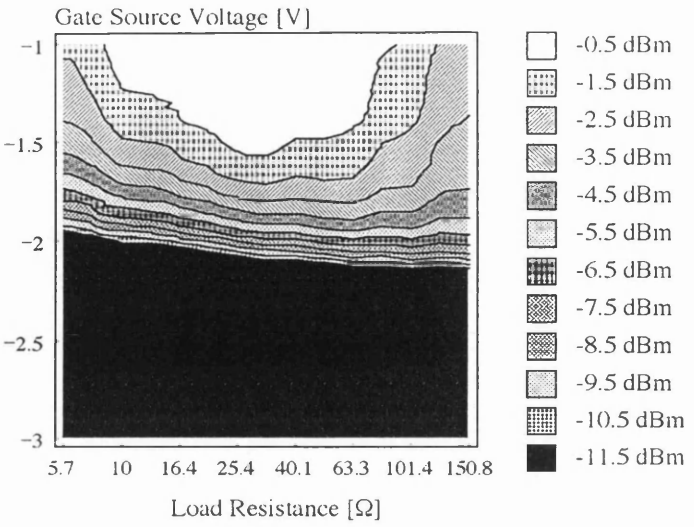


Figure 5.9: Measured contour plot of power gain versus load resistance and gate source voltage; $V_{DS} = 3V$ and input power level is -10 dBm. The device is a CLY5 GaAs MESFET.

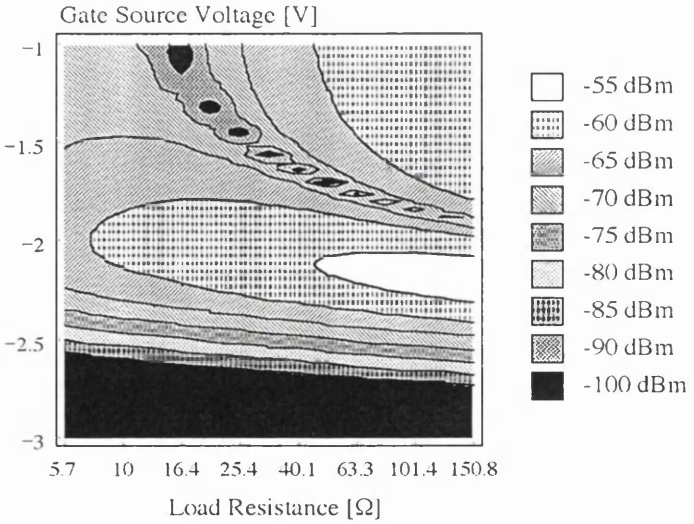


Figure 5.10: Measured contour plot of 2nd order intermodulation distortion versus load resistance and gate-source voltage; $V_{DS} = 3V$ and input power level is -10 dBm. The device is a CLY5 GaAs MESFET.

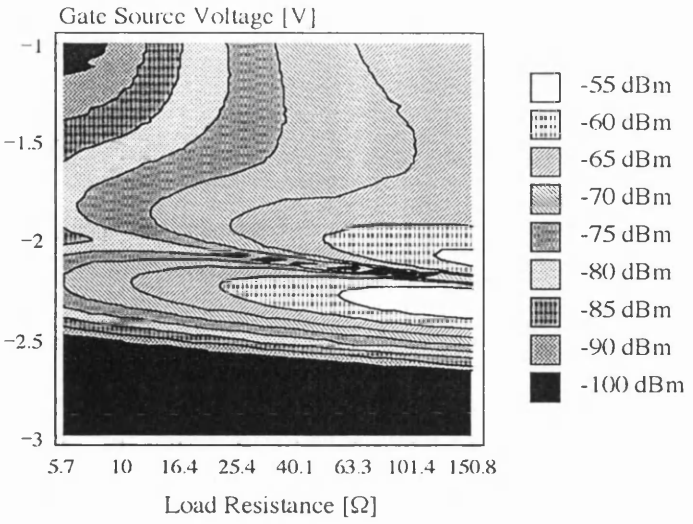


Figure 5.11: Measured contour plots of 3rd order intermodulation distortion versus load resistance and gate-source voltage.; $V_{DS} = 3V$ and input power level is -10 dBm. The device is a CLY5 GaAs MESFET.

drain bias. This is due to the fact that g_{ds} decreases with increasing drain bias. Figure 5.13 and Figure 5.14 show that the IMD2 null is suppressed and the IMD3 level is decreased for higher values of drain bias. It can also be seen that the improvement is greater for the higher load resistance value.

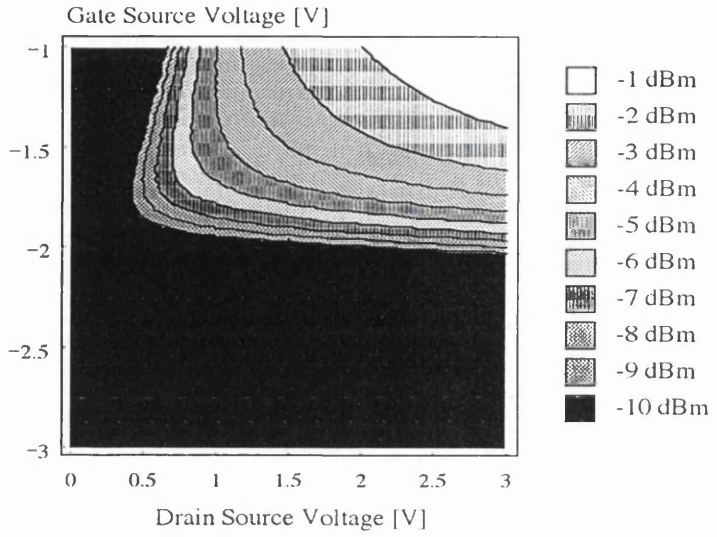
5.3.2 DC Measurements and Modelling

DC measurements were also carried out for this device in order to extract a model. FET FIT 7.4 [4] was used to extract the fit of the Parker Skellern model to the measurement data. The fit of the DC data to the model is shown in Figure 5.15. The model obtained can be used in SPICE simulations.

Having studied the behaviour of a MESFET we will next try to explore the distortion behaviour of various types of FETs with regard to the factors which influence distortion.

5.4 Measured Comparison of Some Devices

As described earlier in Section 5.2, some of the factors that influence distortion in a FET are gate and drain bias, voltage gain and input power levels. In this section we will first show the effect of gate bias for different types of FETs including a GaAs MESFET, a GaAs HEMT, a Si-JFET and a MOSFET. The effect of



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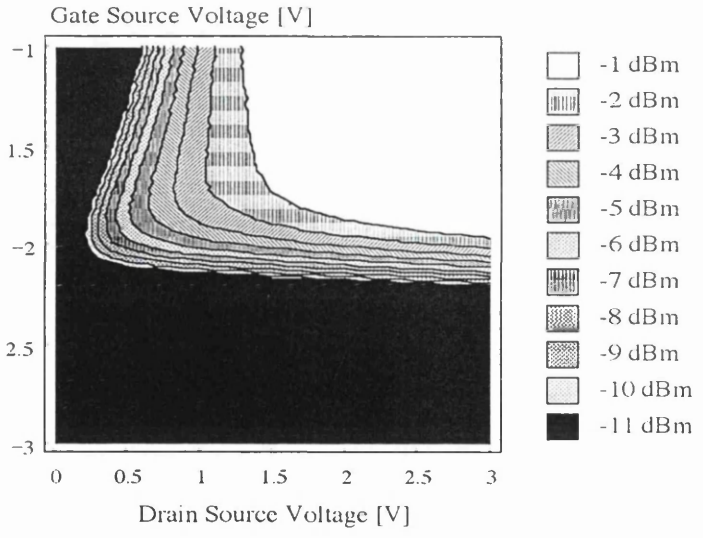
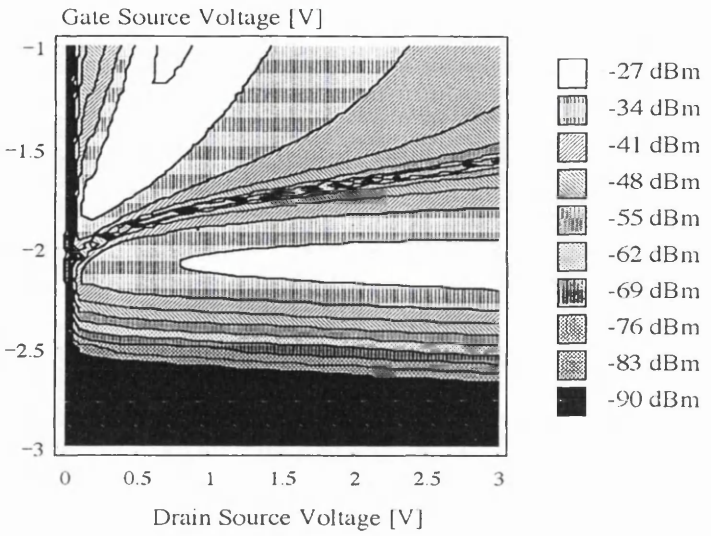


(b)

Figure 5.12: Measured fundamental versus gate-source voltage and drain bias; input signal level is -10 dBm. (a) $R_{Load} = 32.6\Omega$ and (b) $R_{Load} = 150.8\Omega$. The device is a CLY5 GaAs MESFET.



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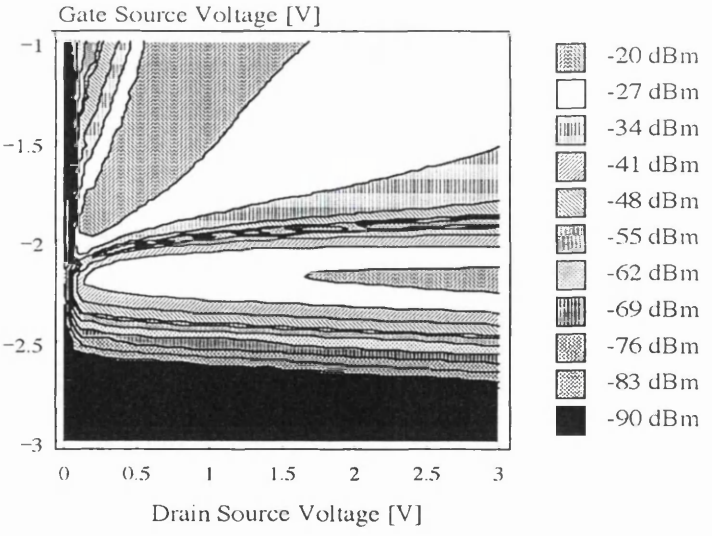
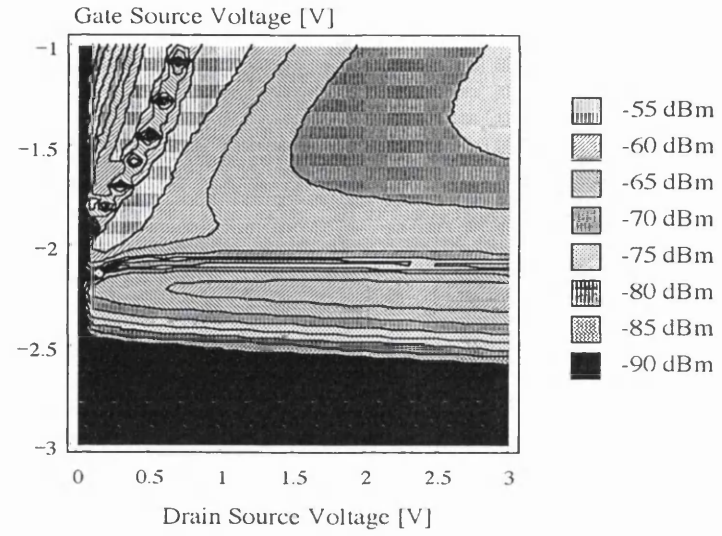


(b)

Figure 5.13: Measured IMD2 versus gate-source voltage and drain bias; input signal level is -10 dBm. (a) $R_{Load} = 32.6\Omega$ and (b) $R_{Load} = 150.8\Omega$. The device is a CLY5 GaAs MESFET.



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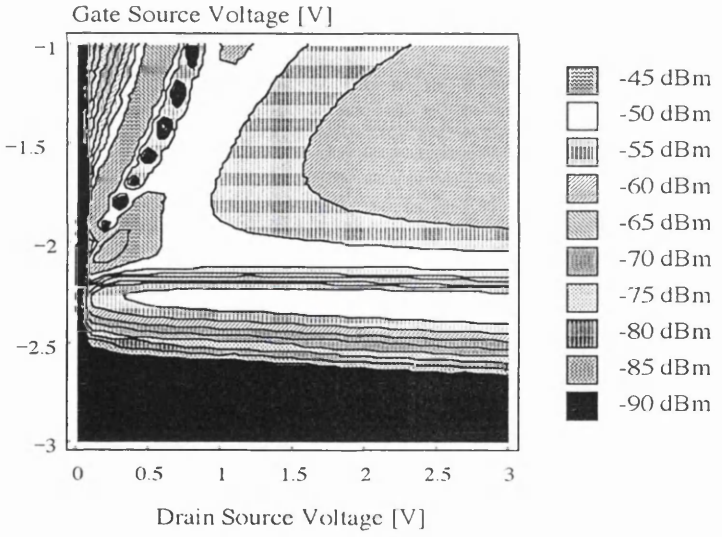

(b)

Figure 5.14: Measured IMD3 versus gate-source voltage and drain bias; input power level is -10 dBm. (a) $R_{Load} = 32.6\Omega$ and (b) $R_{Load} = 150.8\Omega$. The device is a CLY5 GaAs MESFET.

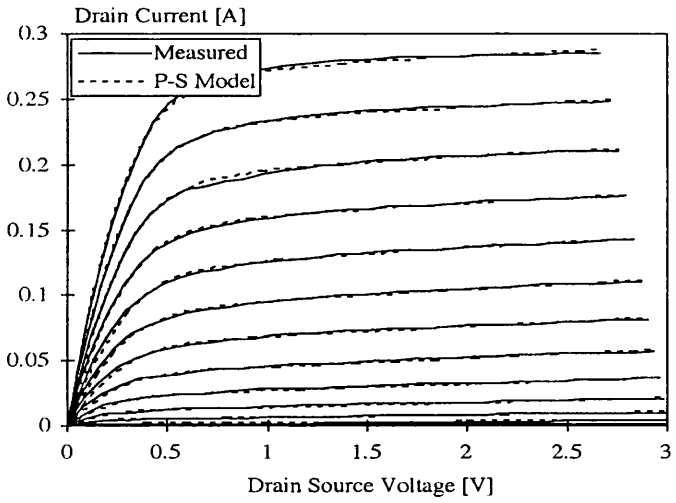

Figure 5.15: DC fit of the Parker Skellern model to measured CLY5 device. Gate bias is swept from -3 V to -1 V in 0.1 V steps.

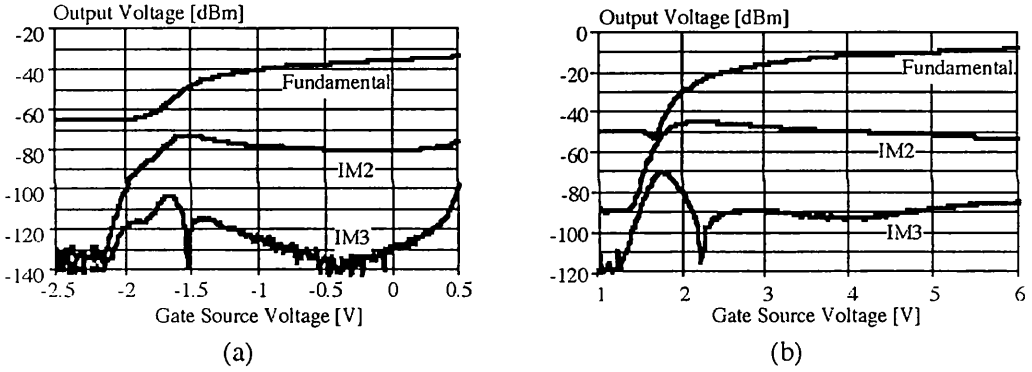

Figure 5.16: Measured bias dependent distortion for (a) a BF244 Si JFET and (b) a MC14007 Si MOSFET.

load resistance i.e. voltage gain for the Si-JFET, MESFET and HEMT will be determined. The effect of drain bias for a MESFET is studied. Finally, the effect of sample to sample variation for a MESFET is considered.

In Figure 5.16 and Figure 5.17 we present plots of the measured small signal distortion with respect to DC gate bias for a fixed load resistance and drain bias for a Si n-JFET and a n-MOSFET and for a GaAs MESFET and an AlGaAs/InGaAs pseudomorphic HEMT, respectively.

These devices despite having widely varying materials, geometry and physical structures, have a number of features in common. All four devices show a distinct peak in 2nd order distortion near pinch-off. As mentioned previously, associated with this peak in the 2nd order distortion there are a pair of peaks in the 3rd

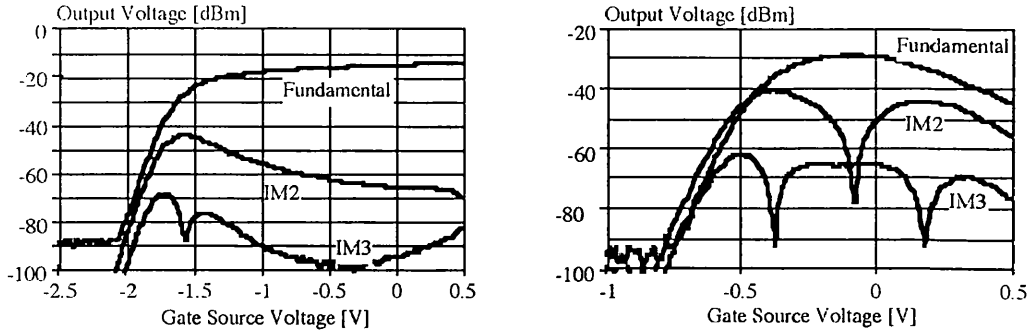

Figure 5.17: Measured bias dependent distortion for (a) a MGF1400 GaAs MESFET and (b) a NE33284 AlGaAs/InGaAs PM HEMT.

order distortion separated by a null. The null is associated with a sign change of the second derivative of the transconductance as disused in Section 5.2.1. It can be seen from Figure 5.16 and Figure 5.17 that for the JFET, MOSFET and MESFET, the gain rises more gently above the pinch-off. This is associated with a fall in the 2nd order nonlinearity and a gentle valley in the 3rd order nonlinearity. The HEMT has a more complex behaviour. It can be seen that the gain falls with high gate bias producing extra nulls in the 2nd and 3rd order distortion. This falling of the gain in a HEMT is due to the parasitic MESFET effect taking place, as discussed in Section 3.4.2.1.

Next, we compare the behaviour of these devices with respect to the effect of change in load resistance i.e. voltage gain. In Figure 5.18 and Figure 5.19 we show the small signal intermodulation distortion versus DC gate bias for a MESFET and a HEMT for different load resistance values, respectively.

Figure 5.18 shows that the 2nd order distortion is specially sensitive to load resistance in the MESFET. There are no notches for low load resistance but for high load resistance, a notch appears at high gate bias and moves rapidly towards pinch-off as the load resistance is increased further. However, for the HEMT case shown in Figure 5.19, the notches in IMD2 and IMD3 move only modestly with increasing load resistance.

In Figure 5.20 we compare the sensitivity of input referred distortion with voltage gain for a MESFET, JFET and a HEMT.

The reason for choosing input referred distortion is that its value will be constant if the nonlinearity is independent of voltage gain. It can be seen from Figure 5.20 that for all devices, the distortion varies with voltage gain. For the HEMT, with voltage gain of 8 dB or less the 3rd order distortion is constant. Whereas for

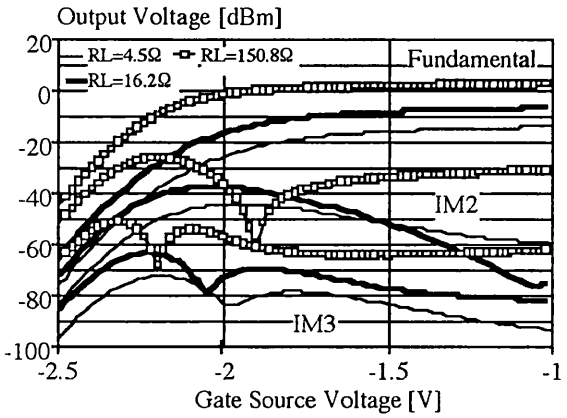

Figure 5.18: Measured bias dependent intermodulation distortion for a CLY5 GaAs MESFET for various load resistance values; input signal level is -17 dBm.

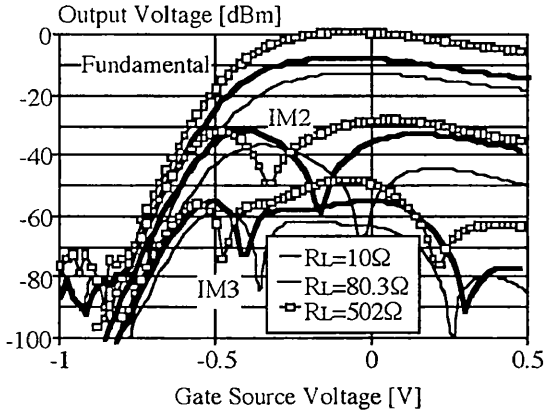

Figure 5.19: Measured bias dependent intermodulation distortion for a NE33284A 0.2 μm AlGaAs/InGaAs PM HEMT for various load resistance values; input signal level is -17 dBm.

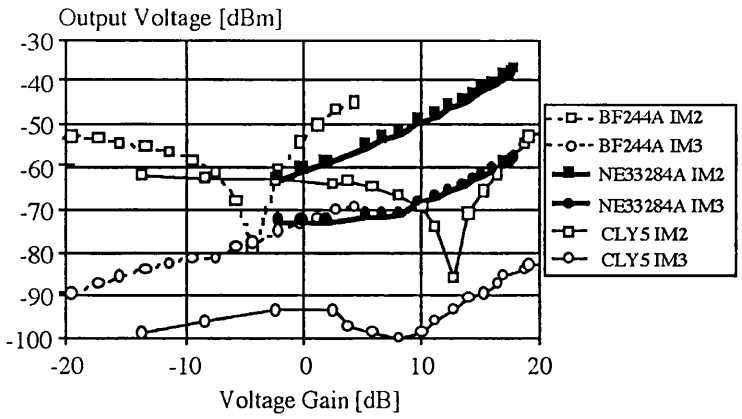

Figure 5.20: Effect of voltage gain on the measured intermodulation distortion for a CLY5 GaAs MESFET biased at $V_{GS} = -1V$ and $V_{DS} = 3V$ with input signal level of -17 dBm; a BF244A Si JFET biased at $V_{GS} = 0V$ and $V_{DS} = 2V$ with input signal level of -12.5 dBm and a NE33284A 0.2 μm AlGaAs/InGaAs PM HEMT biased at $V_{GS} = 0V$ and $V_{DS} = 1.5V$ with input signal level of -17.5 dBm.

the MESFET 3rd order distortion can either rise or fall with voltage gains of 0 dB or higher. For small signal output matching, the MESFET and the HEMT would have voltage gains of 14 dB and 16.5 dB, respectively, for the given quiescent points.

In Figure 5.21 the distortion of the MESFET is shown plotted against load resistance rather than voltage gain.

It can be seen from Figure 5.21 that there is a high level of 3rd order distortion when the output is matched (e.g. case of a low noise amplifier) which in this device occurs at load resistance value of about 30 Ω. On the other hand the distortion is lower for lower load resistance values (e.g. a power amplifier deliberately mismatched to obtain maximum possible output power).

The measured distortion of a MESFET versus DC gate bias for 2 different values of drain bias ($V_{DS} = 2V$ and $V_{DS} = 6V$), with load resistances of 10 Ω and 50 Ω are shown in Figure 5.22 and Figure 5.23, respectively.

It can be seen from Figure 5.22 and Figure 5.23 that by changing the drain bias from 2 V to 6 V, it is possible to reduce the 3rd order intermodulation distortion of a MESFET by about 8-10 dB without significantly changing the gain. The improvement appears greater for higher load resistance. The increase in drain bias also tends to suppress the occurrence of 2nd order distortion nulls. Pinch-off modulation causes the notch in the 3rd order distortion near pinch-off to move to a lower gate bias.

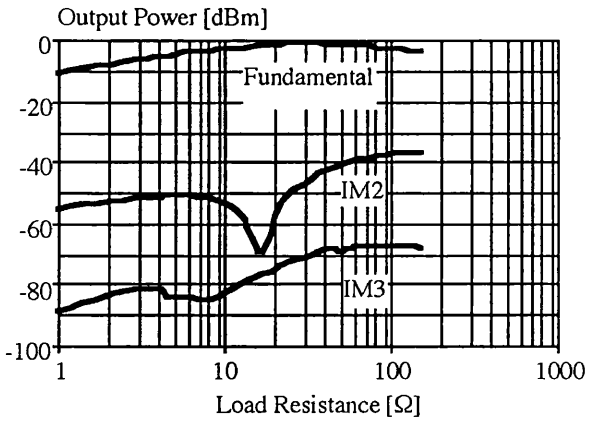

Figure 5.21: Effect of load resistance on the measured intermodulation distortion for a CLY5 GaAs MESFET biased at $V_{GS} = -1V$ and $V_{DS} = 3V$ with input signal level of -17.5 dBm.

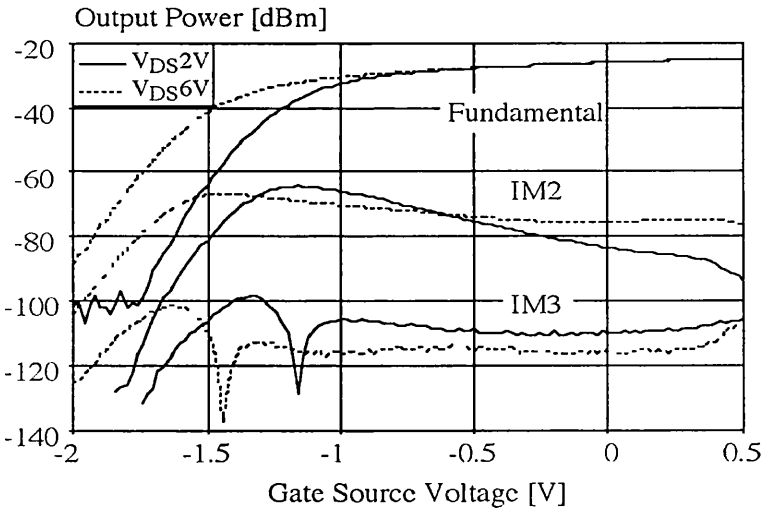

Figure 5.22: Effect of drain bias on measured bias dependent distortion of a MMT F20 6x100 μm MESFET for $V_{DS} = 2V$ and $V_{DS} = 6V$ with load resistance of 10 Ω. Input signal level is -15 dBm.

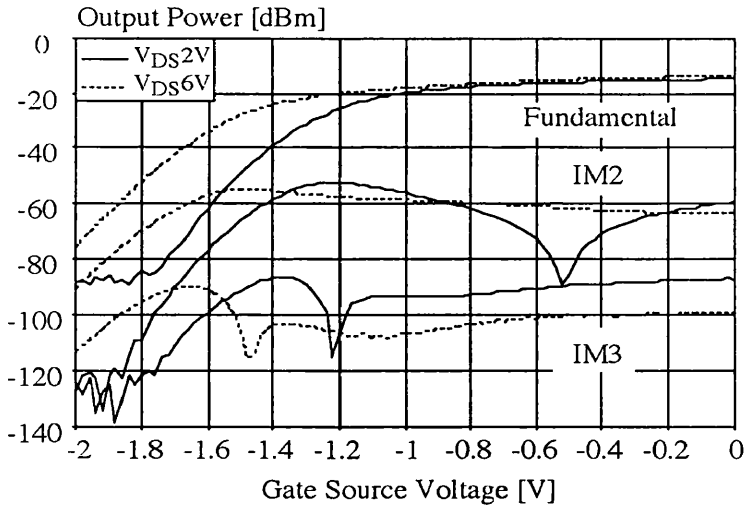

Figure 5.23: Effect of drain bias on measured bias dependent distortion of a MMT F20 6x100 μm MESFET for $V_{DS} = 2V$ and $V_{DS} = 6V$ with load resistance of 50 Ω. Input signal level is -15 dBm.

The bias dependant distortion for 4 samples of a MMT F20 MESFET from the same wafer are shown in Figure 5.24. It can be seen from Figure 5.24 that for devices with similar pinch-off voltage, the bias dependant distortion is almost identical. These devices show exceptional repeatability, with the distortion notches within ± 10 mV. It can be concluded that the bias dependent distortion is primarily influenced by pinch-off voltage variation.

Having described the factors which influence the distortion behaviour of a FET, we now present a visualisation technique which can be used for optimising amplifier performance.

5.5 Visualisation Technique for Optimum Design

As previously explained in Section 2.5 most simulator models are unable to predict 3rd order intermodulation distortion to sufficient accuracy for the minimisation of distortion [1], [5], [6] (see Figure 2.15). Fortunately it is possible to use the results of the nonlinear characterisation technique described, to provide a firm foundation for low distortion microwave design. By mapping intermodulation distortion for different drain and gate bias and load resistance it is possible to generate a composite contour plot. Figure 5.25 shows a contour plot of the magnitude of 3rd order intermodulation distortion, on which the line of maximum small signal power transfer (dotted line) is superimposed, and a line showing the location of

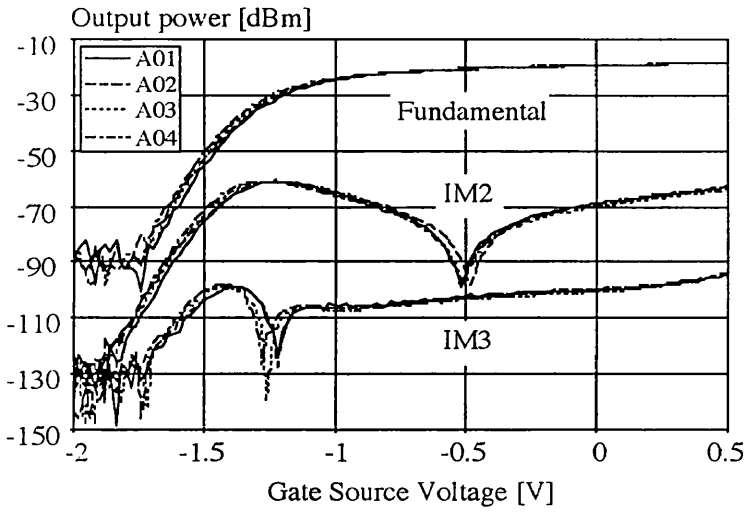

Figure 5.24: Example of sample to sample variation of measured bias dependent distortion for a MMT F20 6x100 μm MESFET for $R_{Load} = 50\Omega$ and $V_{DS} = 2V$.

the notch in 2nd order intermodulation distortion (solid line) with bias and load resistance is also shown.

From these maps it is sometimes possible to identify an optimum bias point for a particular device. Such a point is indicated on Figure 5.25. The minimum in 3rd order distortion shown in Figure 5.25 is relatively wide, allowing some immunity from process spread.

The effect of two different input power levels of -17 dBm and -7 dBm on the contour plot of Figure 5.25 and the optimum bias point is shown in Figure 5.26.

The 1 dB compression point of this device is about 10 dBm. It can be seen that the results are little affected by input powers below 1 dB compression.

In the light of the magnitude of the pinch-off voltage spreads in some processes, one may be tempted to question the usefulness of such maps of performance in a high volume production industrial setting. However, it should be noted that provided a relative measure of pinch-off voltage is available, then it should be possible to approximately transform the optimum bias point of Figure 5.25 on most samples of that process regardless of individual pinch-off voltage. This could mean that quick inexpensive DC measurements could be used to tune an amplifier to a low distortion operating point on a production line without the need for expensive time consuming distortion measurements. Due to the dominance of pinch-off voltage on the nonlinear characteristics, other process variables may have only a modest effect on performance, leading to acceptable yields.

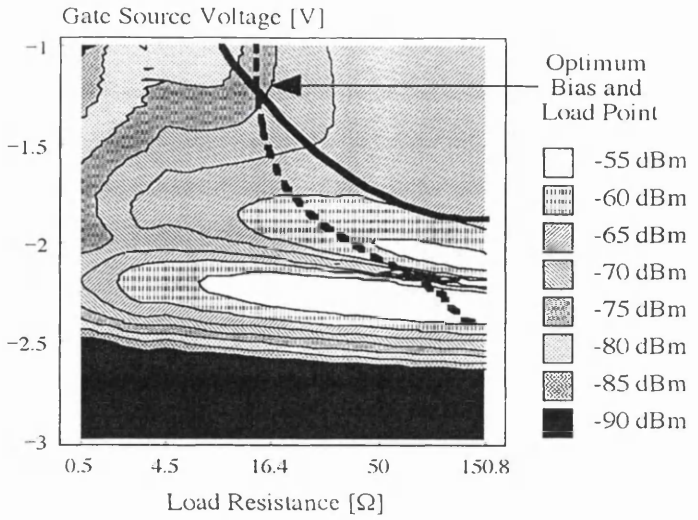

Figure 5.25: Selecting optimum bias and load for a low distortion amplifier (CLY5 GaAs MESFET). The contour plot is the measured 3rd order intermodulation distortion. The position of the 2nd order notch (solid line) and maximum power transfer (dotted line) are superimposed on the IMD3 contour. In put signal level is -17 dBm with a drain bias of 3 V.

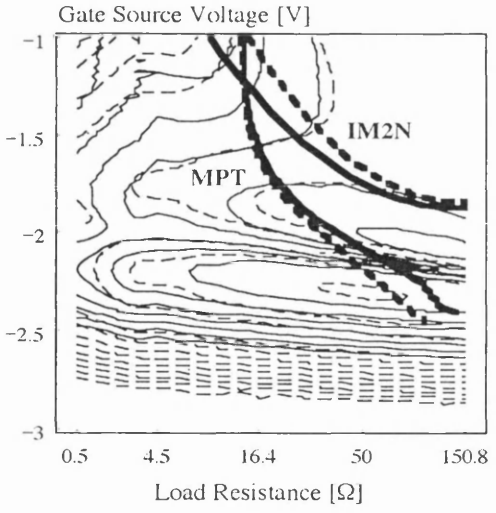

Figure 5.26: Effect of input power on optimum bias and load conditions for a low distortion amplifier (CLY5 GaAs MESFET). The contour plots shown are measured IMD3 for input signal levels of -7 dBm (dotted) and -17 dBm (solid). The positions of the IMD2 nulls (IM2N) and maximum power transfer (MPT) are shown as lines (-7 dBm (dotted) and -17 dBm (solid)) on top of the contour plots. Drain bias is 3 V.

5.6 Summary

When plotted against the DC gate bias the 2nd order distortion has a peak which gives rise to a pair of peaks in the 3rd order distortion. These are separated by a null which is associated with a change of sign of the 3rd derivative of the drain current with respect to gate-source voltage. 3rd order intermodulation in a CLY5 GaAs MESFET for gate biases higher than -0.5 V (class A operation mode) can be reduced considerably by increasing the drain bias. At higher voltage gains obtained with high load resistance the nonlinearity of a MESFET is more pronounced. The results are consistent with previous results [7], [8].

Soft pinch-off produces a characteristic distortion signature that occurs in a wide range of FETs including Si-JFETs, MOSFETs, MESFETs and HEMTs. The intermodulation distortion of a HEMT is considerably less sensitive to voltage gain than for a MESFET. Increasing drain bias can reduce 3rd order intermodulation distortion in a MESFET by up to 10 dB for a limited range of load resistance values. By using a nonlinear mapping technique with a suitable graphical interpretation, it is sometimes possible to identify low distortion regions of operation whilst still giving small signal matching.

In this chapter some of the factors which influence the intermodulation distortion performance of a FET were investigated. In Chapter 6 we will employ derivative superposition technique in order to design a circuit which is capable of generating a prescribed nonlinear function.

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Chapter 6

An Example of Derivative Superposition : A Nonlinear Function Circuit for a Quasi-Optical Tracking System

6.1 General

In Section 3.6.5 we reviewed measured performance results for a frequency doubler and frequency tripler based on the derivative superposition technique. We now apply the derivative superposition technique to a different nonlinear circuit which can be used in a quasi-optical tracking system.

The work in this chapter arose in the context of collaboration with the University of Glasgow [1], [2].

In this section we will discuss the development of a nonlinear function circuit required for a quasi-optical tracking system application (see Section 3.2.2). Derivative superposition [3], [4] will be used to realise this nonlinear function circuit [2] to generate a conjugate phase beam for the quasi-optical system. First we will discuss some preliminary deign considerations such as loss and gain budgets. Then, we will present the design steps for a low frequency version of the circuit operating at 100 MHz. The development of the 100 MHz circuit can provide experience in the use of derivative superposition to design the required nonlinear function and a useful step toward the design of the future version of the circuit to operate at 5 GHz. Due to delays at the University of Glasgow, none of the submitted circuit designs for this particular application have been fabricated.

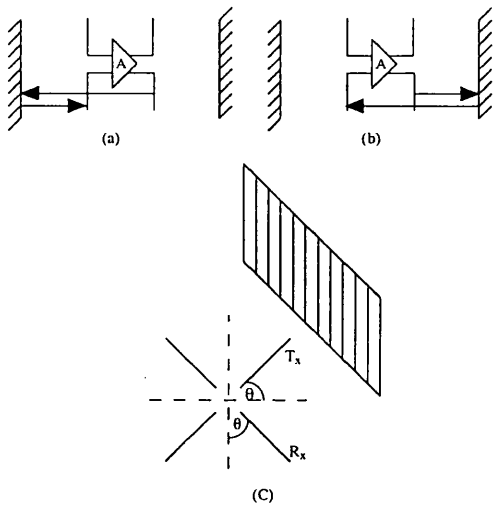

Figure 6.1: Individual amplifier cell, (a) and (b) show the two reflection paths and (c) represents the angle of rotation.

6.2 Preliminary Considerations for the Design

6.2.1 Gain Budget

In this section we consider the gain requirements for the quasi-optical tracking system [1], [2].

Estimation of Losses

It is important to know what the losses of the system will be in order to calculate a sufficient gain budget for the system. The losses present in this system include the antenna loss, grid amplifier alignment loss and propagation loss. Next, we will discuss these losses in turn.

Antenna

The antennas at the both ends are assumed to be quarter wave dipoles [1], [2]. These antennas have a radiation resistance of 72 Ω and have an antenna gain of 1.62 dB [5]. At the microwave frequency to be used of 5 GHz the length of each of the two elements of the dipole will be 1.5 cm. A minor correction factor to this length is necessary to ensure that the antenna is resistive at this frequency.

Effect of Grid Amplifier Alignment

A grid amplifier consists of an array of unit cells which include a receiver, a transmitter and a linear amplifier. At this point the number of transceiver cells and the distance apart were unknown. In order to make progress in developing a minimum requirement for the system we considered the behaviour of a single cell in isolation. Such a system is shown in Figure 6.1.

In Figure 6.1 we show one transceiver at an angle θ to a single polarising mirror. When the angle is 0°, the signal from the output antenna is reflected off the polarising mirror. However, all of the reflected signal is perpendicular to the receiving antenna and no feedback occurs.

When the angle is increased to say 45°, only part of the output signal is reflected from the polarising mirror. However, part of the reflected signal is received by the antenna leading to feedback.

We are now able to define an angle dependent loss due to the antenna alignment with the polarising mirror. This loss is in addition to any loss associated with propagation between the transmit and receive antennas. The angle dependent loss is given by the following expression.

$$L_{angle1m} = 10\log_{10}(\sin\theta\cos\theta) \tag{6.1}$$

From Eq. 6.1 we see that the loss is at a minimum at 45°. In the complete system we have two mirrors. Both mirror systems are described by the same equation. But the two contributions are orthogonal and hence, we have the following.

$$L_{ang2m} = 10\log_{10}(\sqrt{2}\sin\theta\cos\theta) \tag{6.2}$$

Therefore, with two mirrors and the amplifier array at an angle of 45° to the polarising mirrors there is a 3 dB loss. This loss is higher at other angles.

Propagation Loss

We now consider the case where the input and output antennas are aligned (this is not allowed in our system, but it enables us to calculate the propagation loss). We assume that the transceiver is approximately 5 cm from each polarising mirror, giving a total propagation distance of 10 cm (i.e. including the return path from the mirror). If we assume the propagation loss is described as in [5], then,

$$L_{prop} = 20\log_{10} f(MHz) + 20\log_{10} d(km) + 32.45 \tag{6.3}$$

where L_{prop} is the propagation loss, f is the frequency of operation in MHz and d is the distance between mirrors in km (see Figure 6.1).

Total Loss

In order to initiate oscillation, the electrical gain of the amplifier cell should be higher than the losses of the system. We can now sum the losses explained previously and derive the antenna gain as follows.

$$L_{overall} = L_{prop} + L_{ang} - G_{tx} - G_{rx} \tag{6.4}$$

where G_{tx} and G_{rx} are the transmitter and receiver gain, respectively.

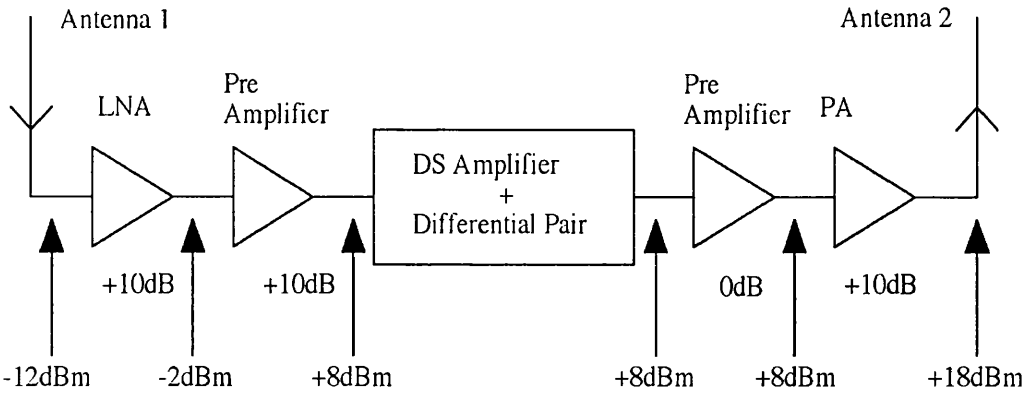

Figure 6.2: Gain budget of the system.

Thus, the minimum overall loss at 5 GHz is 25 dB (for 10 GHz the loss was 31 dB with the same mirror distance). This suggests a gain of at least 26 dB is needed to initiate oscillation.

In practice the loss will be less due to the contributions from the other transceivers in the grid and "near field" effects in the antenna [5].

Having defined the approximate power amplifier output and calculated the approximate loss of the system, it is now possible to sketch the power levels at different parts of the receiver. We assume that the power amplifier is at 1 dB compression, and producing the specified power. The system requires a particular power level for optimum performance. We can now see how many gain blocks are needed to obtain the correct input power to the nonlinear function block. We show such a gain and power budget in Figure 6.2.

6.2.2 Power Amplifier Considerations

The absolute output power of the grid amplifier has not been defined and it does not affect the initiation of oscillation. For convenience we choose a power level that requires minimum matching. Since the radiation resistance ($R_{rad.}$) of the antenna is 75 Ω, and a typical drain bias (V_P) is 3 V, then the maximum output power (P_{out}) is given by the following.

$$P_{out} = 20\log_{10}(V_P) - 10\log_{10}(2R_{rad.}) = -12.219dB \tag{6.5}$$

which is equivalent to 60 mW (or 18 dBm) and is achievable using a FET of moderate gate width.

6.2.3 Proposed Electrical Specification of the Transceiver Cell

The specification of the proposed transceiver cell is given in Table 6.1.

Table 6.1: Specification of the proposed transceiver cell.

Parameter	Value	Unit
Input impedance	75	Ω
Output impedance	75	Ω
Gain	28	dB
Output power at 1dB comp.	18	dBm
Bandwidth	10	%

An issue of importance is amplitude stabilisation. Ideally we want to stabilise the gain so that the nonlinear function cell is working at the optimum signal level to maximise the level of conjugate reflection. This is somewhat contrary to the nature of oscillation, where amplitude stabilisation is normally achieved by 1 dB compression of the output stage with no control of the signal level at the input of the function block. Hence, more complex amplitude stabilisation techniques should ideally be considered in the light of the performance of the entire system.

In this section we have looked at the behaviour of a single transceiver in the grid amplifier environment in an attempt to derive the minimum electrical performance to ensure oscillation of the grid amplifier.

Next, we will discuss the design procedure for a 100 MHz circuit based on derivative superposition capable of generating the desired nonlinear function to generate a conjugate phase beam for the quasi-optical system.

6.3 UoG MESFET Characterisation

This design is intended for fabrication in MMIC form using the University of Glasgow MONOFAST MESFET MMIC process. On-wafer distortion measurements based on the TDFD method were carried out in order to study the nonlinear behaviour of the device to be used. The measurement set-up is the one described in Section 4.3.3. DC measurements were carried out on a UoG MESFET device with 1 gate finger of 60 μm in order to facilitate the extraction of a model to be

used in the design of the circuit. The FET FIT 7.4 package [6] was used to extract a Parker Skellern model according to the DC measurement data [7], [8], [9], [10]. One way of extracting a model using FET FIT is to use DC measurement data and also RF transconductance, g_m, and output conductance, g_{ds} , values. RF distortion measurements carried out for this device for two values of load resistance enabled us to calculate the RF g_m and RF g_{ds} of the device using the technique described in Section 5.3.1. FET FIT 7.4 was used to fit a Parker Skellern model. The Parker Skellern model parameters are presented in Table 6.2.

Table 6.2: Parker Skellern model parameters of a 60 μm UoG MONOFAST MESFET.

General I-V Curves			Rate and History Dependance		
Triode Region			LF Electrostatic Feedback		
Beta [A]	VTO [V]	P	LFGAM	LFG1 [V^{-1}]	LFG2 [V^{-1}]
0.0002	*-0.484*	*2.270*	*0.123*	*0.085*	*0.030*
Knee Region			HF Electrostatic Feedback		
XI	MXI	Z	HFGAM	HFG1 [V^{-1}]	HFG2 [V^{-1}]
0.207	*0.0*	*0.867*	*0.277*	*-0.096*	*0.081*
Saturated and Subthreshold			HF Transconductance Drop		
Q	VST	MVST [V^{-1}]	HFETA	HFE1 [V^{-1}]	HFE2 [V^{-1}]
1.713	*0.090*	*0.193*	*-1.143*	*-0.129*	*-1.896*
Contact Resistance			Time Constants and Self Heating		
RS [Ω]	RD [Ω]		TAUG [s]	TAUD [s]	DELTA [W^{-1}]
180	*180*		*1E-4*	*1E-5*	*3.256*

An example of the DC fit of the model is shown in Figure 6.3. It can be seen from Figure 6.3 that the model gives a very good fit of the DC I-V behaviour. The model also provided an acceptable fit of HF g_m and g_{ds}.

6.4 Design of a 100 MHz Circuit

Now we will present the steps for the design of a low frequency MMIC version working at 100 MHz to verify the correct operation of the nonlinear function circuit block. We will describe the design paying attention to each part of the circuit with relevant SPICE simulations.

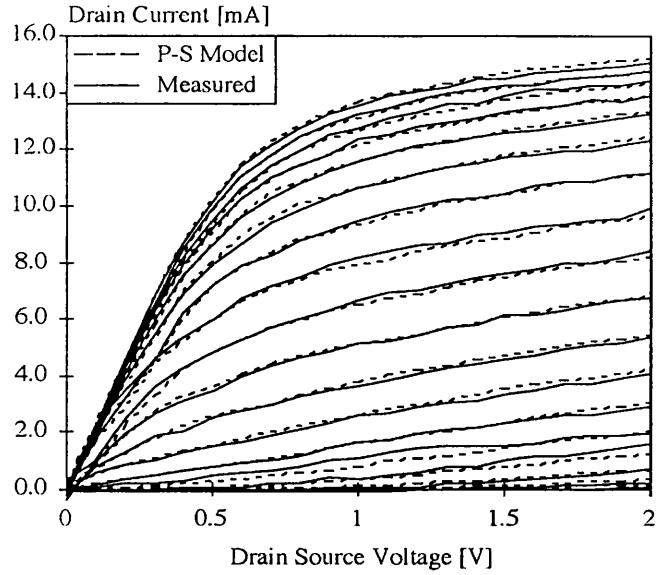

Figure 6.3: DC I-V fit of the P-S model to the 1x60 μm UoG MONOFAST MESFET. Gate bias is swept from -1.2 V to +0.5 V in 0.1 V steps.

6.4.1 Design Strategy

As mentioned before, the idea for this design is to use the 3rd order nonlinearity in the transceiver to generate a conjugate signal to implement a thin hologram at microwave frequencies. In order to satisfy this, let us consider a transfer characteristic function of the following form.

$$y = kx^3 + rx \tag{6.6}$$

where x and y are the input and output signals, respectively, and k and r are constants. Ideally large values of k and r should be used in order to obtain significant signal transfer and conjugate waveform generation. At this point we are only interested in the approximate ratio of k and r, as the overall magnitude can be changed by linear amplification.

6.4.2 A Derivative Superposition Solution

In order to understand the implementation steps of the transfer characteristic of Eq. 6.6 it is desirable to differentiate the transfer characteristic in order to obtain a parabolic function. This will give us the transconductance with respect to the gate source voltage.

$$\frac{dy}{dx} = 3kx^2 + r \tag{6.7}$$

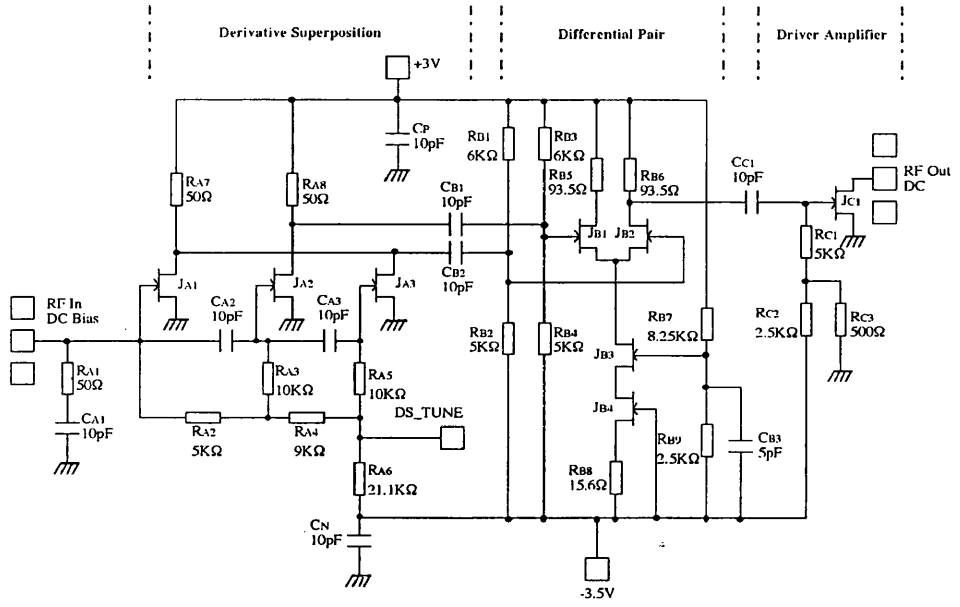

Figure 6.4: Proposed circuit for implementing $y = kx^3 + rx$ function.

Eq. 6.7 describes a transconductance that falls and rises parabolically around the quiescent point, $x = 0$, but does not fall to zero at $x = 0$.

In order to implement this function we need a minimum number of 3 FETs. FET1 gives finite transconductance. FET2 reduces the transconductance to form the left hand downward curve of the parabola. FET3 increases the transconductance to form the right hand upward curve of the parabola. The biasing point for the circuit would then be at the minimum of the parabolic region.

Having described the circuit requirements, next we will present the implementation procedures of this circuit.

6.4.3 Circuit Implementation

The schematic diagram of the whole circuit designed is presented in Figure 6.4.

The passive and active component values for the 100 MHz design are given in Table 6.3 and Table 6.4, respectively.

The circuit shown in Figure 6.4 can be divided into 3 sections as follow. Transistors J_{A1} to J_{A3} comprise the derivative superposition block, transistors J_{B1} to J_{B4} comprise a differential pair block and transistor J_{C1} comprises the output driver stage. Each section will be described in turn.

Table 6.3: Passive components of the design.

Derivative Superposition Section										
Resistors [Ω]								Capacitors [pF]		
R_{A1}	R_{A2}	R_{A3}	R_{A4}	R_{A5}	R_{A6}	R_{A7}	R_{A8}	C_{A1}	C_{A2}	C_{A3}
50	5K	10K	9K	10K	21.1K	50	50	10	10	10

Differential Pair Section											
Resistors [Ω]									Capacitors [pF]		
R_{B1}	R_{B2}	R_{B3}	R_{B4}	R_{B5}	R_{B6}	R_{B7}	R_{B8}	R_{B9}	C_{B1}	C_{B2}	C_{B3}
6K	5K	6K	5K	93.5	93.5	8.25k	15.6	2.5k	10	10	5

Driver amplifier			
Resistors [Ω]			Capacitor [pF]
R_{C1}	R_{C2}	R_{C3}	C_{C1}
5K	2.5K	500	10

6.4.3.1 Derivative Superposition Block

This section consists of 3 common-source FETs of different gate widths with different gate bias points. The input RF signal is applied to all 3 FETs. The bias for the FET gates is provided by a resistive potential divider. In order to determine the component values necessary for the biasing of the gates, this section was simulated using SPICE version 3f4. Two resistors of value 50 Ω on the drains of transistors J_{A1} and J_{A2} of Figure 6.4 are to ensure stability at low frequencies. Considering the DS section of Figure 6.4 J_{A1} provides finite transconductance, J_{A2} reduces the transconductance to form the left hand downward curve of the required parabola and J_{A3} increases the transconductance to form the right hand upward curve of the parabola. The biasing point for the circuit would then be at the minimum of the parabolic region. In Figure 6.5 we show the simulated transconductance curves of the DS section forming the composite structure described by Eq. 6.7 as a function of gate source voltage.

The optimum bias point is at gate source voltage of 0 V at the minimum of the parabolic region. The dynamic transfer characteristic of the DS section is compared with that of the ideal case given by Eq. 6.7 and is shown in Figure 6.6.

It can be seen from Figure 6.6 that the design gives a reasonable approximation to Eq. 6.7.

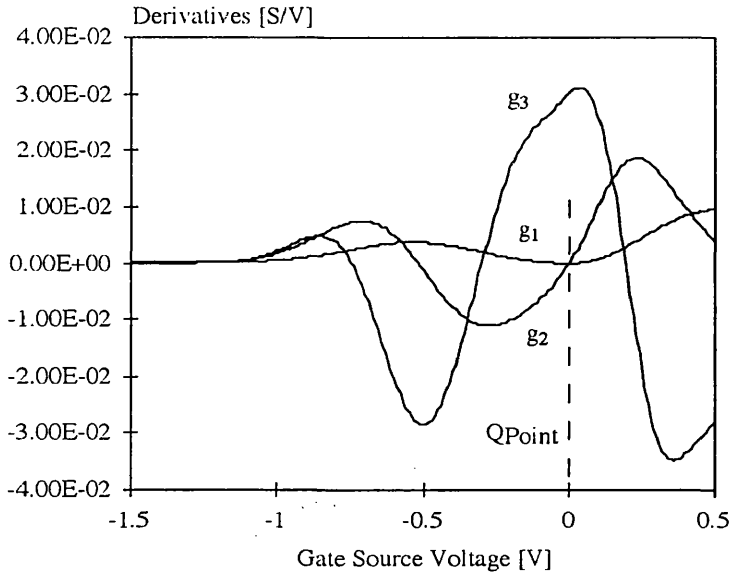

Figure 6.5: Derivative structure versus gate bias.

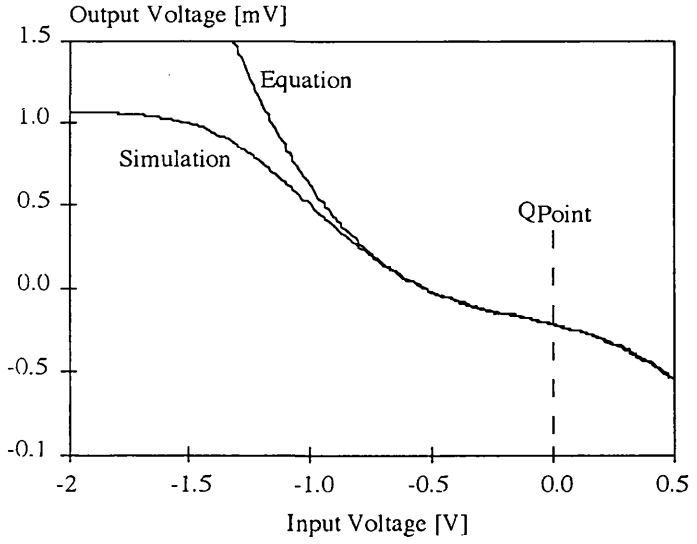

Figure 6.6: Dynamic transfer characteristic simulation with equation fit.

Table 6.4: Active components of the design.

Transistor	Gate width [μm]	Gate length [μm]	V_{GS} [V]
JA_1	1x100	1	0
JA_2	1x135	1	-0.50
JA_3	1x90	1	-1.39
JB_1	2x100	1	-0.52
JB_2	2x100	1	-0.52
JB_3	4x100	1	-0.52
JB_4	4x100	1	-0.52
JC_1	4x87.5	1	-0.6

In derivative superposition it is important that the signals at the gates of the FETs are in phase. Figure 6.7 shows the simulated phase of the signal at the gate of each FET.

As can be seen from Figure 6.7 between 100 MHz and 2 GHz the phase difference is only about 5 degrees maximum and reduces as frequency increases.

6.4.3.2 Differential Pair Block

It was previously discussed that it was necessary for the output current of transistor J_{A2} to be subtracted from the output currents of transistors J_{A1} and J_{A3} (see Figure 6.4). In order to carry out this subtraction a differential pair will be employed which is capable of providing broad bandwidths. Various configurations of differential pair were investigated including resistive and active loads, cascode and non-cascode current sources and various gate and drain bias voltages. These options are now discussed.

6.4.3.2.1 Passive Loading

With passive loading two slightly different designs were investigated.

First Configuration

The circuit diagram of this differential pair amplifier is shown in Figure 6.8.

The voltage between the drain and source of each FET is 1 V. The gate width of each of the FETs in the differential pair is 100 μm. The transfer characteristic of the differential pair was obtained using SPICE and is shown in Figure 6.9.

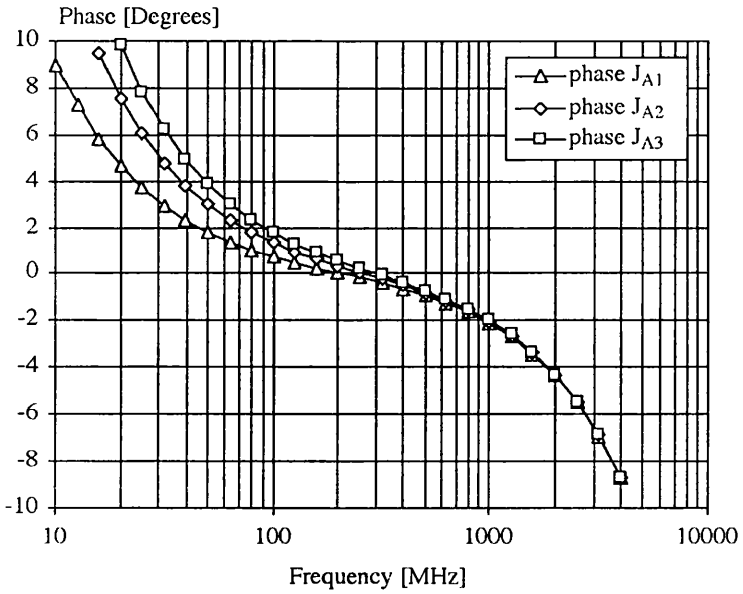

Figure 6.7: The phase response on the gates of the FETs.

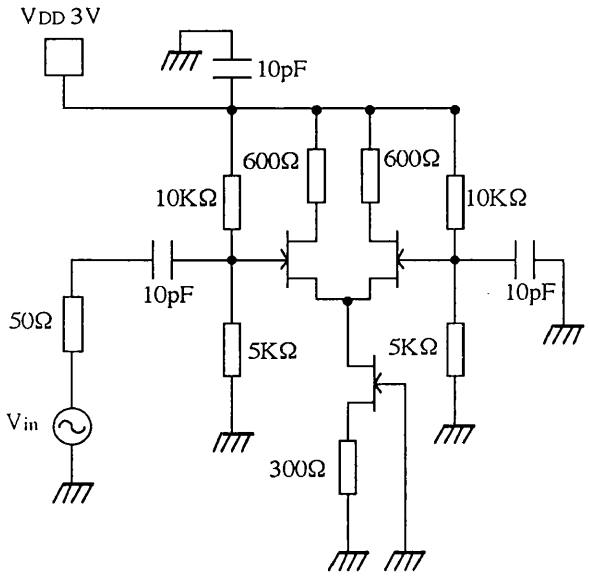

Figure 6.8: Differential pair with passive loading; connection to ground.

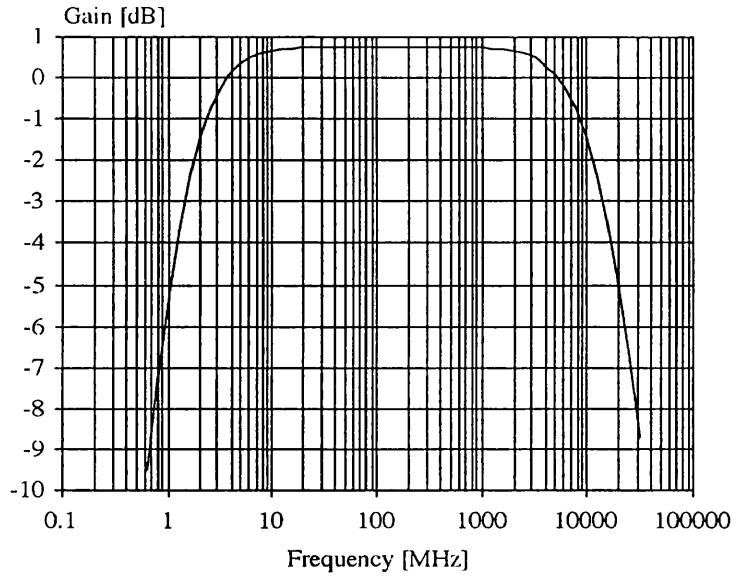

Figure 6.9: The transfer characteristic of the differential pair with passive loading; connection to ground.

It can be seen from Figure 6.9 that very little gain is achievable at the frequency of operation. Increase of the load resistances in order to increase gain caused an unacceptable reduction in bandwidth.

Second Configuration

In the first configuration the voltage between the drain and source of each transistor of the differential pair was 1 V. This voltage (V_{DS}) was to be increased in order to obtain a lower output conductance and higher voltage gain for the circuit. Therefore, the biasing resistors and the source resistor of the current source were connected to a negative supply voltage. The circuit diagram for this design is shown in Figure 6.10 .

The voltage between the drain and source of each FET is now 1.5 V. This also enables us to use a larger load resistance for the differential pair than the one used in the first configuration which results in having a higher voltage gain. The gate width of each of the FETs in the differential pair is still 100 μm. The plots for gain and common mode rejection ratio are in Figure 6.11 and Figure 6.12, respectively.

It can be seen from Figure 6.11 and Figure 6.12 that the circuit is capable of providing a gain of about 5.25 dB and a rejection of about -16.3 dB over the operating bandwidth of 50 MHz to 300 MHz. The transient simulations of the differential pair amplifier with a large amplitude DC signal using SPICE is shown in Figure 6.13.

As it can be seen from Figure 6.13 the circuit is capable of working in the linear

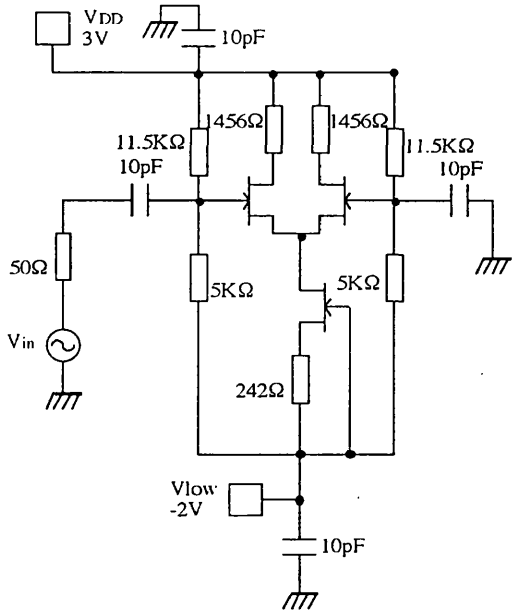

Figure 6.10: Differential pair with passive loading; connection to -2 V rail.

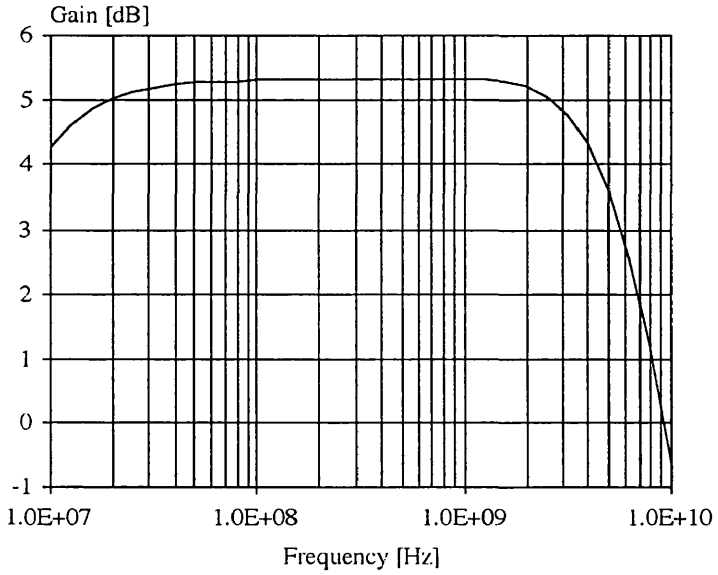

Figure 6.11: The transfer characteristic of the differential pair with passive loading; connection to -2 V rail.

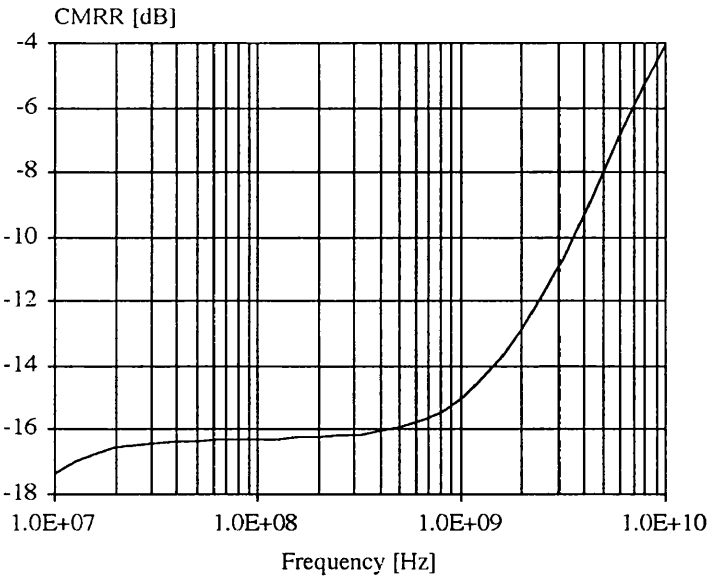

Figure 6.12: The common mode rejection ratio of the differential pair with passive loading; connection to -2 V rail.

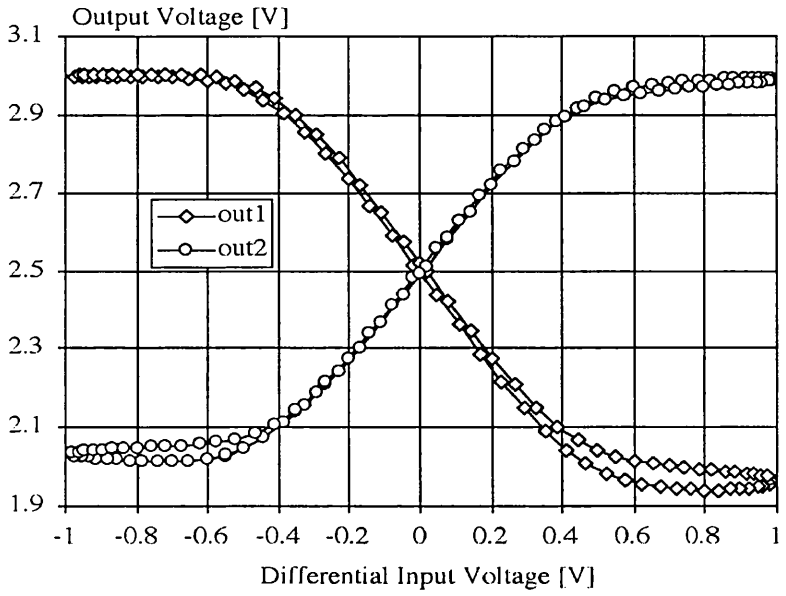

Figure 6.13: The transient characteristic of the differential pair amplifier with passive loading; connection to -2 V rail.

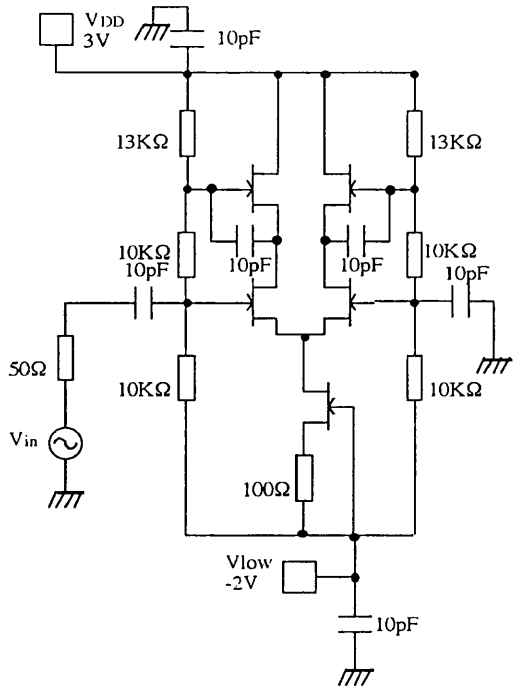

Figure 6.14: Differential pair with active loading.

region for input voltages ranging from about -0.3 V to +0.3 V.

6.4.3.2.2 Active Loading

An active loading configuration for the differential pair was also investigated. The circuit diagram is shown in Figure 6.14.

The voltage between the drain and source of each FET is 1.5 V. The gate width of each of the FETs in the differential pair and the active loads is 100 μm. The gain and common mode rejection ratio responses are presented in Figure 6.15 and Figure 6.16, respectively. It can be seen from Figure 6.15 and Figure 6.16 that the gain is reduced by about 0.25 dB and the bandwidth is decreased substantially with the rejection being about 1 dB better than the design with passive loading (second configuration) described earlier.

6.4.3.2.3 Cascode Current Source Configuration

In order to reduce the output conductance of the current source and hence, increase the CMRR, it was decided to use a cascode current source configuration. Two configurations were studied in regard to the gate length of the transistors.

1 μm Gate Length Design

The circuit diagram is shown in Figure 6.17.

This circuit uses passive loading together with a cascode current source in order

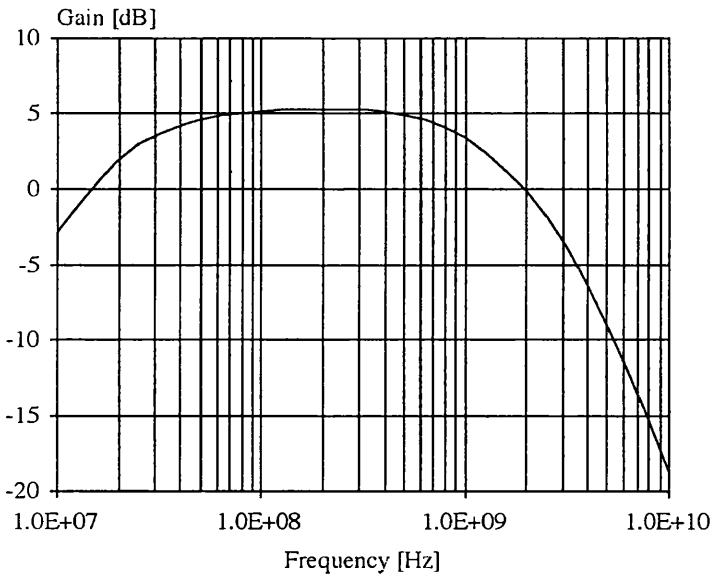

Figure 6.15: The transfer characteristic of the differential pair with active loading; connection to -2 V rail.

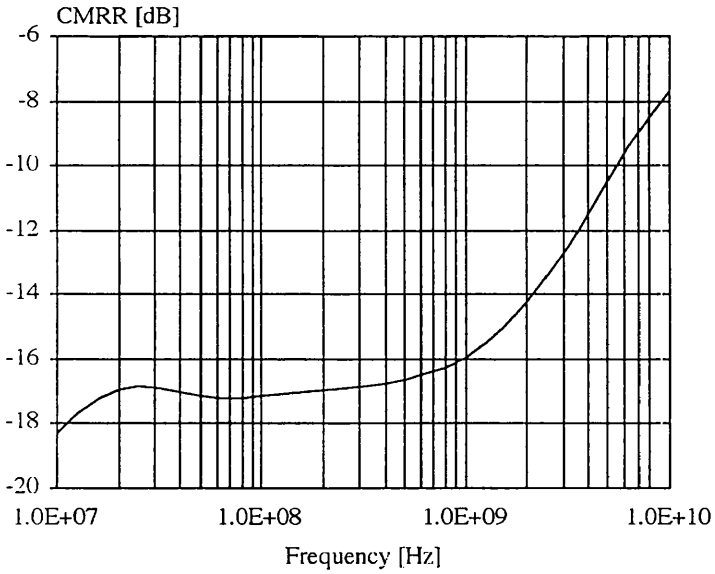

Figure 6.16: The common mode rejection ratio of the differential pair with active loading; connection to -2 V rail.

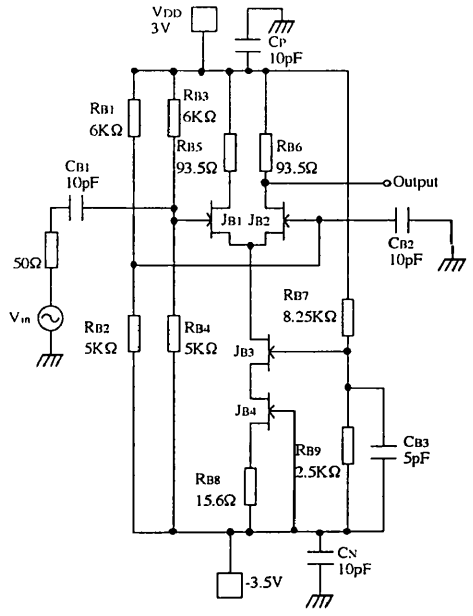

Figure 6.17: Differential pair with cascode current source configuration.

to reduce the output conductance effects. The voltage across each FET is 1.5 V. The gate width of each of the FETs in the differential pair is 200 μm. The gain and rejection responses are presented in Figure ?? and Figure 6.18, respectively.

It can be seen that the gain is increased only by a small amount. The common mode rejection ratio is improved by about 16 dB over the frequencies of interest compared to the design with active loading.

In order to see the effect of the "next stage" (driver amplifier) loading on the performance of the differential pair amplifier, input capacitor, C_{gs}, of the driver amplifier was determined by SPICE and it was found to be 0.5 pF. The simulated gain performance of the design with and without the effect of "next stage" loading is shown in Figure 6.19.

It can be seen from Figure 6.19 that the bandwidth is reduced substantially due to this "next stage" loading.

0.2 μm Gate Length Design

The circuit diagram is the same as Figure 6.17. The gate width of each of the FETs in the differential pair is 200 μm. The gain and common mode rejection ratio responses are presented in Figure 6.20 and Figure 6.21, respectively.

It can be seen from Figure 6.20 and Figure 6.21 that the gain and the common mode rejection ratio characteristic have degraded substantially compared to the 1 μm gate length design. This is due to the output conductance problems associated with the short gate length FETs. The gain performance with the effect of the

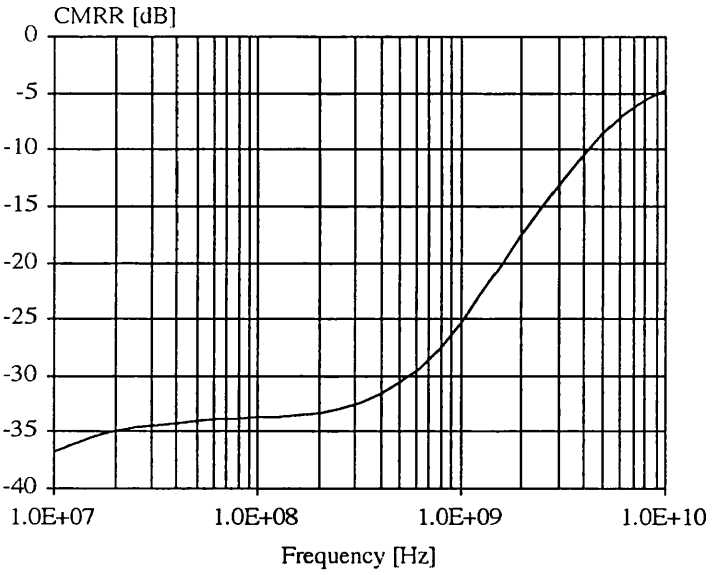

Figure 6.18: The common mode rejection ratio of the differential pair with cascode current source configuration; 1 μm gate length design.

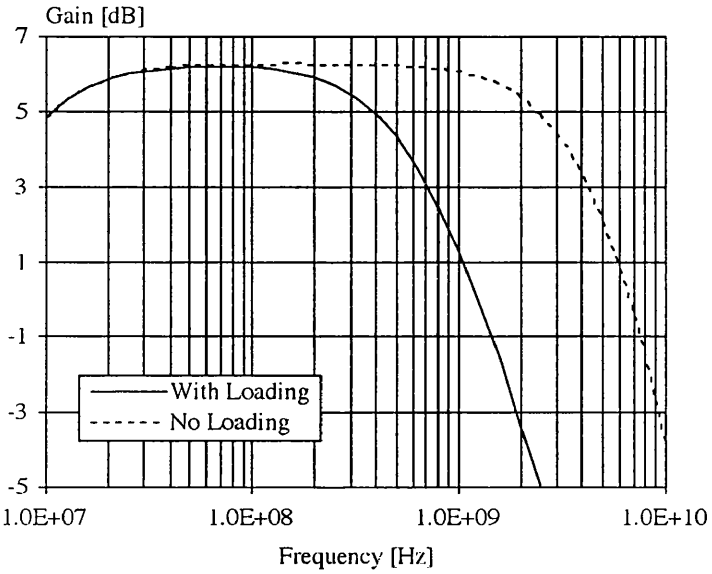

Figure 6.19: The effect of the next stage (driver amplifier) loading on the performance of the differential pair amplifier with cascode current source configuration; 1 μm design.

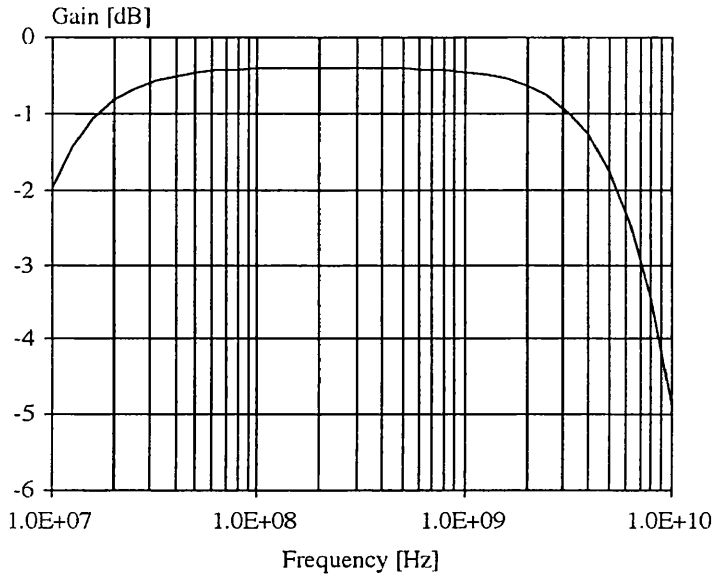

Figure 6.20: The transfer characteristic of the differential pair with cascode current source configuration; 0.2 μm gate length design.

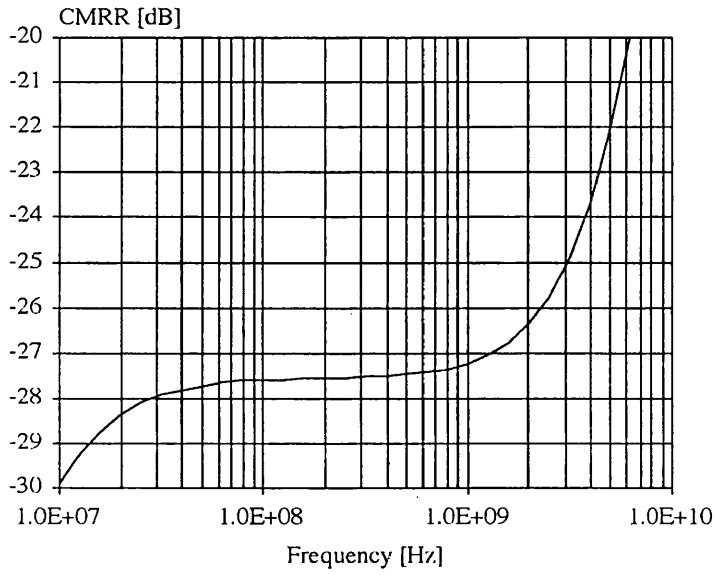

Figure 6.21: The common mode rejection ratio of the differential pair with cascode current source configuration; 0.2 μm gate length design.

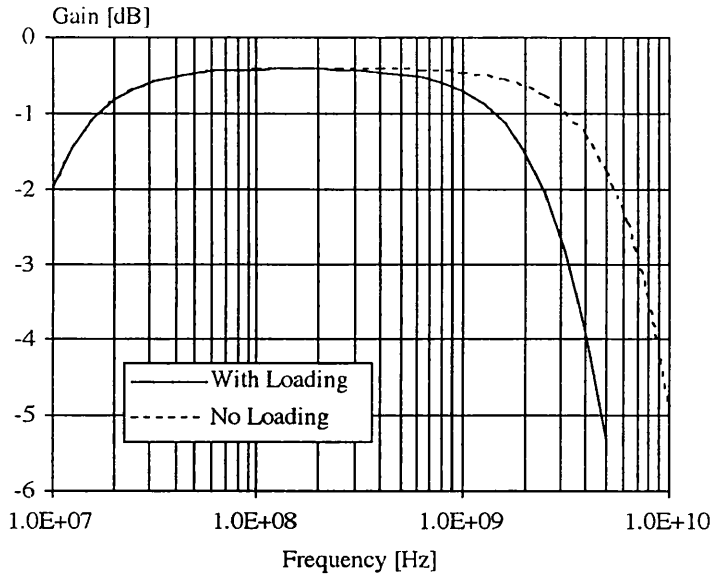

Figure 6.22: The effect of the next stage (driver amplifier) loading on the performance of the differential pair amplifier with cascode current source configuration; 0.2 μm gate length design.

loading of the next stage is shown in Figure 6.22.

It can be seen from Figure 6.22 that the bandwidth is not reduced significantly compared to the loading case for the 1 μm design.

Considering the simulations described, the final design of the 100 MHz circuit for this section was chosen to have the following design decisions.

It was decided to adopt the resistive loading case due to the high gain and good common mode rejection ratio described above. It was decided to use a cascode current source configuration in order to obtain a lower output conductance for the circuit. The 0.2 μm gate length gave a better bandwidth but since the 1 μm design produced a better gain and also the fact that the 0.2 μm design suffers more from output conductance problems than the 1 μm design, it was decided that the design will be based on 1 μm gate length FETs.

6.4.3.3 Driver Amplifier Block

Since the combined gain of the derivative superposition section and the differential pair amplifier is very small, an amplifier is needed to boost the signal. The schematic diagram of the driver amplifier is shown in Figure 6.23. It should be noted that the 50 Ω driving impedance of the amplifier is a close approximation of the output impedance of the differential pair presented in Figure 6.17; which is approximately equal to the parallel combination of the output resistance of the

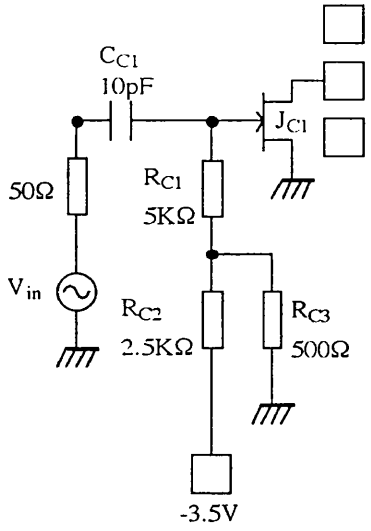

Figure 6.23: The schematic diagram of the driver amplifier.

J_{B2} transistor and R_{B6} resistor of Figure 6.17.

Table 6.5 shows the simulations carried out for FETs with different gate widths biased at various gate source voltages with $V_{DS} = 3V$ and 75 Ω load.

The SPICE simulation of the gain of this stage is shown in Figure 6.24. This amplifier uses a FET with the gate width of 350 μm biased at $V_{GS} = -0.6V$ and $V_{DS} = 3V$ with a load resistance of 75 Ω and as can be seen in Figure 6.24, it is capable of providing a gain of about 7.5 dB over the frequency of operation.

6.4.4 MMIC Layout

The layout plot of the overall circuit is shown in Figure 6.25. The RF input is applied to the gates of the FETs from the left hand side. The bias voltages required for the DS FETs are provided by a resistor chain. The drains of transistors J_{A1} and J_{A3} of the DS section are joined to provide current summation and are fed to one side of the differential pair and the drain of transistor J_{A2} of the DS section is fed to the other side of the differential pair in order to have a current subtraction. The output taken from the differential pair is fed to an amplifier stage. The RF output pad is on the right hand side of the layout. The top and bottom DC pads are used for biasing.

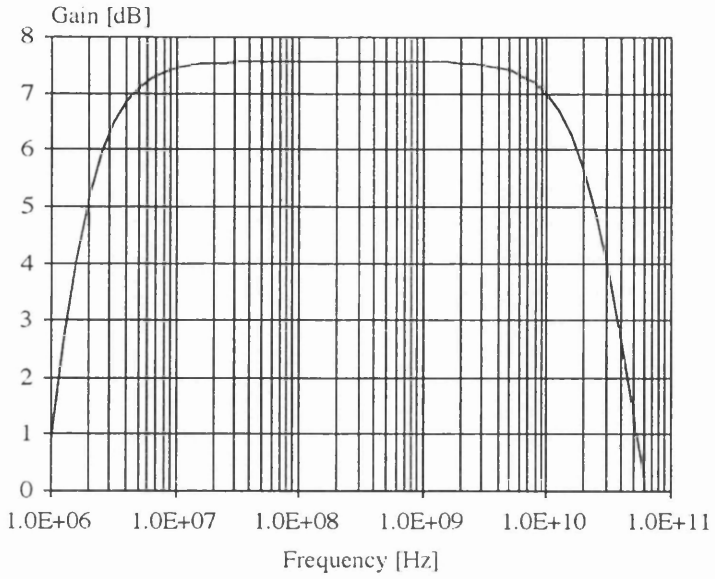

Figure 6.24: The gain performance of the driver amplifier stage.

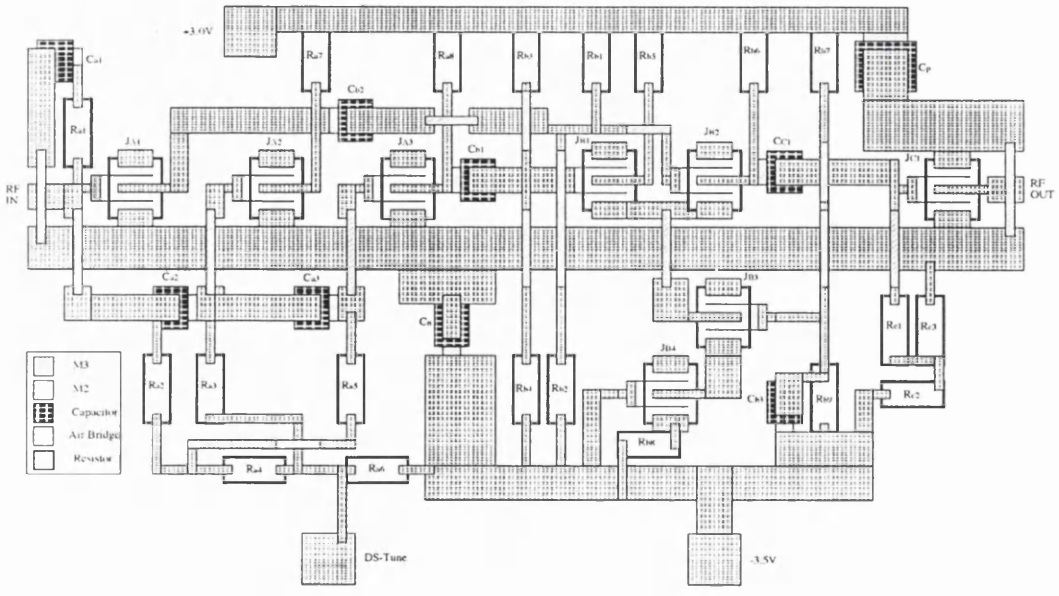

Figure 6.25: Layout plot of the overall circuit.

Table 6.5: Simulated comparison of various driver stages.

GW	V_{GS}	P_{1dB}	P_{Sat}	PAE_{1dB}	PAE_{Sat}	Gain_{1dB}
[μm]	[V]	[dBm]	[dBm]	[%]	[%]	[dB]
250	-0.4	15.37	18.46	32.87	66.98	7.13
250	-0.5	14.87	17.83	34.36	67.98	6.63
250	-0.6	14.25	17.17	35.79	70.07	6.01
300	-0.4	16.29	19.33	33.90	68.24	8.05
300	-0.5	15.82	18.65	35.68	68.45	7.58
300	-0.6	15.25	17.93	37.51	69.62	7.01
350	-0.4	17.00	20.10	34.20	69.85	8.76
350	-0.5	16.55	19.38	36.14	69.37	8.31
350	-0.6	16.00	18.61	38.25	69.75	7.76

6.5 Summary

The possibility of implementing a nonlinear function circuit working at 100 MHz using derivative superposition approach has been discussed. The design uses a differential pair for the required subtraction and a driver amplifier stage in order to boost the overall gain of the circuit. The simulation results appear to be promising. This circuit is to be implemented using the University of Glasgow MONOFAST MESFET MMIC process as a single chip.

In this chapter it was shown that it is possible to employ derivative superposition technique in order to design circuits which are capable of generating a prescribed nonlinear function. In Chapter 7 we will explore the possibility of applying the derivative superposition technique in a power amplifier.

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Chapter 7

Low Distortion MMIC Power Amplifier Using Derivative Superposition

7.1 General

In modern multi-channel high capacity wireless communication systems, there is a stringent requirement to minimise interference to adjacent channels to prevent data loss. This is a particular concern in power amplifiers where operation close to 1 dB compression is highly desirable. A number of practical system level black-box techniques have been proposed for reducing adjacent channel interference arising from nonlinear device behaviour including feedforward, feedback and predistortion which were discussed in Section 3.7.2. An alternative approach is to minimise distortion at a circuit level. One such approach is the derivative superposition (DS) method [1], [2] which was discussed in Sections 3.4.2, 3.5.6 and 3.6.5. This utilises several parallel FETs of different gate width and gate bias to alter the nonlinear behaviour of a main FET. The key difficulty with extending such techniques to large signals is that available CAD models do not correctly describe large signal frequency dispersion effects seen in GaAs FETs [3], [4], [5]. In multi FET circuits, measurement based design approaches (such as [2], [6]) are useful for minimising small signal distortion, but are very difficult to modify for minimising large signal distortion due to frequency dispersion effects described in Section 2.5.8 of this thesis.

In Section 3.7.3 the possibility of using the derivative superposition technique to design power amplifiers was discussed. Some problems were encountered such as the need to use unrealistically low load resistors in order to control the shape of

the derivatives [7]. The objective of the work described in this chapter is to design a simplified form of derivative superposition amplifier in MMIC form suitable for power amplifier implementation using only two FETs [8] which overcomes some of these difficulties. The design should achieve a null in the 3rd order intermodulation distortion at high signal levels close to 1 dB compression and be sufficiently robust that it can be designed with existing CAD tools.

In Section 7.2 we propose a novel MMIC DS power amplifier using the phase reversal technique. We first describe some distortion measurements carried out in order to characterise a MMT F20 device. Then, a Parker Skellern model [9], [10], [11], [12] is extracted for simulation purposes. Then, we describe the derivative superposition strategy used for this design. Results of simulation using Super Deriv [13] will be presented. These include spectral regrowth and adjacent channel power ratio (ACPR) simulations. Then, the measured performance of the MMIC DS power amplifier will be studied including single and two tone efficiencies and two tone carrier to interference ratio performance. The effect of load resistance, drain bias and voltage offset on distortion will also be studied. Then, an example will be presented indicating the potential advantage of the DS amplifier compared with single FET amplifiers. An alternative implementation of the DS amplifier using the University of Glasgow (UoG) MONOFAST MESFET process will also be discussed and some measured responses will be presented. Finally, a comparison will be carried out for the technologies used.

In Section 7.3 we explore the possibility of designing a composite Doherty-DS amplifier. The Doherty amplifier [14], [15], [16] was discussed in Section 3.5.5. This will include the simulation results of carrier to interference ratio and efficiency response for a reference FET, the Doherty circuit, the DS circuit and the composite Doherty-DS structure.

In Section 7.4 an overall summary of the work presented in this chapter will be given.

7.2 MMIC Design, Fabrication and Test

7.2.1 MMT F20 Characterisation

On-wafer distortion measurements based on the TDFD method were carried out in order to study the behaviour of the MMT F20 device to be used. The measurement set-up is the one described in Section 4.3.3. First DC measurements were carried out in order to investigate a proposed load line for a single device which is used

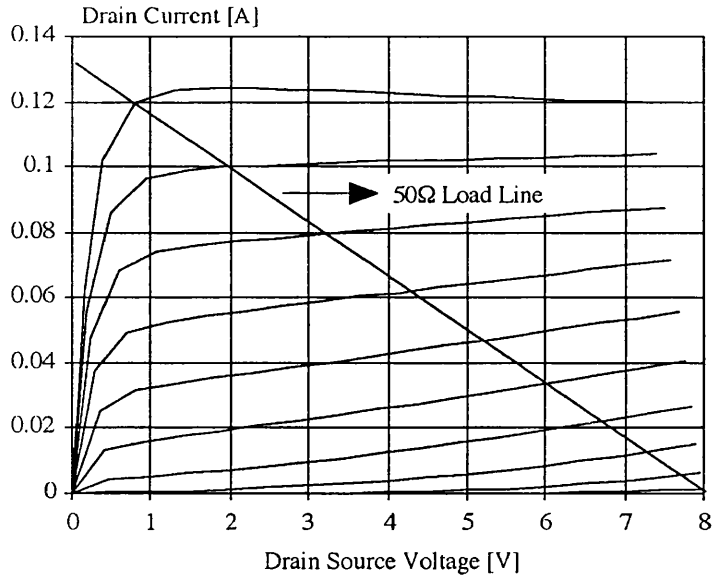


Figure 7.1: Proposed load line for the design. Gate bias is swept from -2 V to +0.5 V in 0.25 V steps.

as a reference with which to compare the derivative superposition amplifier. The 50 Ω load line for a F20 GaAs MESFET with 6 gate fingers of 100 μm is shown in Figure 7.1.

Distortion measurements were carried out to see the effect of varying the drain source voltage. The plot of the results is shown in Figure 7.2 .

It can be seen from Figure 7.2 that higher drain bias causes a suppression of the IMD2 notch and a reduction of the IMD3 level in agreement with results for other devices carried out in Section 5.2.2.

As mentioned in the background section, in order to have a derivative superposition circuit functioning properly, it is important to have an idea of the process changes which cause the position of the notches in IMD2 and IMD3 to vary. In Figure 7.3 we present the distortion measurement results for 5 FETs from the same wafer in order to observe the repeatability of the device characteristics.

It can be seen from Figure 7.3 that for four of the devices the process variation is quite negligible. The 5th device shows considerable process variation and this effect should be accounted for in the design. In order to see the effect of load resistance variation on intermodulation distortion of this device, 4 load resistor values were used. The plot for this measurement is shown in Figure 7.4.

It can be seen from Figure 7.4 that increasing the load resistance moves the notches in IMD2 and IMD3 to a more negative gate bias, as expected and in agreement with the results in Section 5.2.3. The movement is greater for the

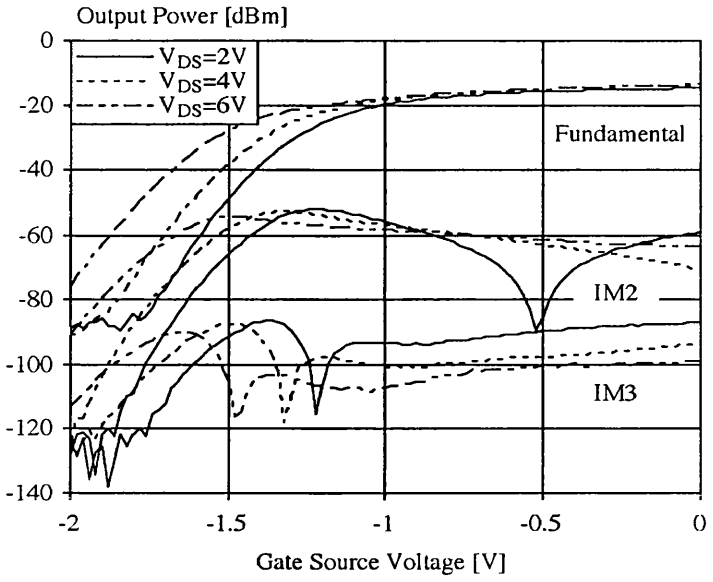


Figure 7.2: Measured effect of different drain source voltages on a 6x100 μm F20 GaAs MESFET. Input signal level is -15 dBm and load resistance is 50 Ω.

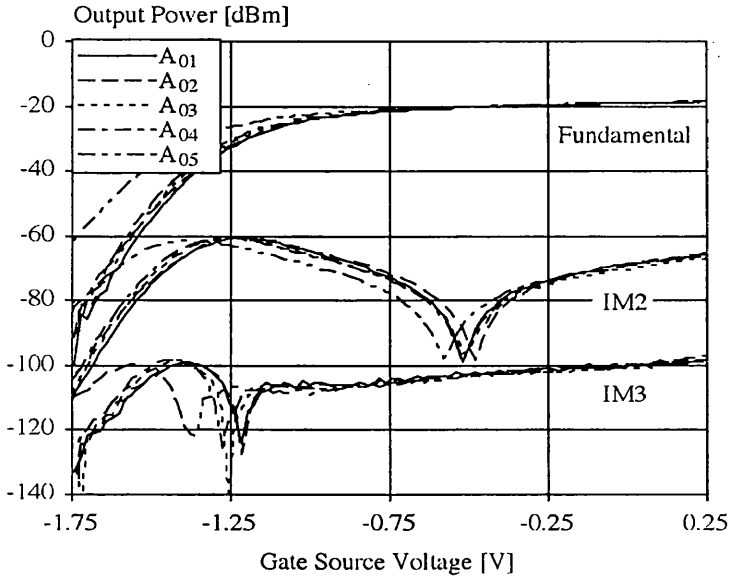


Figure 7.3: Measured sample to sample study of five 6x100 μm F20 GaAs MESFETs from the same wafer.

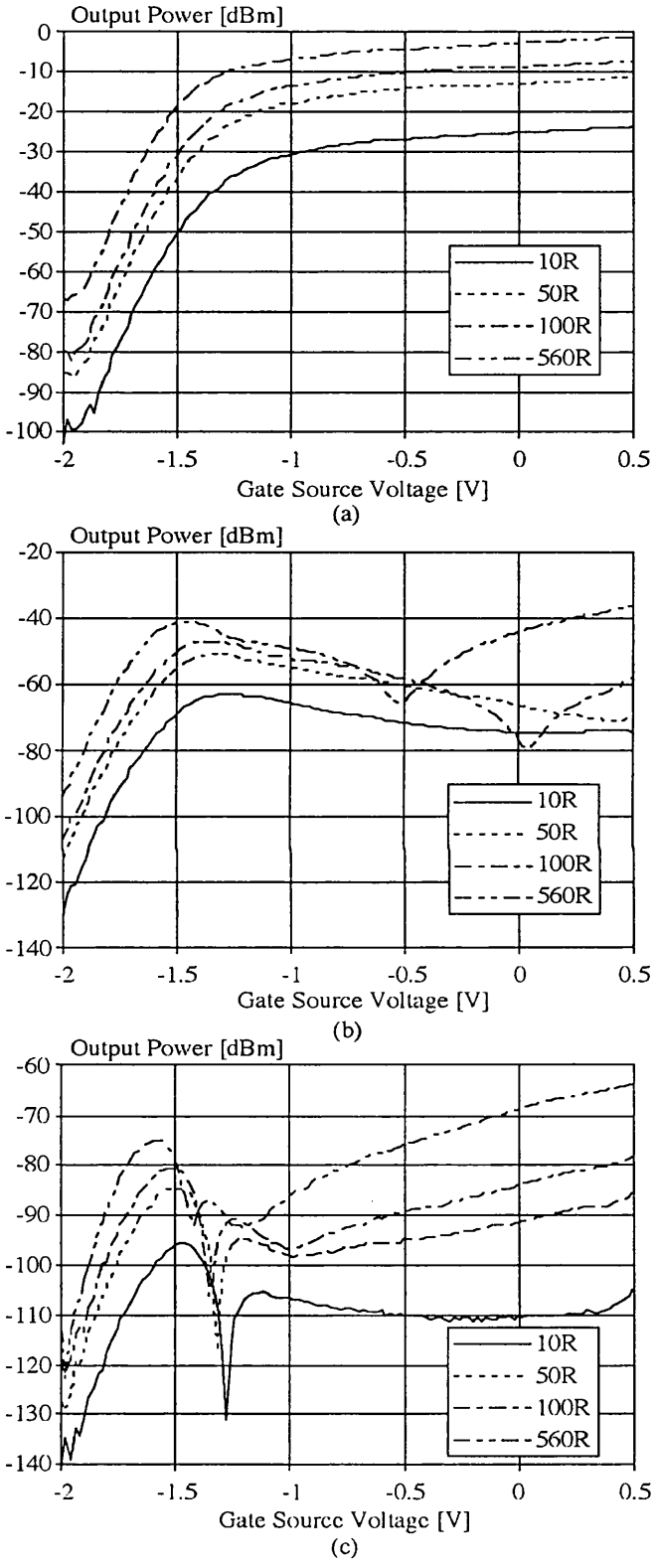


Figure 7.4: Measured effect of load resistance on a 600 μm F20 GaAs MESFET; (a) Fundamental, (b) IMD2 and (c) IMD3.

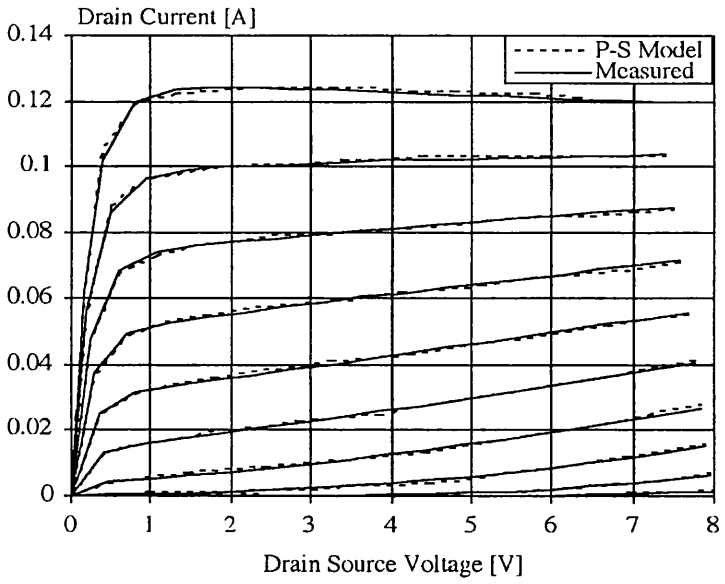


Figure 7.5: DC I-V fit of the Parker Skellern model to the 6x100 μm F20 GaAs MESFET. Gate bias is swept from -2 V to +0.5 V in 0.25 V steps.

IMD2 notch.

7.2.1.1 DC TDFD Parker Skellern Model Extraction

It is now necessary to extract a Parker Skellern model for this device [9], [10], [11], [12]. The FET FIT 7.4 package [13] was used to extract a model according to the DC measurement data. One way of extracting a model using FET FIT is to have DC measurement data and also RF transconductance, g_m, and output conductance, g_{ds}, values. RF distortion measurements carried out for this device for two values of load resistance enabled us to calculate the RF g_m and RF g_{ds} of the device using the technique described in Section 5.3.1. FET FIT 7.4 was used to obtain a Parker Skellern model. The V_{st} parameter in the Parker Skellern model had to be changed in order to get a reasonable fit to the measured data. An example of the DC fit to the measured data is shown in Figure 7.5.

It can be seen from Figure 7.5 that the model gives a very good fit of the DC I-V behaviour.

7.2.1.2 Parker Skellern Model Based on Pulsed I-V Measurements

Another way of extracting a model for a device using FET FIT [13] is to use the measured DC data together with pulsed I-V measurement data [17]. The characterisation results of a 3x100 μm F20 GaAs MESFET obtained with the Advanced

Pulsed Semiconductor Parameter Analyser (APSPA) developed at Macquarie University, Sydney, were used for pulsed I-V model fitting in FET FIT 7.4. 1 μs pulse times and 1 ms pauses between pulses were used for the pulsed I-V measurement. The quiescent points ranged from 0 to 4 V V_{DS} in 1 V steps and -2 to 0 V V_{GS} in 0.25 V steps. The pulsed I-V data ranged from 0 to 8 V V_{ds} and -2 to 0.4 V V_{gs}. FET FIT 7.4 was used to extract and study the fit of the Parker Skellern model to the measured data. The Parker Skellern model parameters for the 3x100 μm F20 GaAs MESFET are presented in Table 7.1.

Table 7.1: Parker Skellern model parameters of a 3x100 μm GaAs F20 MESFET.

General I-V Curves			Rate and History Dependance		
Triode Region			LF Electrostatic Feedback		
Beta [A]	VTO [V]	P	LFGAM	LFG1 [V^{-1}]	LFG2 [V^{-1}]
0.00015	*-1.215*	*2.788*	*0.031*	*0.021*	*0.008*
Knee Region			HF Electrostatic Feedback		
XI	MXI	Z	HFGAM	HFG1 [V^{-1}]	HFG2 [V^{-1}]
0.237	*0.01*	*4.433*	*0.104*	*0.037*	*0.011*
Saturated and Subthreshold			HF Transconductance Drop		
Q	VST	MVST [V^{-1}]	HFETA	HFE1 [V^{-1}]	HFE2 [V^{-1}]
2.193	*0.119*	*0.005*	*0.030*	*0.036*	*0.046*
Contact Resistance			Time Constants and Self Heating		
RS [Ω]	RD [Ω]		TAUG [s]	TAUD [s]	DELTA [W^{-1}]
830	*830*		*1E-4*	*1E-5*	*70.453*

An example of pulsed I-V fit is shown in Figure 7.6.

It can be seen from Figure 7.6 that the model is considerably overestimating the drain current in the knee region. This predicts a larger V_{DS} swing than that measured. Therefore, the output power is overestimated by the model and hence, a different 1 dB compression point and load line is obtained. This error, due to large signal frequency dispersion, is not fully understood at the present time [4] , [5]. This error will be accounted for in the design.

7.2.2 Preliminary Amplifier Design

The first stage of the design was to choose a realistic operating point. Typically the MMT F20 MESFET has a maximum gate drain voltage of the order of 13 V.

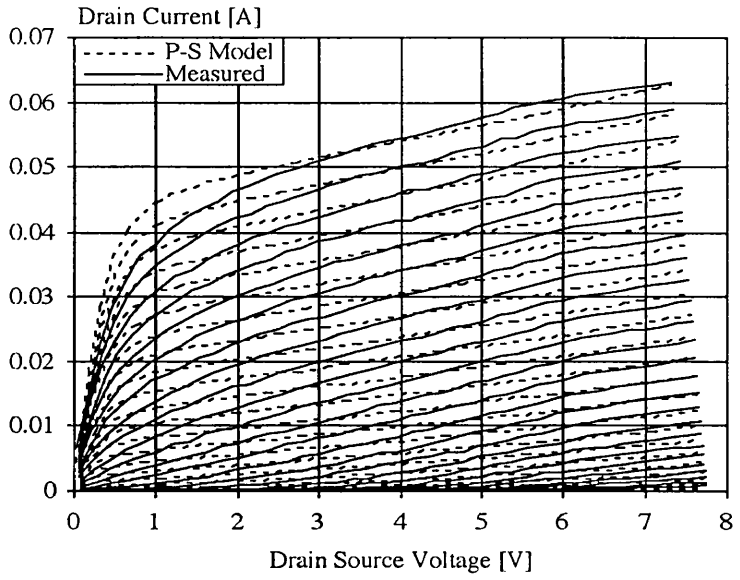


Figure 7.6: Example fit of the Parker Skellern model to the pulsed I-V for a 300 μm GaAs F20 MESFET device. Nominal $V_{GS} = -0.75V$, $V_{DS} = 4V$ and Pulse is 1 μs with 1 ms rest.

A maximum drain voltage of 8 V was chosen to ensure no gate drain breakdown. The amplifier is to operate in a Class A mode, hence, a DC drain bias of 4 V was chosen (with a bias tee at the drain, a Class A amplifier will see an RF drain voltage up to twice the DC drain voltage). For the design to work directly into a 50 Ω load, a maximum current of about 160 mA is needed to realise a load line that is close to maximum possible output power for this drain bias. A width of 6x100 μm was chosen as this gives a peak current of about 120 mA (see Figure 7.1). This ensures that the load line is close to the maximum output power resistance, whilst constraining the load line to be just outside the knee region to reduce the effect of the knee on the derivatives. This was used as the basis of the derivative superposition design and a single FET reference.

7.2.3 Derivative Superposition Design Strategy

As described earlier derivative superposition is the summation (and occasionally subtraction) of the derivatives of FET drain current (with respect to gate source voltage) to achieve a desired nonlinearity. This can be achieved by the parallel connection of several common source FETs of different gate widths and gate bias points with AC coupled gates and sharing a common drain connection. Previously in [2] the authors designed the circuit to have low small signal 3rd order distortion

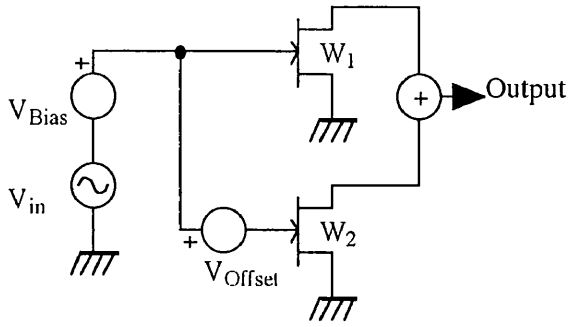


Figure 7.7: The block diagram of the derivative superposition amplifier.

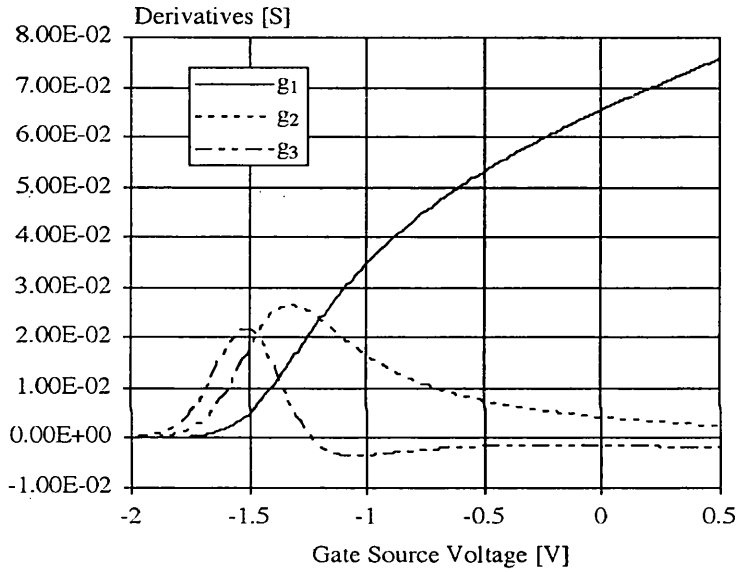


Figure 7.8: The bias dependent derivatives of a single FET.

at and around the quiescent point in order to minimise 3rd order intermodulation distortion (IMD3) for a range of signal amplitudes.

An alternative approach proposed here is to design the circuit not to reduce the magnitude of the 3rd derivative of drain current with respect to gate source voltage (the g_3 derivative) at the quiescent point, but to introduce a region of opposite sign around the quiescent point. The proposed block diagram of the derivative superposition amplifier is shown in Figure 7.7.

It can be seen from Figure 7.7 that only two FETs are used in the amplifier circuit in order to have the simplest possible structure for the derivative superposition circuit. Super Deriv simulations [13] were carried out to investigate the behaviour of such a circuit. The bias dependent derivatives of the reference device are shown in Figure 7.8.

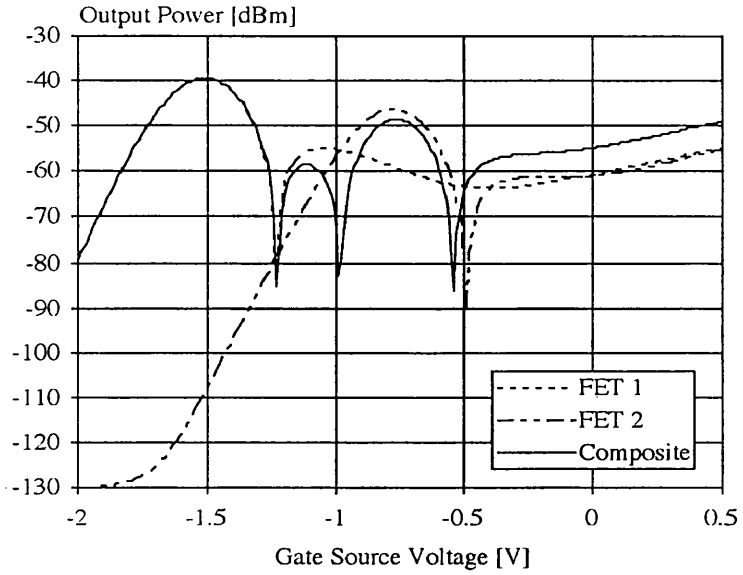


Figure 7.9: The bias dependent small signal 3rd order distortion of the single FETs and the composite structure.

It can be seen from Figure 7.8 that there exists a region on the IMD3 curve where distortion is low for a wide range of bias points. The idea is to add a secondary device so that the positive peak of the g_3 of this device will cut through the low g_3 derivative region of the main device giving a low IMD3 region with two nulls. For a two FET sign reversal DS amplifier, Figure 7.9 shows the variation of small signal 3rd order distortion (which is proportional to the magnitude of the g_3 derivative) arising from each FET and for the composite amplifier; the quiescent point is $V_{GS} = -0.75V$; an amplitude scale in dB is now used.

The sharp null in small signal distortion with gate bias indicates where the sign of the g_3 derivative reverses. To understand its operation it is necessary to use the concept of a time dependent derivative which was previously used to apply Volterra analysis to mixers in [18] , [19].

Figure 7.10(a) shows the 3rd derivative of drain current (g_3) with respect to gate source voltage. It can be seen from Figure 7.10(a) that there exist a region of opposite sign around the quiescent point. Under small signal excitation, the g_3 derivative is essentially time invariant and finite as shown in Figure 7.10(b). As the level of excitation is increased, the peaks of the signal pass into the two adjoining regions where the derivative has an opposite sign. This results in a time varying derivative as shown in Figure 7.10(c). For large signals, the signal will spend much of the time in the surrounding regions of opposite sign, essentially reversing the polarity of the derivative. Depending on the waveform and the g_3

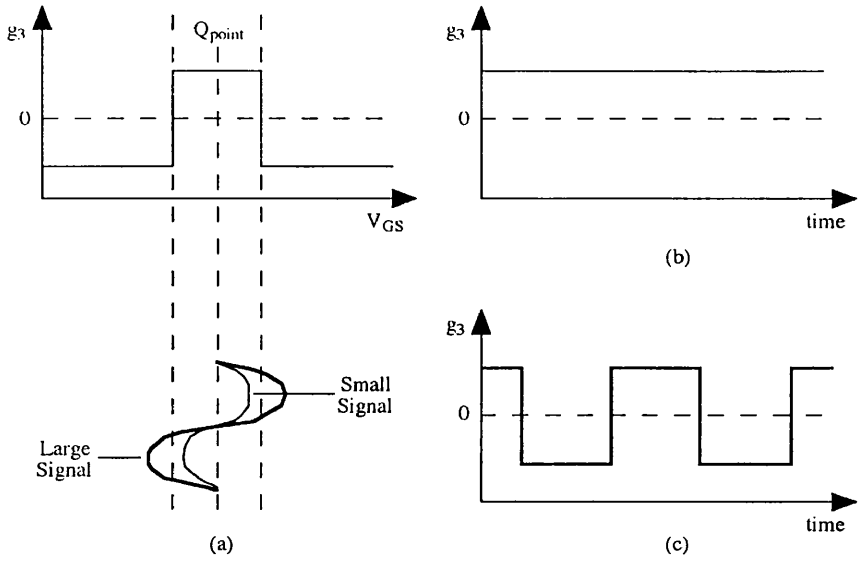


Figure 7.10: (a) Idealised variation of the 3rd derivative of drain current, g_3, with gate source voltage for the DS power amplifier around its quiescent point. (b) Variation of g_3 with time under small signal excitation. (c) Variation of g_3 with time under large signal excitation.

derivative shape, there will exist an amplitude where the average of this time varying g_3 derivative is zero, leading to zero 3rd order intermodulation distortion at this signal amplitude.

In the case of the distortion nulling form of DS [2] it was necessary to determine the FET nonlinearity to a high degree of accuracy to obtain a correct design. The sign reversal technique requires only a region of opposite sign to exist for correct operation. This can lead to a relaxation on the required CAD model accuracy, allowing working designs to be obtained with existing CAD models providing they describe the soft pinch off behaviour such as [20] and [21]. These CAD models could not be used with the nulling technique of [2] with any confidence of success with frequency dispersive FET technologies.

Having considered some of the fundamental issues in this design, next we present the detailed steps carried out in the MMIC design of the derivative superposition power amplifier.

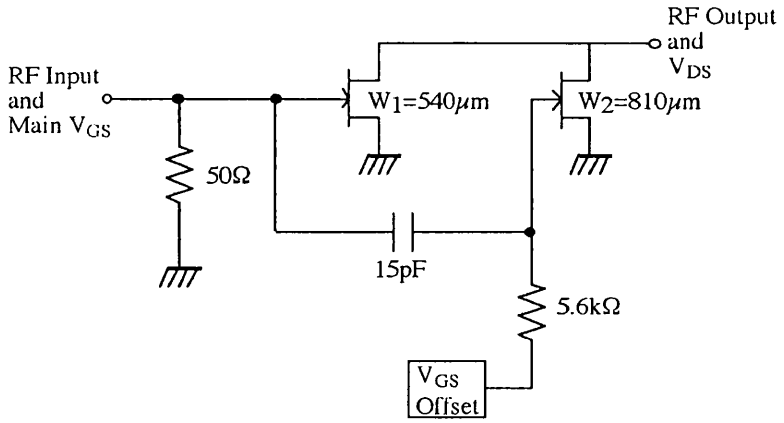


Figure 7.11: The schematic diagram of the derivative superposition amplifier.

7.2.4 MMIC Power Amplifier Design

7.2.4.1 Detailed Design Using Super Deriv

The schematic diagram of the derivative superposition amplifier is shown in Figure 7.11.

Using the UCL Super Deriv 4.0 package [13], the derivative superposition design was carried out. Load resistance value of 50 Ω, drain bias of 4 V and reference device gate width of 600 μm were chosen, as described previously. It is now necessary to find the optimum gate bias for the devices and also the secondary device gate width. The simulated small signal distortion along the load line for this device on its own is shown in Figure 7.12.

From Figure 7.12 peaks in the 2nd and 3rd order derivatives can be observed both near pinch off ($\Delta V_{gs} = -1V$) and in the region where gain collapses as the FET is driven into its knee region ($\Delta V_{gs} = 1V$). A gate bias of $V_{GS} = -0.75V$ was chosen to almost centralise the quiescent point between these two regions of high distortion.

Next, a secondary device is to be added in order to align the positive peak of the g_3 derivative of the secondary device on top of the low g_3 derivative region of the main device. The simulated small signal 3rd order distortion along the load line for the reference device and the composite device is shown in Figure 7.13.

This arrangement causes a phase reversal which in turn causes a deep null in IMD3 in the power sweep. This is shown in Figure 7.14.

Generation of the sign reversal in the 3rd order derivative is more difficult for load resistance values above that for which maximum output power occurs. This led to a design with a secondary device having a DC offset of -0.75 V from the

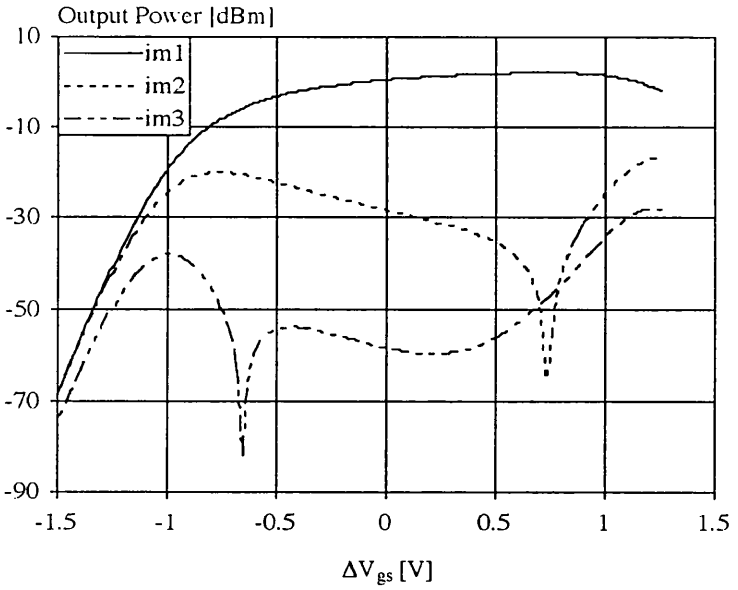


Figure 7.12: Simulated small signal distortion along the load line for a single 6x100 μm F20 GaAs MESFET. $V_{GS} = -0.75V$, $V_{DS} = 4V$ and $R_{Load} = 50$.

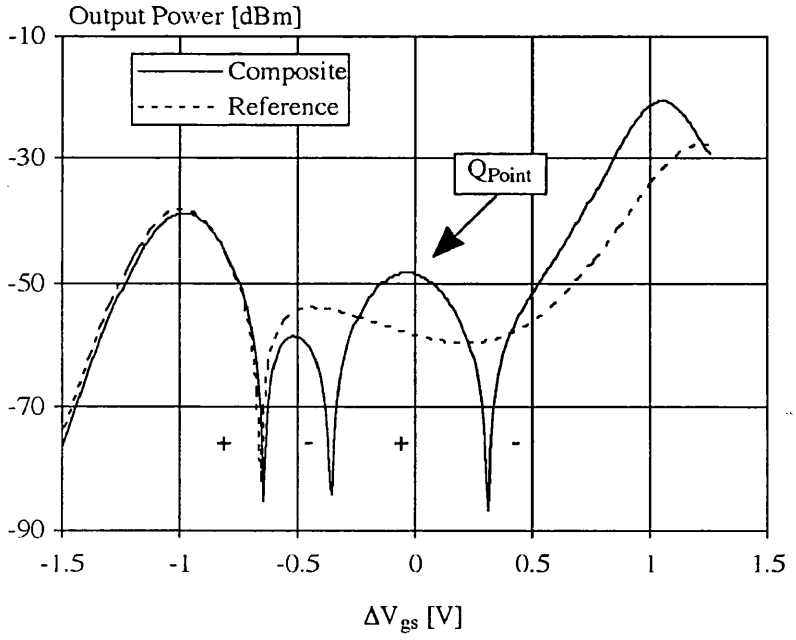


Figure 7.13: Simulated small signal 3rd order distortion along the load line for the single FET and the composite structure. $V_{GS} = -0.75V$, offset= $-0.75V$, $V_{DS} = 4V$ and $R_{Load} = 50\Omega$. The gate width of the first FET is 540 μm and the gate width of the second FET is 810 μm.

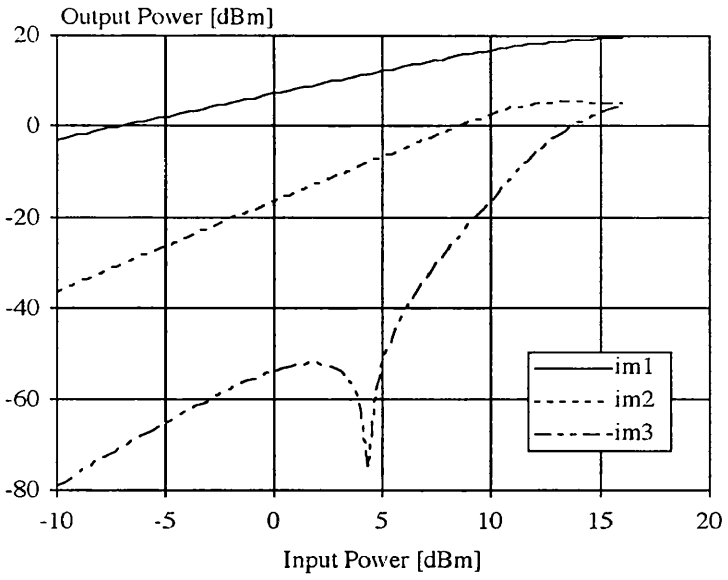


Figure 7.14: Simulated power sweep of the composite structure. $V_{GS} = -0.75V$, offset= $-0.75V$, $V_{DS} = 4V$ and $R_{Load} = 50\Omega$.

bias of the reference FET. The area of the secondary device was chosen to be 1.5 times greater than that of the area of the main device to ensure correct operation of the fabricated circuit. It was noted that further increasing the gate width of the secondary device moved the distortion null to higher power levels. However, the improvement became asymptotic at gate widths greater than 2.5 times the reference device. The simulation of the small signal 3rd order distortion of the composite circuit as a function of input signal power for various secondary device gate widths is shown in Figure 7.15.

In this design it was decided to use a secondary device of gate width 1.5 times of that the reference device to achieve a reasonable compromise between circuit performance and overall chip area. The secondary device is approximately pinched off at the quiescent point (hence the quiescent power dissipation is only increased slightly) and operates as a Class B amplifier in parallel with the main FET which operates as a weak Class AB amplifier. The design was normalised to give the same small signal gain as the 6x100 μm single FET reference. This led to FET gate widths of 540 μm and 810 μm. The design was then checked using SPICE3F4.

7.2.4.2 Spectral Regrowth Simulations

Simulation of the spectral regrowth for the reference device and for the composite circuit were carried out using Super Deriv [13]. The composite circuit at 1 dB compression point did not show any significant improvement over the reference

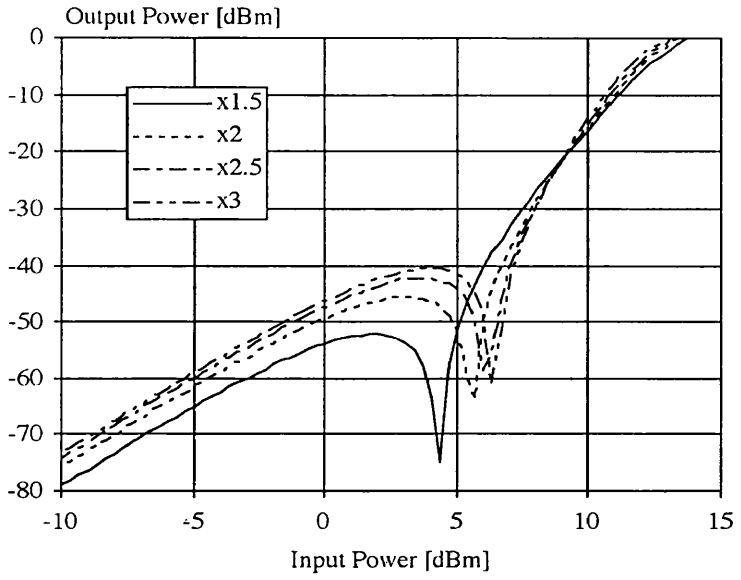


Figure 7.15: Simulated small signal 3rd order distortion of the composite circuit for various secondary FET gate widths.

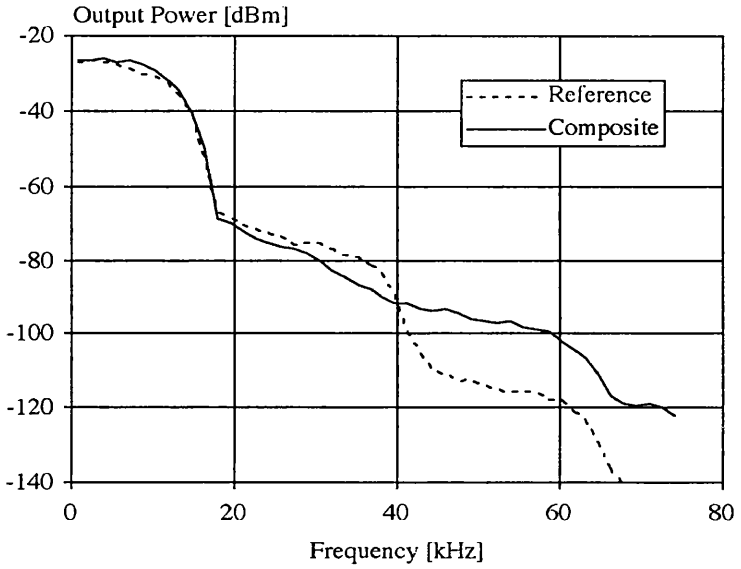
device. However, the spectral regrowth simulations for the composite circuit at several dBs of back-off from the 1 dB compression point showed a considerable improvement over the reference device. The spectral regrowth plots at 2 dB and 4 dB back-off from the 1 dB compression point are shown in Figure 7.16(a) and (b), respectively.

It can be seen from Figure 7.16(a) and (b) that a significant reduction of adjacent channel interference is obtained by the composite circuit, however, the distortion in the next to adjacent channel due to 5th order nonlinearity is increased but is still below the adjacent channel level.

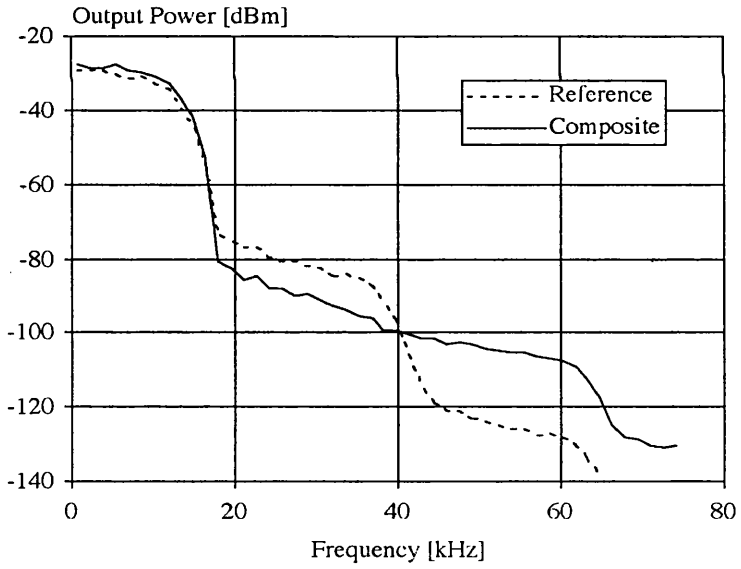
In Figure 7.17(a) and (b) we show the contour plots of the spectral regrowth for the reference device and the composite circuit as a function of frequency and input power, respectively.

We approximate the adjacent channel power ratio (ACPR) defined in Section 2.3.1.2 of this thesis by taking spot frequencies in the channel (0.781 kHz) and next to adjacent channel (35.156 kHz) of Figurers 7.17(a) and (b). The ACPR simulations for the reference device and for the composite circuit are compared in Figure 7.18.

It can be seen from Figure 7.18 that the composite circuit offers a significant improvement in the ACPR over the reference FET for a wide range of output power spectral density in the pass band.

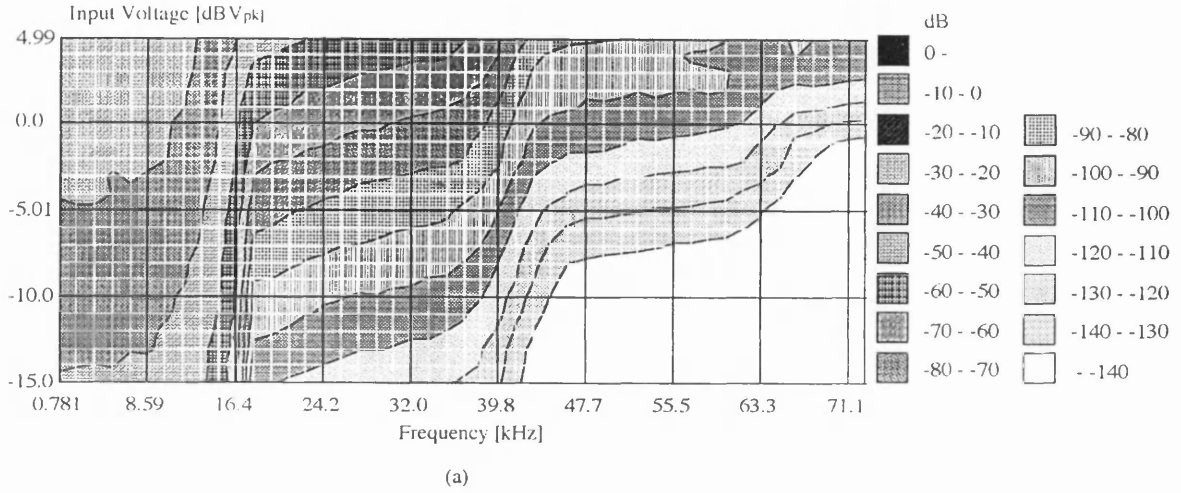


(a)

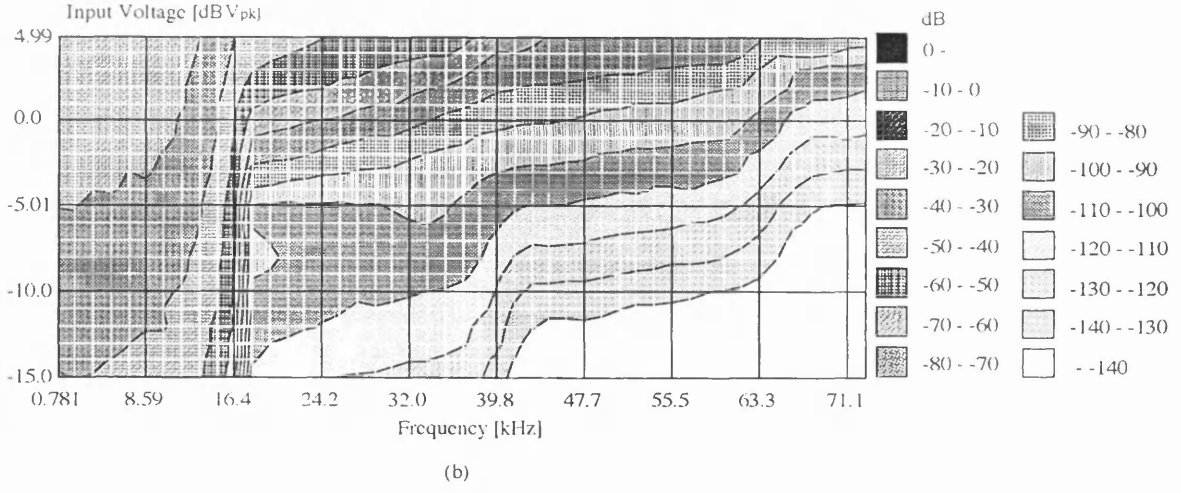


(b)

Figure 7.16: Simulated spectral regrowth comparison of the reference FET and the composite circuit; (a) at 2 dB back-off from 1 dB compression point and (b) at 4 dB back-off from 1 dB compression point.



(a)



(b)

Figure 7.17: Simulated contour plots of the spectral regrowth for the reference FET and the DS amplifier; (a) reference FET and (b) composite circuit. 1 dB compression points of the reference FET and the composite circuit are 10.6 dBm and 12.0 dBm, respectively.

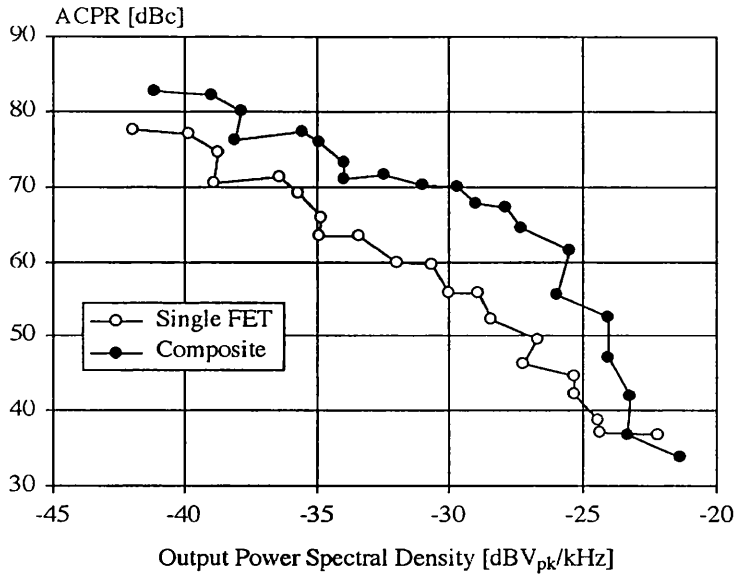


Figure 7.18: Simulated ACPR of the reference FET and the DS amplifier.

7.2.5 MMIC Layout

A photograph of the prototype MMIC design is shown in Figure 7.19. The chip dimensions are 961 μm x 764 μm. The RF input port is on the left hand side of the layout. This also provides the gate bias for the lower MESFET (the Class AB FET). To allow flexibility to test over a wide range of frequencies and bias conditions, no matching networks were used on the prototype MMIC. Instead a 50 Ω resistor was used at the gate to provide a wideband RF input termination. The upper MESFET (the class B FET) is AC coupled to the RF input through a 15 pF SiN capacitor. Its gate bias is applied through a DC pad and a 5 kΩ resistor. The drains of the FETs are connected to provide the required current summation. The RF output port is on the right hand side.

7.2.6 Measured Performance

In this section we present measured results on the MMIC. The set-up for 2 tone intermodulation distortion measurement using 20 MHz and 29.3 MHz signals is as described in Section 4.3.3 and the measurement set-up using 470 MHz and 480 MHz signals is as described in Section 4.4. Measurements made include gain, single and two tone efficiency, 3rd order intermodulation distortion, frequency response, and also the effect of load resistance, drain bias and offset voltage on distortion.

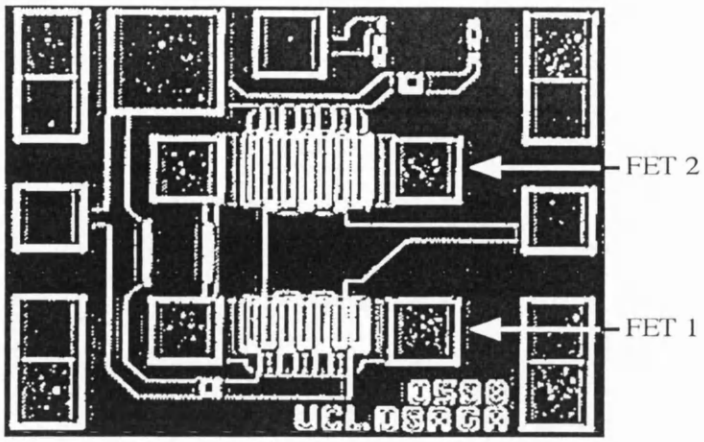


Figure 7.19: Photograph of the MMIC DS power amplifier.

7.2.6.1 Gain

In this section we compare the large signal performance of a 6x100 μm reference MESFET with the derivative superposition composite amplifier measured at 480 MHz. The single FET and the main FET of the composite are operating in a weakly Class AB mode (the pinch off voltage is -1.55 V). Figure 7.20 shows the measured variation of gain with output power for the two amplifiers.

At low signal levels the DS amplifier has a slightly better gain than the reference FET. The composite amplifier gives a significantly higher gain at high output power.

7.2.6.2 Single Tone Efficiency

In Figure 7.21 we compare the measured efficiency at 480 MHz of the composite amplifier with that of a single FET.

It can be seen from Figure 7.21 that the composite circuit does not offer any efficiency advantage over the reference FET.

7.2.6.3 3rd Order Intermodulation Distortion

In Figure 7.22 we show contour plot of the magnitude of the 2 tone 3rd order intermodulation distortion (IMD3) measured at 20 MHz and 29.3 MHz as a function of input bias voltage and input signal power for both the single FET reference and the derivative superposition power amplifier.

The positive peak in the 3rd order derivative with bias occurring in the soft pinch off region in Figure 7.8appears as a ridge (SPR) in Figure 7.22(a). Similarly the zero crossing in the soft pinch off region in Figure 7.8appears as a valley (SPV)

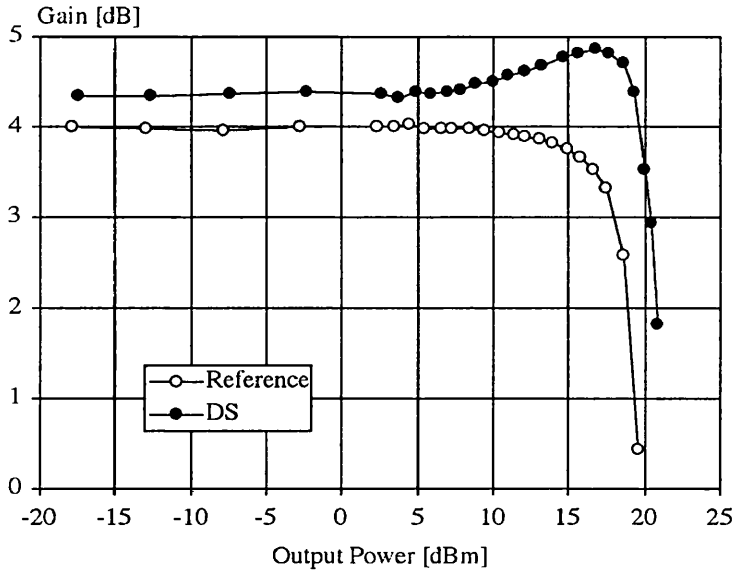


Figure 7.20: Measured variation of gain as a function of output power for the reference FET and the derivative superposition amplifier.

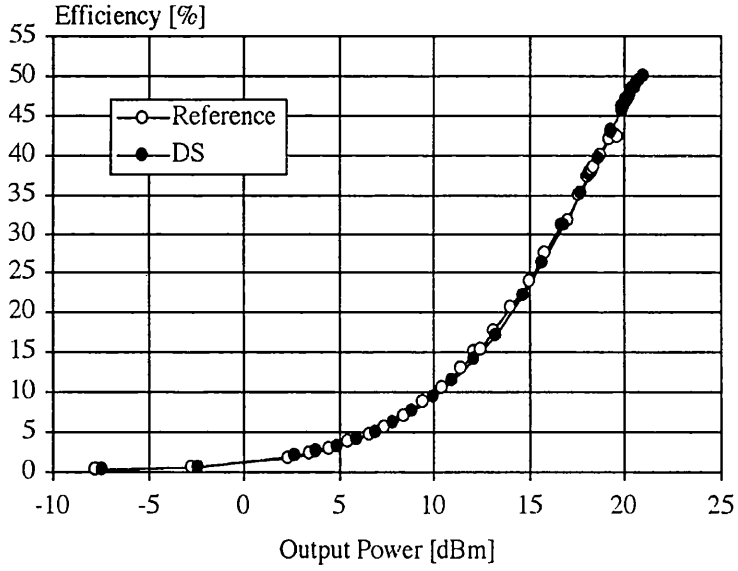
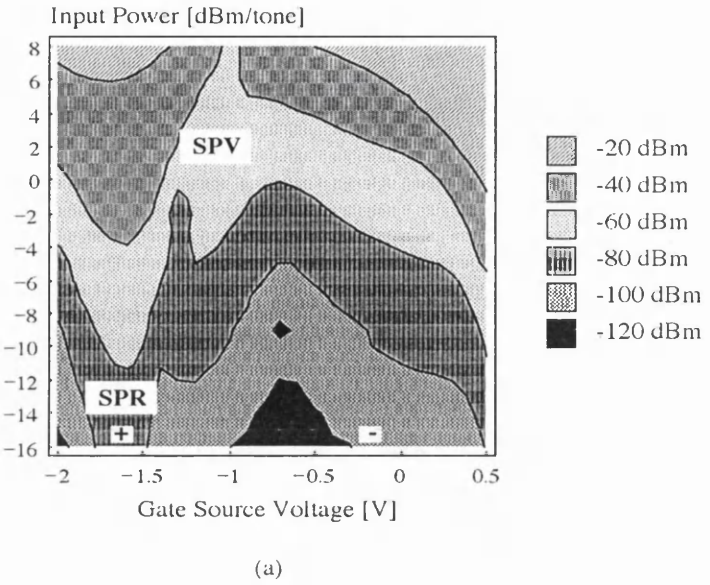
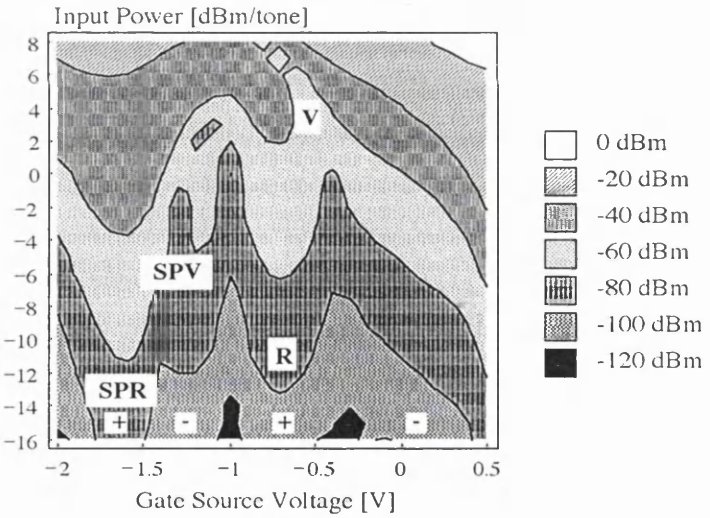


Figure 7.21: Measured single tone efficiency as a function of output power for the reference FET and the derivative superposition amplifier.



(a)



(b)

Figure 7.22: Measured contour plot of the 3rd order intermodulation distortion with gate source voltage and input power level; (a) reference FET and (b) derivative superposition amplifier. $V_{GS} = -0.75V$, offset$= -0.8V$, $V_{DS} = 4V$ and $R_{Load} = 50\Omega$.

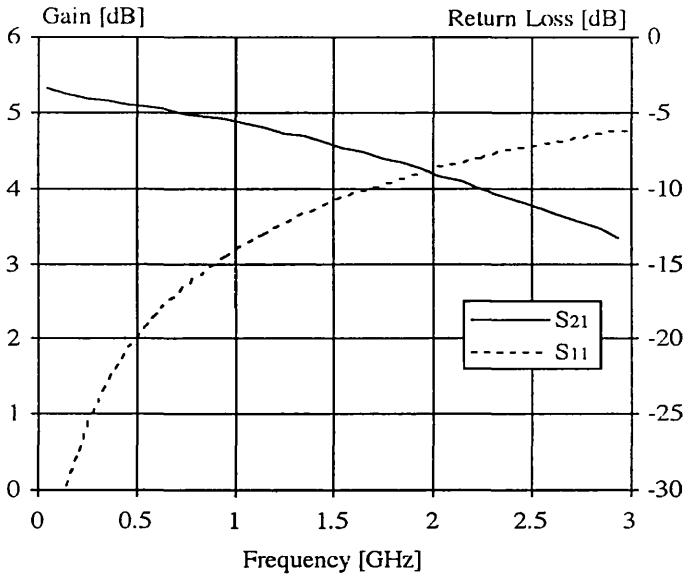


Figure 7.23: Measured frequency response of the derivative superposition amplifier.

in Figure 7.22 (a). As the power is increased the location of the SPV valley moves to an increasing gate voltage causing it to curl to the right. This feature remains strongly bias dependent and hence relatively sensitive to drift.

These features are also visible in the derivative superposition amplifier in Figure 7.22 (b). The island where the derivatives has an opposite sign to the surrounding area in Figure 7.9 appears as a ridge (R) at low input powers in Figure 7.22(b). As the input power increases, the distortion null to the right of the ridge curls to the left, giving a notch in distortion for large signals at the gate bias where the ridge (R) occurs for low signals. This region is shown by a letter V in Figure 7.22(b). The relatively strong curvature with gate bias means that this feature is relatively insensitive to bias drift than the null generated by the class AB operating point (see Figure 7.22(a)).

7.2.6.4 Frequency Response

In Figure 7.23 we show the frequency response of the DS amplifier. It can be seen from Figure 7.23 that the DS amplifier provides a gain of at least 4.5 dB and an input return loss of better than 14 dB up to 1 GHz.

The response of the DS amplifier can easily be improved by using matching networks. A possible off chip matching network based on lumped elements and transmission lines for the DS power amplifier is presented in Figure 7.24. The parameter values for the matching network are given in Table 7.2.

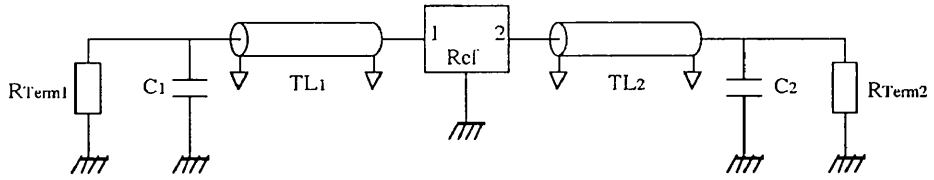


Figure 7.24: A possible off chip matching network for the DS power amplifier.

Table 7.2: Parameter values of the matching network for the DS power amplifier.

Transmission Lines				Resistors		Capacitors	
Par.	Z[Ω]	E[°]	f[GHz]	Par.	Value[Ω]	Par.	Value[pF]
TL_1	142.47	90	9.97	R_{Term1}	50	C_1	1.77
TL_2	70.00	90	10.00	R_{Term2}	50	C_2	0.25

The response of the DS amplifier with the matching network is shown in Figure 7.25. It can be seen from Figure 7.25 that an almost flat gain (i.e. a ripple of less than 0.25 dB) with an input return loss of better than 16.5 dB can be achieved up to 2.3 GHz.

7.2.6.5 Effect of Load Resistance on Distortion

In Figure 7.26(a), (b) and (c) we show the contour plots of the 3rd order intermodulation distortion measured at 20 MHz and 29.3 MHz with gate bias and input power for three different load resistance values of 40 Ω, 50 Ω and 63.5 Ω, respectively.

It can be seen from Figure 7.26 that increasing the load resistance moves the generated IMD3 null to more negative gate source voltages. In Figure 7.27 we show the carrier to interference ratio (c/i) as a function of output signal power measured at 20 MHz and 29.3 MHz with the 3 different load resistance values for the reference FET and the DS amplifier.

It can be seen from Figure 7.27 that increase of the load resistance moves the peak in the c/i of the composite circuit to a lower output power level. It can also be seen from Figure 7.27 that the DS amplifier provides substantial improvement in its c/i over the corresponding reference FET for the different load resistance values considered.

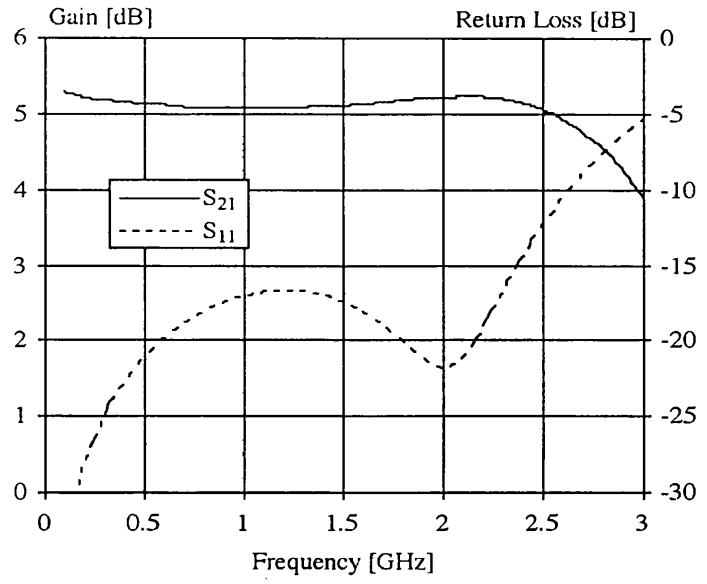


Figure 7.25: Response of the DS power amplifier with the designed matching network.

7.2.6.6 Effect of Drain Bias on Distortion

In Figure 7.28(a), (b) and (c) we show the contour plots of the 3rd order intermodulation distortion measured at 470 MHz and 480 MHz against input power levels and drain bias values of 3.5 V, 4.5 V and 5.5 V, respectively.

In Figure 7.28 it can be seen that increasing drain bias causes considerable reduction of the 3rd order intermodulation distortion.

In Figure 7.29 we show the c/i variation of the reference FET and the DS amplifier measured at 470 MHz and 480 MHz with output power for three different drain bias values. It can be seen from Figure 7.29 that increasing the drain bias from 3.5 V to 5.5 V moves the peak in the c/i of the DS amplifier to a higher value of output power (circa by about 6.5 dB). It can also be seen from Figure 7.29 that the DS amplifier provides a considerable improvement in its c/i over the corresponding reference FET for the different drain bias values considered.

7.2.6.7 Effect of Offset Voltage on Distortion

In Figure 7.30(a), (b) and (c) we show the contour plots of the variation of the magnitude of the 2 tone 3rd order intermodulation distortion (IMD3) measured at 470 MHz and 480 MHz with DC gate bias and input power level for various offset voltages of -0.6 V, -0.7 V and -0.9 V, respectively.

The contour plot of IMD3 for the offset voltage of -0.8 V is the same as the

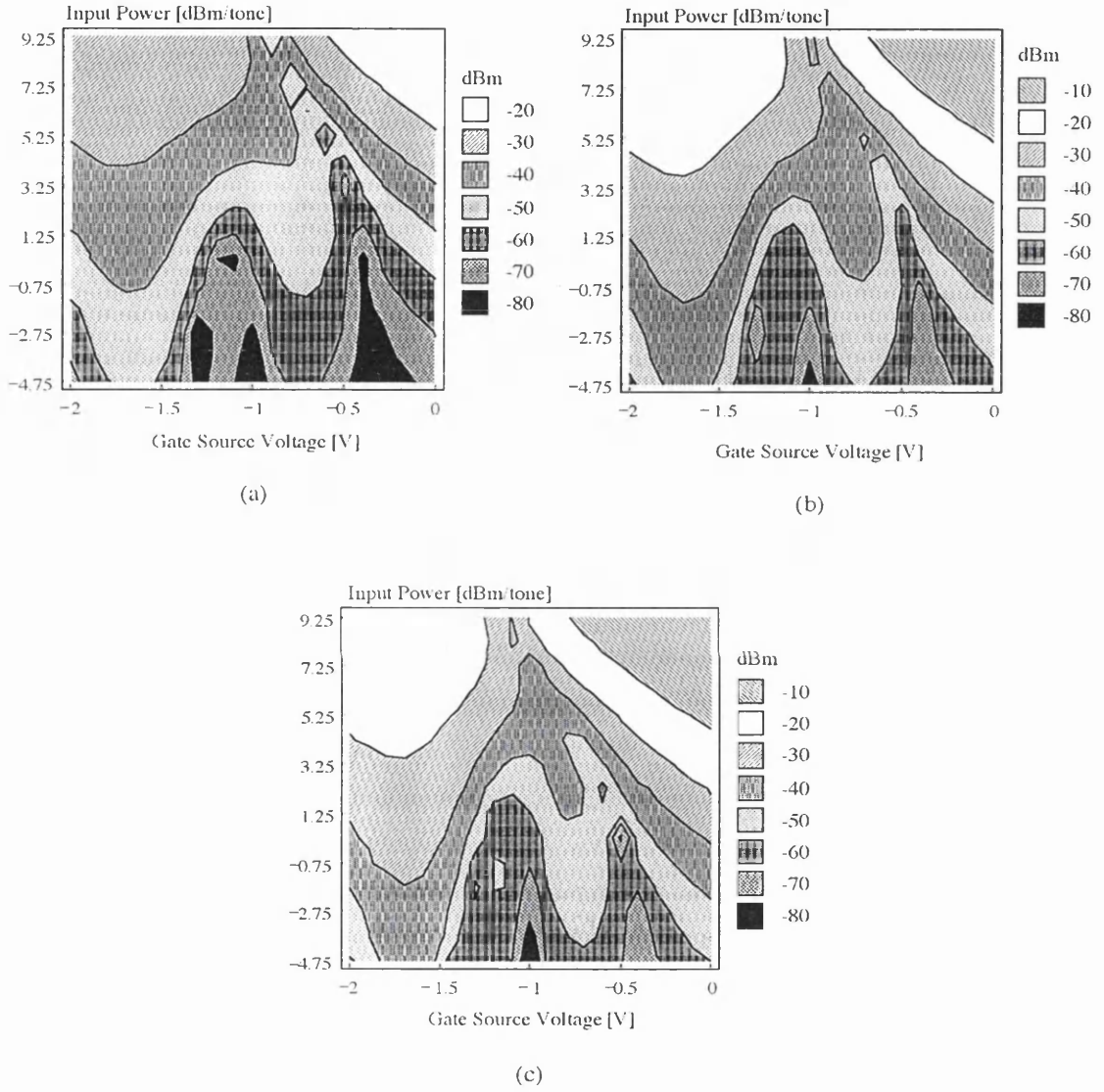


Figure 7.26: Measured contour plot of the 3rd order intermodulation distortion of the derivative superposition amplifier against gate bias and input power levels for different load resistances; $V_{GS} = -0.75V$, offset= $-0.8V$ and $V_{DS} = 4.5V$. (a) $R_{Load} = 40\Omega$, (b) $R_{Load} = 50\Omega$ and (c) $R_{Load} = 63.5\Omega$.

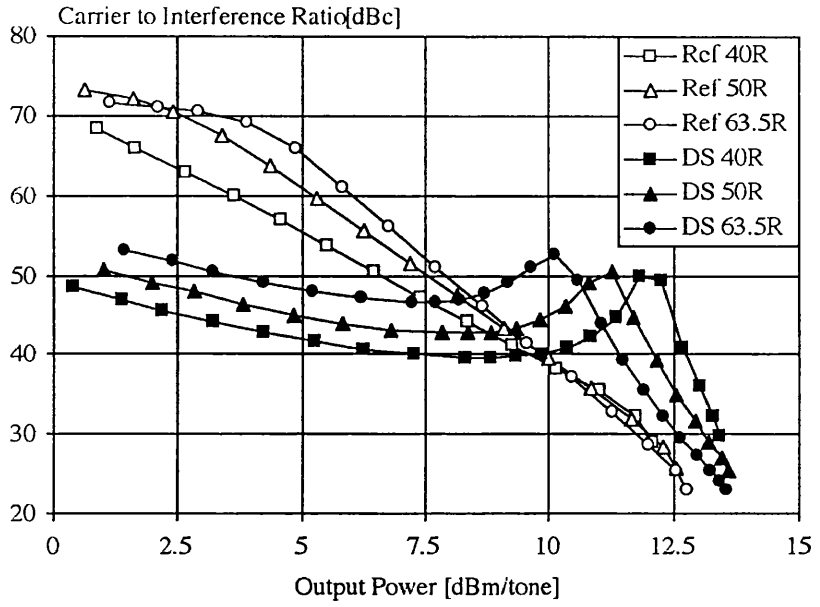


Figure 7.27: Measured two tone (20 MHz and 29.3 MHz) c/i comparison versus output power for the reference FET and the DS amplifier for various load resistance values. $V_{GS} = -0.75V$, offset= $-0.8V$, $V_{DS} = 4.5V$.

one presented in Figure 7.28(b). It can be seen from Figure 7.30 that a higher magnitude of offset value moves the generated IMD3 null to a more positive gate source voltage value.

In Figure 7.31 we show the traces of the nulls in the 3rd order intermodulation distortion with gate bias.

Figure 7.31 confirms that the generated IMD3 null moves to a more positive gate source voltage as the magnitude of the offset voltage is increased.

7.2.6.8 Comparison Indicating Potential Advantage

Not only was it possible to measure the DS amplifier, but it was also possible to operate each FET individually, allowing comparisons with other single FET amplifiers. In Figure 7.32 and Figure 7.33 we show the gain and efficiency responses of the DS amplifier and various forms of the reference FETs.

The design data is defined in the first four columns of Table 7.3.

The designs include the DS amplifier working into a 50 Ω load, FET1 of the DS amplifier operating in class A mode working into a 50 Ω load with FET2 turned off, and FET2 of the DS amplifier operating in class B and AB modes working into a 50 Ω load with FET1 turned off. The use of the same load resistor and drain bias for all designs means that the designs are not all fully optimised but

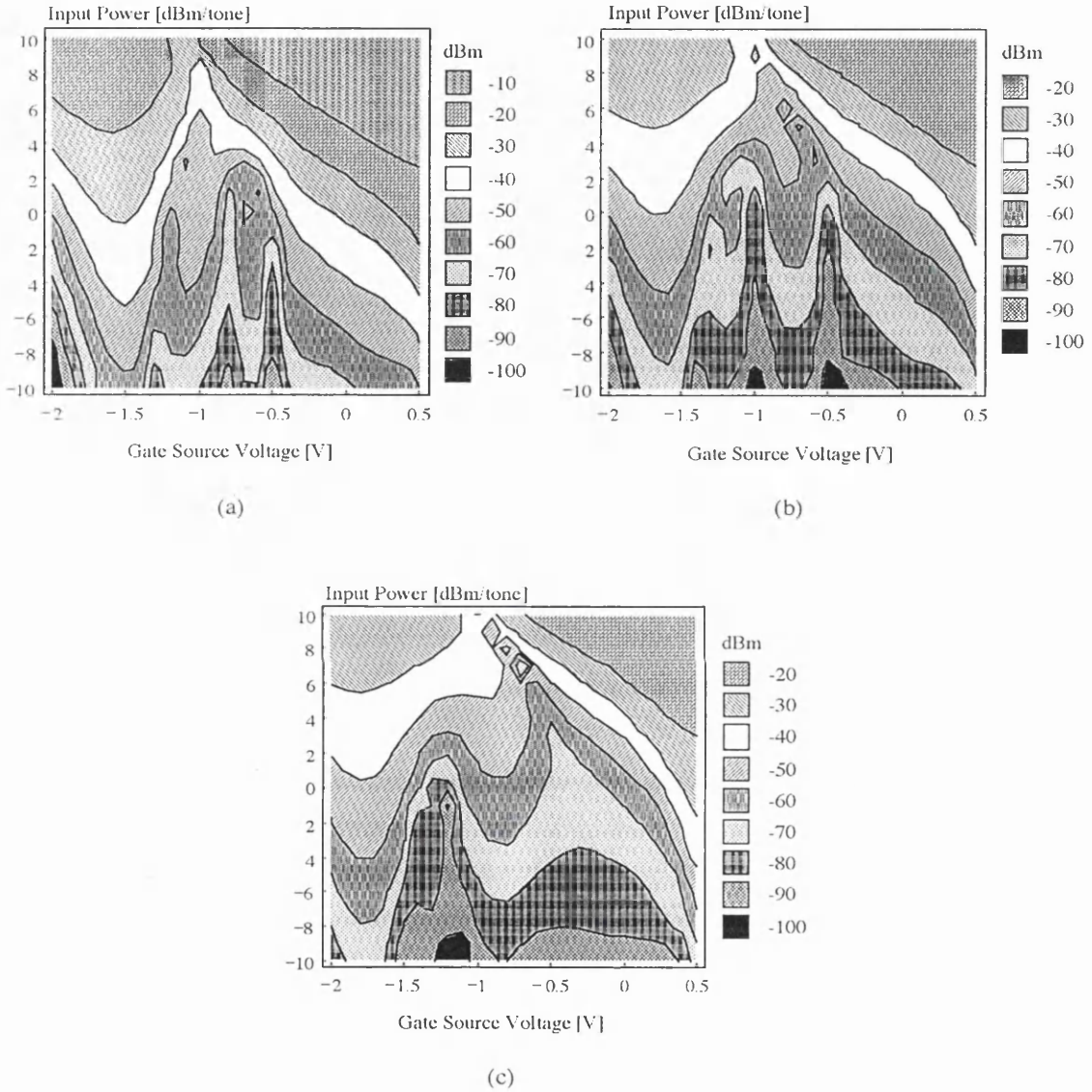


Figure 7.28: Measured contour plot of the 3rd order intermodulation distortion with gate bias and input power levels for different drain bias values for DS amplifier; $V_{GS} = -0.75V$, offset= $-0.8V$ and $R_{Load} = 50\Omega$. (a) $V_{DS} = 3.5V$, $V_{DS} = 4.5V$, and $V_{DS} = 5.5V$.

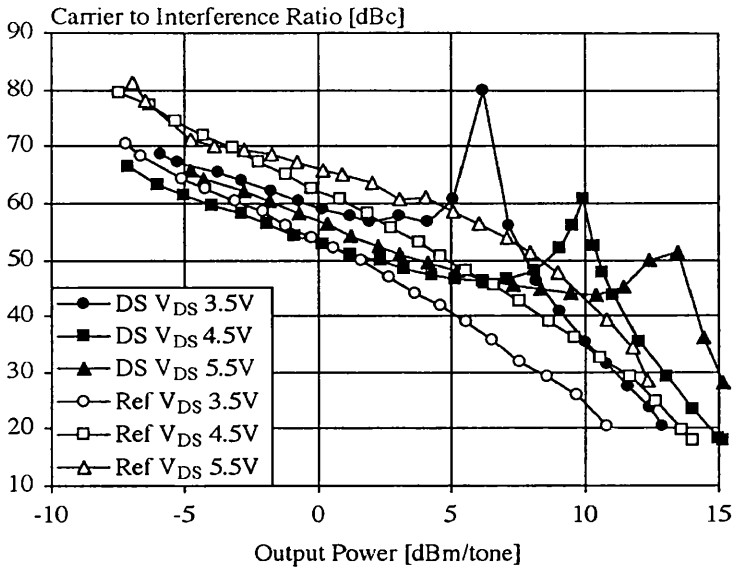


Figure 7.29: Measured two tone (470 MHz and 480 MHz) c/i comparison versus output power for the reference FET and the composite circuit for various V_{DS} values; $V_{GS} = -0.75V$, offset $= -0.8V$ and $R_{Load} = 50\Omega$.

the results are considered representative.

The measured carrier to interference ratios (c/i) for the designs are presented in Figure 7.34.

It can be seen from Figure 7.34 that the DS amplifier produces a strong peak at high output power in the c/i plot as expected. The class A amplifier and the class B amplifier did not produce any peaks in the c/i plot. The class AB amplifiers have weak peaking effects in the c/i curves but the position of these peaks are not easily controllable (i.e. they vary strongly with gate bias).

In order to have a better assessment of amplifier performance, the measured output referred 1 dB compression points (single tone at 0.48 GHz and two tones at 0.47 GHz and 0.48 GHz) for the designs were measured and they are presented in Table 7.3. Due to the limitation of the test equipment (i.e. maximum signal powers of the generators were not high enough) and the shape of the curves for the class B and AB1 amplifiers, their 1 dB compression points could not be determined precisely and approximate values were extrapolated from the measured data. For the amplifiers exhibiting gain enhancement, we define 1 dB compression as being 1 dB below the peak gain. Table 7.3 also summarises the single tone and two tone efficiencies for each of the five amplifiers.

To illustrate the potential advantage of the DS circuit we consider a hypothetical example which requires a minimum two tone c/i ratio of 45 dBc over a

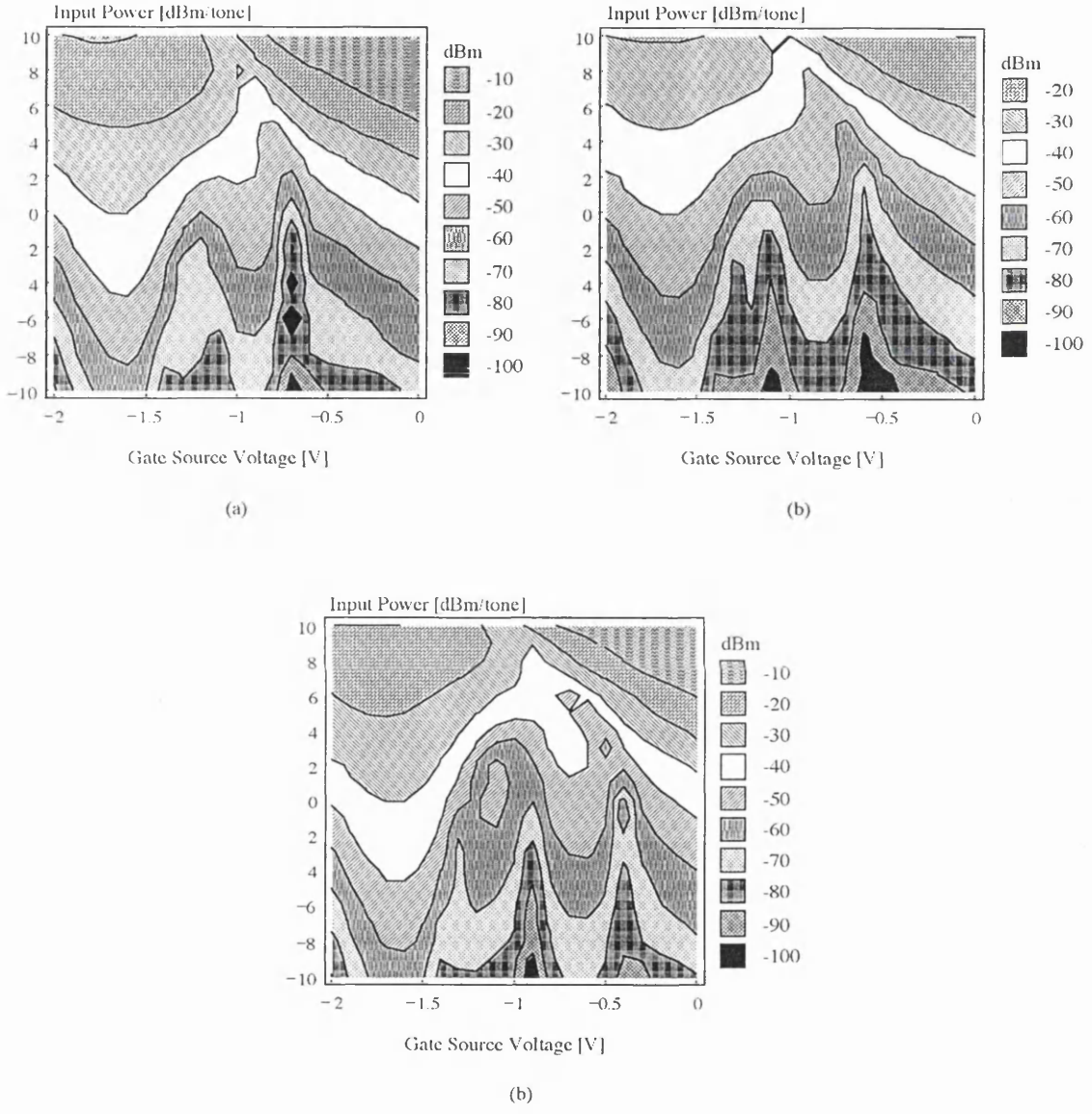


Figure 7.30: Measured contour plots of the 3rd order intermodulation distortion with gate bias and input power levels for various offset voltages; $V_{GS} = -0.75V$, $V_{DS} = 4.5V$ and $R_{Load} = 50\Omega$; (a) offset voltage of -0.6 V, (b) offset voltage of -0.7 V and (c) offset voltage of -0.9 V .

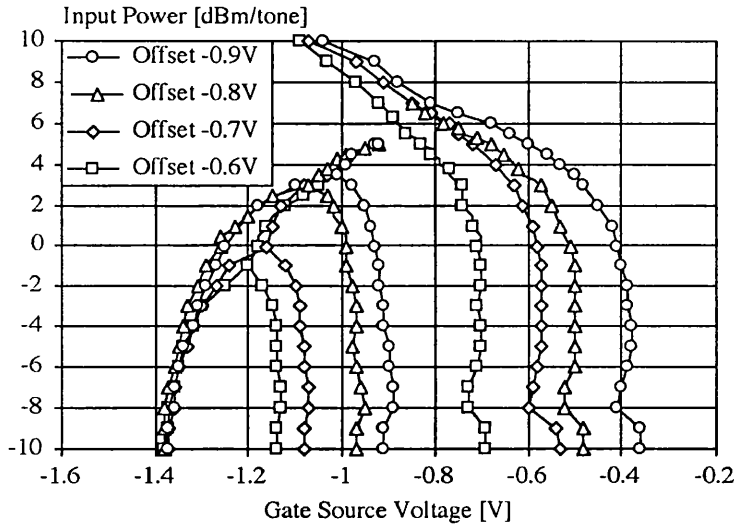


Figure 7.31: Measured traces of the null in the 3rd order intermodulation distortion of the DS amplifier for various offset voltages. $V_{GS} = -0.75V$, $V_{DS} = 4.5V$ and $R_{Load} = 50\Omega$.

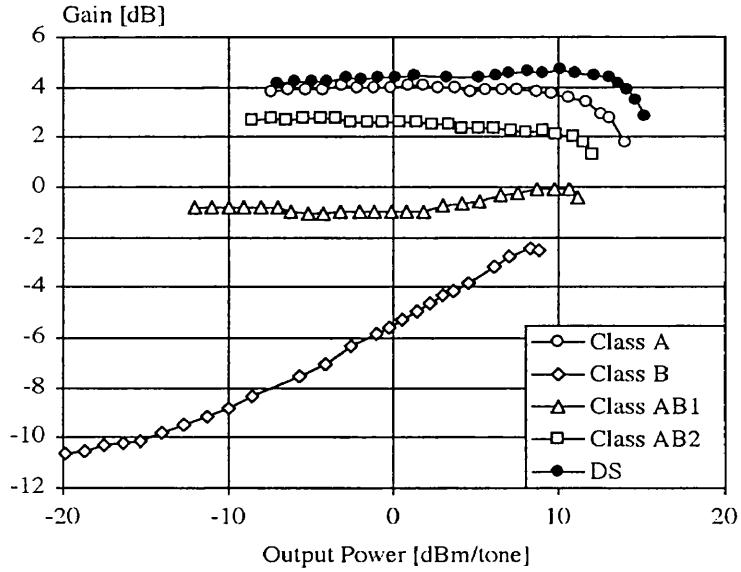


Figure 7.32: Measured gain comparison of the DS amplifier and various forms of the reference FETs against output power levels. Drain bias is 4.5 V and load resistance is 50 Ω. Gate source voltages of the amplifier A, AB2, AB1 and B are -0.75 V, -1 V, -1.25 V and -1.55 V, respectively. V_{GS} of DS is -0.75 V and its offset is -0.8 V.

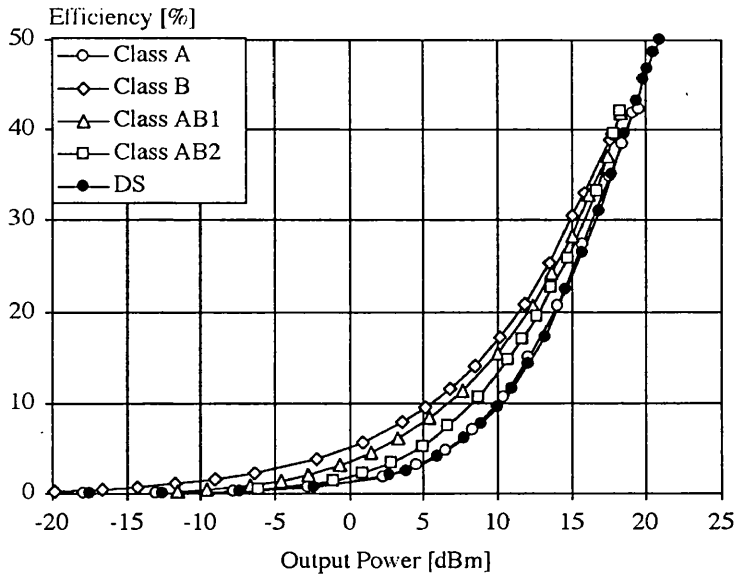


Figure 7.33: Measured efficiency comparison of the DS amplifier and various forms of the reference FETs against output power levels. Drain bias is 4.5 V and load resistance is 50 Ω. Gate source voltages of the amplifier A, AB2, AB1 and B are -0.75 V, -1 V, -1.25 V and -1.55 V, respectively. V_{GS} of DS is -0.75 V and its offset is -0.8 V.

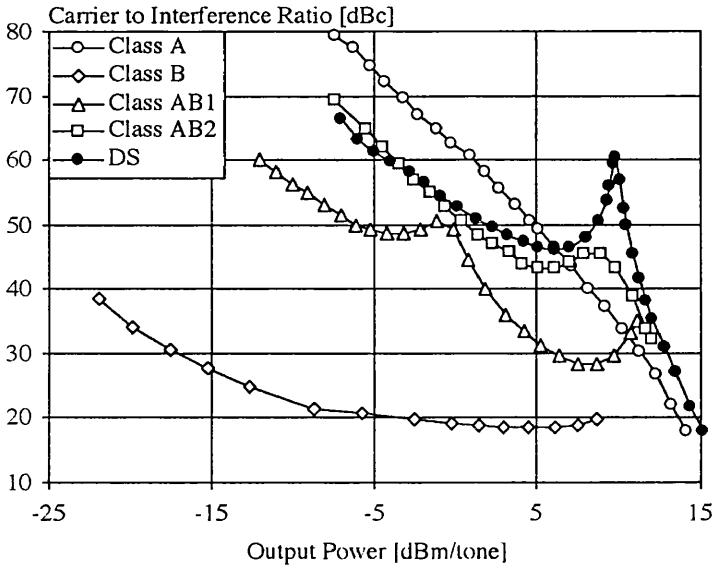


Figure 7.34: Measured c/i of the DS amplifier and various forms of the reference FETs against output power levels. Drain bias is 4.5V and load resistance is 50 Ω. Gate source voltages of the amplifier A, AB2, AB1 and B are -0.75 V, -1.0 V, -1.25 V and -1.55 V, respectively. The V_{GS} of the DS amplifier is -0.75 V and its offset voltage is -0.8 V.

Table 7.3: Circuit designs tested and their output referred 1 dB compression points (P_{1-dB}) and efficiencies at their 1 dB compression points (η); $R_L = 50\Omega$ and V_{DS} = 4.5V. $^{+}$ 0.48 GHz; $^{\$}$ 0.47 GHz and 0.48 GHz.

				1Tone^{+}		2Tone$^{\$}$	
Class	FETs*	V_{GS1}	V_{GS2}	P_{1-dB}	η	P_{1-dB}	η
		[V]	[V]	[dBm]	[%]	[dBm]	[%]
DS	FET1+FET2	-0.75	-1.55	20.19	47.31	15.01	68.14
A	FET1	-0.75	-	18.12	37.53	13.07	43.45
AB2	FET2	-	-1.0	18.0	39.5	11.6	26.62
AB1	FET2	-	-1.25	≈18.5	≈42.0	≈11.0	≈28.04
B	FET2	-	-1.55	≈19.5	≈43.5	≈9.5	≈31.0

wide signal range. From Figure 7.34, we have determined the maximum output power for which the amplifiers of Table 7.3 meet the 45 dBc c/i ratio requirement. For this condition we have tabulated the output power (P_{out}), efficiency, gain and degree of back-off from 1 dB compression point (BO) in Table 7.4.

Table 7.4: Output power (P_{out}), efficiency, gain and degree of back-off from 1 dB compression point (BO) to meet a two tone 45 dBc c/i ratio.

Class	P_{out} [dBm]	Efficiency [%]	Gain [dB]	BO [dB]
DS	11	22.46	4.54	4
A	7	8.01	3.94	6
AB2	9	18.47	2.23	2.6
AB1	0.75	6.80	-1.0	≈10.25
B	-22	0.28	-10.78	≈31.5

It can be seen, that the DS amplifier has the highest output power, highest efficiency and highest gain. The class AB2 amplifier has the lowest back-off and good efficiency but has a significantly lower gain, and in the light of the contour graph of Figure 7.22(a), is more sensitive to gate bias. The class A amplifier has high gain, good output power but poor efficiency. The class AB1 and B amplifiers have output power and efficiency, under the requirement of a 45 dBc c/i ratio,

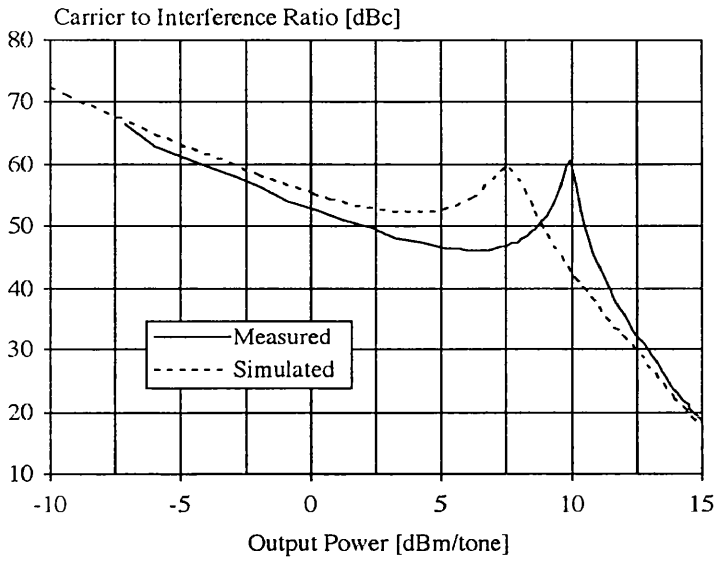


Figure 7.35: Measured and simulated (at 470 MHz and 480 MHz) c/i comparison of the DS amplifier.

which is too low to be directly useful.

7.2.6.9 Measured and Simulated C/I Comparison

In order to examine the robustness of the derivative superposition amplifier with respect to CAD inaccuracies a comparison was carried out between the measured and simulated responses of the amplifier. In Figure 7.35 we compare the measured carrier to interference ratio from Figure 7.29 with the simulated response using a Parker Skellern MESFET model with parameters given in Table 7.1 as a function of output power for the DS power amplifier.

It can be seen from Figure 7.35 that the measured c/i ratio for the DS amplifier occurs at an output power level of 9.9 dBm, whereas in simulation it occurs at an output power level of 7.5 dBm. This difference is due to a combination of process variation and inability of even a good FET model, such as the Parker Skellern, to accurately describe the large signal nonlinear behaviour of a FET circuit. One reason for the discrepancies in Figure 7.35 is large signal frequency dispersion [3], [4], [5]. However, despite this difference it can be concluded that the design of the DS power amplifier using sign reversal is robust enough to allow practical working circuits to be designed.

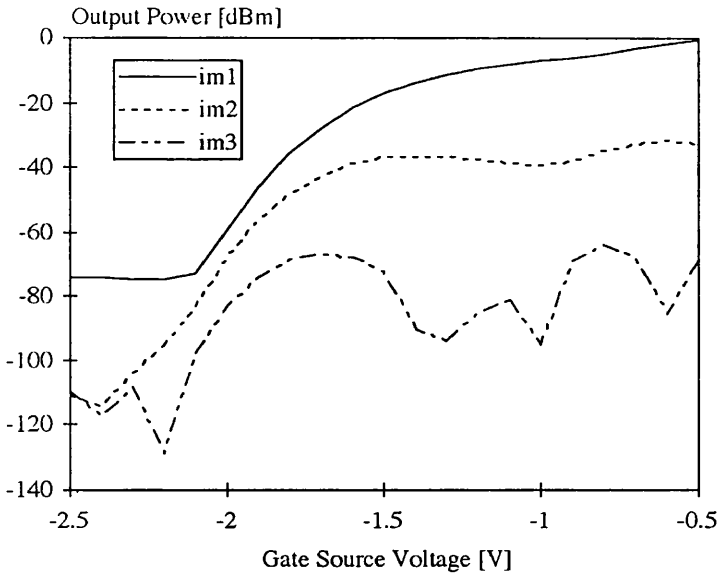


Figure 7.36: Measured (at 20 and 29.3 MHz) small signal intermodulation distortion of the DS amplifier using UoG MONOFAST MESFET process.

7.2.6.10 Alternative Implementation Using UoG MONOFAST MESFET Process

The DS power amplifier was also designed and fabricated using the UoG MONOFAST MESFET process. The circuit diagram is the same as the one given in Figure 7.11. The parameter values for this design are given in Table 7.5.

Table 7.5: Parameter values of the DS amplifier design using the UoG MONOFAST MESFET process.

DS Amplifier Design Parameters Using UoG Process					
V_{GS} [V]	Offset [V]	W_1 [μm]	W_2 [μm]	V_{DS} [V]	R_{Load} [Ω]
-0.7	-0.5	252	504	3	32.2

The measured small signal distortion as a function of gate bias is presented in Figure 7.36.

It can be seen from Figure 7.36 that the design produces the required sign reversal characteristic in the 3rd order intermodulation distortion as expected.

In Figure 7.37 we show contour plot of the magnitude of the 2 tone 3rd order intermodulation distortion (IMD3) measured at 20 MHz and 29.3 MHz as a function of input bias voltage and input signal power for both the single FET reference

and the derivative superposition power amplifier.

The measured 3rd order intermodulation distortion signature of the reference FET and the DS amplifier presented in Figure 7.37 are similar to those obtained for the reference and DS amplifier using MMT F20 MESFET process which were discussed in Section 7.2.6.3.

In Figure 7.38 we show the two tone carrier to interference ratio and gain as a function of output signal power measured at 20 MHz and 29.3 MHz for the reference FET (class A) and the DS amplifier.

It can be seen from Figure 7.38 that the DS amplifier produces a peak in c/i at high output power levels as expected. The 1 dB compression points of the reference FET and the DS amplifier are at 6.8 dBm and 9.6 dBm of output power, respectively. The position of the peak in the c/i curve of the DS amplifier occurs at 6.4 dBm of output power which is a back-off of 3.2 dB from its 1 dB compression point.

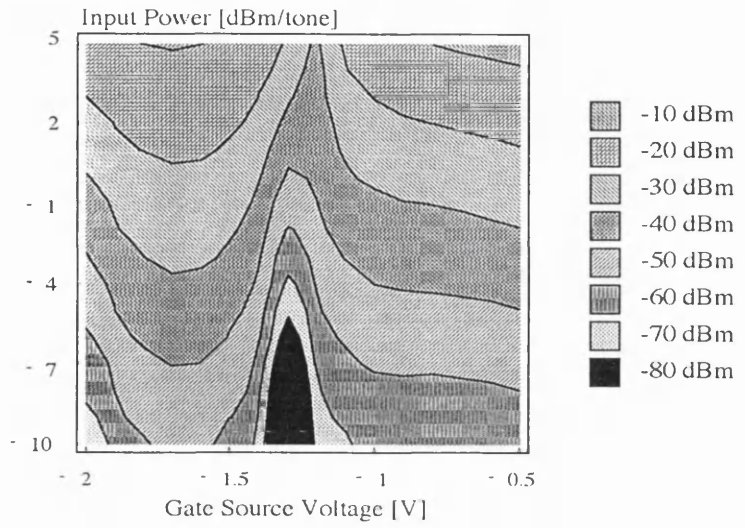
These results are in line with those obtained from the DS amplifier using the MMT F20 FET process. This gives more confidence that the DS power amplifier using the sign reversal technique is robust enough to not only be designed with the existing CAD models but with different processes.

7.2.6.11 Comparison of the Technologies Used

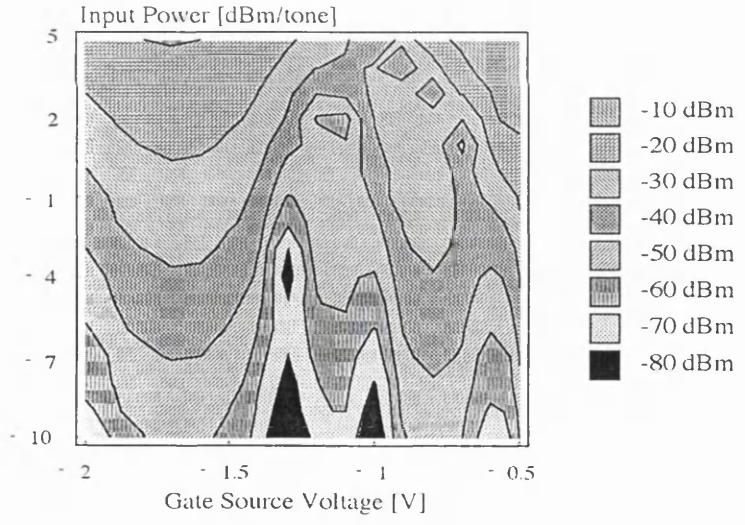
As previously discussed the DS amplifier was designed with two technologies. These were MMT F20 MESFET process and UoG MONOFAST MESFET process. In Table 7.6 we compare some of the characteristics of the two technologies used.

Table 7.6: Comparison of some of the parameter values of the MMT F20 MESFET process and the UoG MONOFAST MESFET process.

Parameters	MMT F20 MESFET	UoG MONOFAST MESFET
Gate Length [μm]	0.5	0.5
Pinch-off Voltage [V]	-1.55	-1.25
Gate-Drain Breakdown [V]	13	5
RF g_m [$\mu S/\mu m$]	123.73	153.30
RF g_{ds} [$\mu S/\mu m$]	12.57	21.00
I_{DSS} [$\mu A/\mu m$]	166.70	61.90
f_T [GHz]	20	40



(a)



(b)

Figure 7.37: Measured (at 20 MHz and 29.3 MHz) contour plot of the 3rd order intermodulation distortion with gate source voltage and input power level; (a) reference FET and (b) DS amplifier using the UoG MONOFAST MESFET process.

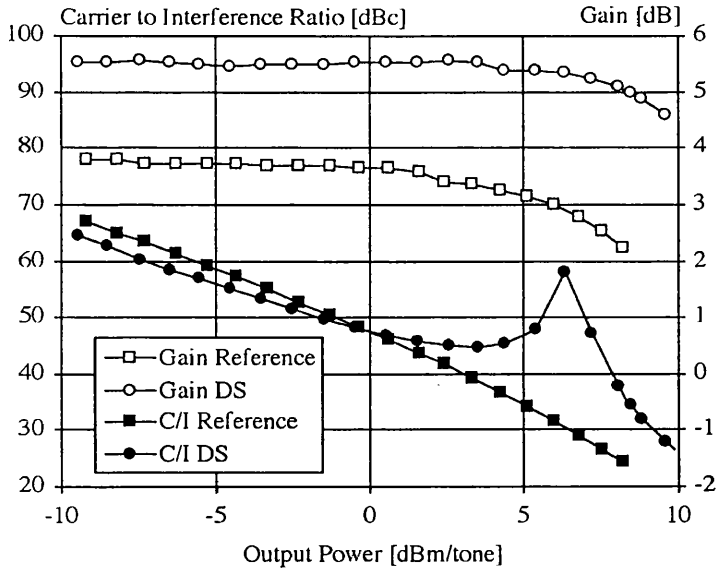


Figure 7.38: Measured two tone c/i and gain (at 20 and 29.3 MHz) as a function of output power for the reference FET and the DS amplifier using UoG MONOFAST MESFET process.

In Figure 7.39 we compare the measured gain and c/i responses of the two DS amplifiers as a function of output power using the two technologies.

It can be seen from Table 7.6 and Figure 7.39 that although the two technologies are quite different from each other the characteristics are similar and behave as expected.

In the next section we explore the possibility of combining the Doherty circuit with that of the DS amplifier in order to obtain improved performance.

7.3 Simulation of the Doherty Amplifier and the Composite Doherty-DS Structure

7.3.1 Design

In Section 3.5.5 the concept of the Doherty amplifier [14], [15], [16] was discussed. Preliminary simulation results which will be presented in the next section suggest that it is possible to bias a Doherty circuit to obtain a null in the 3rd order intermodulation distortion with respect to output signal power. This led to the idea of developing a composite Doherty-DS structure in which the nulls in the 3rd order intermodulation distortions obtained by each of the designs are combined together to produce low distortion over a much wider signal range. The schematic

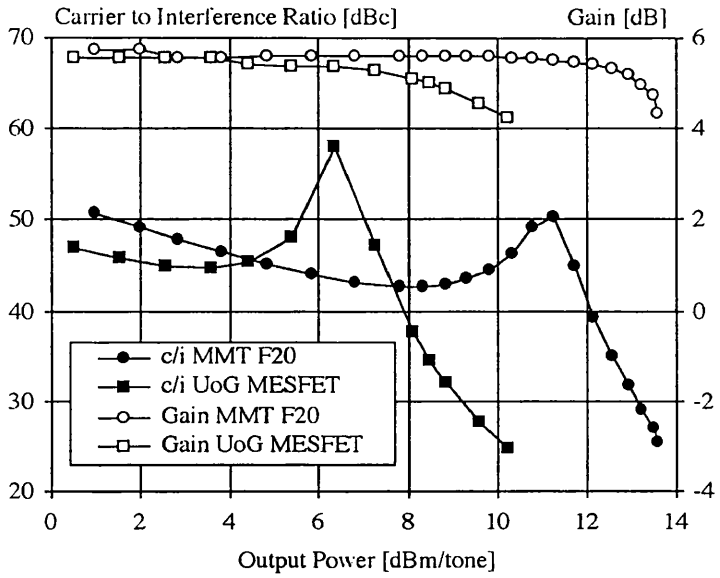


Figure 7.39: Measured (at 20 MHz and 29.3 MHz) gain and c/i responses of the two DS amplifiers using different processing technologies. Load resistance of the DS amplifier using MMT F20 process is 50 Ω and the DS amplifier using UoG MESFET process is 32.2 Ω.

circuit diagram of the structure studied is shown in Figure 7.40. The parameter values of the design are given in Table 7.7. The circuit shown in Figure 7.40 is basically a slight variation of the DS amplifier form discussed in Section 7.2 of this thesis which has two added transmission lines. The transmission line TL_1 is an impedance transformer and the transmission line TL_2 provides a 90° phase shift at the inputs of the two transistors having the same functions as those used in the Doherty amplifier which was discussed in Section 3.5.5 of this thesis. The gate width of the transistor W_2 is chosen to be 2.5 times larger than that of the transistor W_1 in order to produce a sign reversal characteristic similar to the one discussed in Section 7.2 of this thesis.

In the next section the preliminary simulation results are presented.

7.3.2 Simulated Performance

7.3.2.1 Carrier to Interference Ratio Response

In Figure 7.41 we show simulation results of the carrier to interference ratios (c/i) as a function of output power for a reference FET (Class A), the Doherty amplifier, the DS amplifier and the Doherty-DS composite structure (DhDS). The design values are given in the first three columns of Table 7.8.

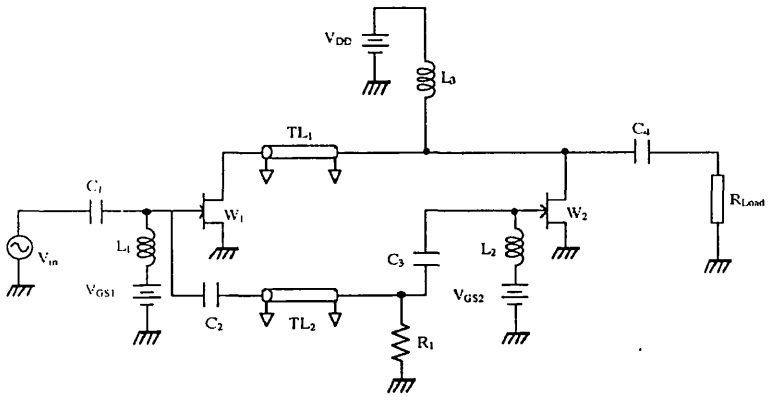


Figure 7.40: Schematic diagram of the Doherty-DS composite structure.

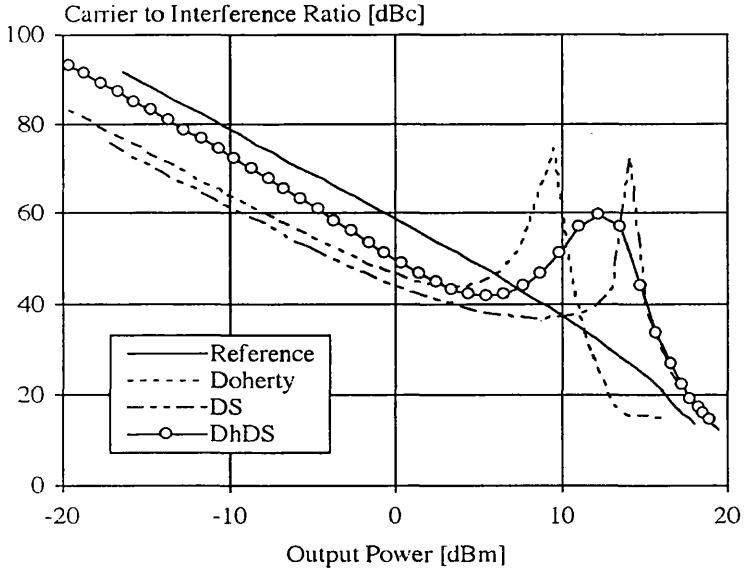


Figure 7.41: Simulated c/i versus output power responses of a reference FET, the Doherty circuit, the DS circuit and the composite Doherty-DS circuit.

Table 7.7: Parameter values of the Doherty-DS composite structure design. Drain bias is 3 V.

Resistors		Inductors		Capacitors	
Par.	Value [Ω]	Par.	Value [μH]	Par.	Value [nF]
R_1	50	L_1	10	C_1	10
R_{Load}	25	L_2	10	C_2	10
		L_3	10	C_3	10
				C_4	10

Transistors		
Parameter	GW [μm]	V_{GS} [V]
W_1	540	-1.28
W_2	1350	-1.70

Transmission Lines			
Par.	Z [Ω]	E [°]	f [MHz]
TL_1	50	90	20
TL_2	50	90	20

It can be seen from Figure 7.41 that the composite Doherty-DS structure offers a much better performance in terms of c/i close to 1 dB compression point in terms of dynamic range over the Doherty and DS amplifiers on their own as a less high but wider peak in the c/i is more useful in practice than a narrower higher peak. It should be noted that the biasing conditions of the Doherty-DS composite structure are different from those of the DS amplifier on its own (see Table 7.8). This is due to the impedance transformer used in the composite structure which changes the currents and voltages in the circuit, and therefore, results in a different quiescent point from that of the DS amplifier on its own.

7.3.2.2 Efficiency

In Figure 7.42 we show simulation results comparing the single tone efficiencies of the reference FET, the Doherty amplifier, the DS amplifier and the Doherty-DS composite structure.

It can be seen from Figure 7.42 that the composite Doherty-DS amplifier offers a reasonable compromise in terms of efficiency compared to those of the Doherty and the DS amplifiers on their own. The performance of the amplifiers are tabulated

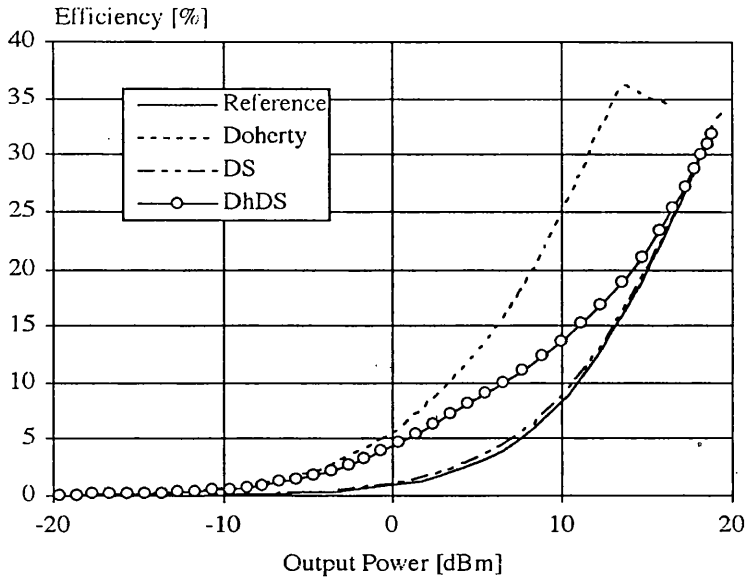


Figure 7.42: Simulated efficiency comparison of the reference FET, Doherty amplifier, DS amplifier and Doherty-DS composite structure.

in Table 7.8.

Table 7.8: Performance comparison of the circuits designed.

Class	V_{GS1} [V]	V_{GS2} [V]	P_{1dB} [dBm]	η_{1dB} [%]	W_1 [μm]	W_2 [μm]
Ref A	-0.75	-	14.5	18.6	675	-
Doherty	-1.34	-3.0	13.0	35.0	675	675
DS	-0.75	-1.65	17.0	27.0	540	1350
Doherty-DS	-1.28	-1.70	18.0	30.0	540	1350

7.4 Summary

In this chapter a 100 mW MMIC DS power amplifier utilising a novel form of DS, which has a region of sign reversal in its g_3 derivative around the quiescent point, has been described. The circuit can be designed with existing CAD models providing they describe soft pinch off behaviour. Good 3rd order intermodulation distortion suppression is achievable with modest back-off at the expense of 5th order intermodulation distortion performance. The MMIC DS power amplifier

achieved a two tone carrier to interference ratio of 45 dBc and an efficiency of 22.5 % when backed off by 4 dB from the 1 dB compression point around 0.5 GHz.

It was found that the DS amplifier achieved a good compromise between carrier to interference ratio, output power, gain, and efficiency. The single FET amplifier classes A, B and AB were unable to achieve the same level of performance in all these parameters simultaneously. The DS amplifier provides this additional flexibility at the cost of a higher chip area than its single FET counterparts.

Although an on chip resistor was used here to match the input of the power amplifier, it is perfectly feasible to use reactive narrow band matching networks, on or off chip, to achieve higher voltage gain. Now that it has been demonstrated that it is possible to design this circuit with the current CAD models it is, therefore, possible to further improve the circuit performance through optimising the device widths and gate bias.

The secondary device is bigger than the reference device which might look disadvantageous at first sight. But on the other hand more power is obtainable and also comparing to other linearisation techniques it occupies less chip area (for example in feedforward the second amplifier makes no contribution to output power and some power from the main device is lost in the couplers). The RF pads occupy quite a lot of chip area (minimum bond pad size 120 μm by 120 μm) compared to a transistor and therefore, the size penalty of the secondary device being larger than the reference device would be tolerable in many cases.

Despite serious modelling difficulties and process variations the design behaved as anticipated which proves it to be a practical robust design.

We then proposed a composite Doherty-DS structure capable of providing a wider dynamic range for better c/i performance close to 1 dB compression point. The composite circuit also offers a good compromise in terms of efficiency compared to those of the Doherty and DS amplifiers on their own. The composite Doherty-DS structure is believed to be a promising avenue for future work. Further development of this circuit is, however, outside the scope of the present thesis due to time restrictions.

In this chapter it was shown that it is possible to use the DS technique in order to design power amplifiers with low distortion near 1 dB compression. In Chapter 8 we will use derivative superposition to design a nonlinear circuit.

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Chapter 8

MMIC Derivative Superposition Frequency Tripler

8.1 MMIC Design, Fabrication and Test

8.1.1 General

The frequency multiplier is a special class of circuit which is used in communication and instrumentation systems. Frequency doublers and triplers are employed in signal processing applications, for modulation or frequency synthesis and have the advantage of providing an extended frequency range. RF frequency doublers are much easier to design than frequency triplers as the fundamental breakthrough can be suppressed by use of balanced structures, but filtering is needed to reduce even harmonic content. Broadband frequency doublers can be readily implemented with balanced techniques [1], [2]. High Q filtering of the output of a nonlinear device has also been used for fixed frequency multiplication. A frequency tripler using feedback to eliminate the need for filtering out the fundamental of the output signal has been described in [3]. Broadband frequency doubling and square root circuits have been designed using square law FET models [4], [5]. Fattaruso [6] proposed a MOSFET version of the multi-tanh approximation for triangle wave to sine wave conversion. Gilbert [7] has successfully demonstrated the use of the BJT multi-tanh approach to implement high performance mixers. Seevinck [8] has shown the possibility of extending Gilbert's translinear loop principle to MOSFETs to realise various algebraic functions.

At microwave frequencies, the common source amplifier is perhaps the most used FET configuration. The derivative superposition (DS) technique [5], [9] can be used to control the nonlinear behaviour of the common source amplifier at the

circuit level in order to produce nonlinear functions such as frequency multipliers.

In Section 3.6.5 a frequency tripler using derivative superposition was reviewed [5]. In this section we present a complete derivative superposition frequency tripler that has been implemented in MMIC technology on a single chip. We begin by discussing the design approach, and then present simulation results. The MMIC layout and comments on the measured results of this circuit will be given at the end of this section.

8.1.2 Design Strategy

A MMIC derivative superposition frequency tripler is to be designed for operation over the frequencies ranging from 100 MHz to 1 GHz. In the following we will present the steps taken in order to design this circuit.

8.1.2.1 Derivative Superposition Solution

The frequency tripler is a nonlinear circuit designed to realise a specified transfer characteristic. In order to obtain the 3rd harmonic (i.e. frequency tripling) we need a cubic function. The expansion of a cubic function contains a fundamental term as well as a tripled term. In order to cancel the fundamental term and hence, obtain an ideal transfer characteristic for a transconducting frequency tripler we need to subtract the same amount of the fundamental. Therefore, we obtain the following expression for an ideal frequency tripler.

$$i_{out} = k\left(a^3 v_{in}^3 - \frac{3}{4} a v_{in}\right) \tag{8.1}$$

where v_{in} is the input voltage and i_{out} is the output current. The constants a and k are input and output scaling factors, respectively.

In order to obtain such a transfer characteristic a minimum of 3 transistors are needed. The schematic arrangement is shown in Figure 8.1. The first transistor (J_{A1}) is to provide finite transconductance. The second transistor (J_{A2}) performs a subtraction and hence, reduces the transconductance. The drain of the third transistor (J_{A3}) is joined with the drain of the first transistor (J_{A1}) and hence, results in the increase of the transconductance. By correct choice of gate widths and biasing points of the transistors a transfer characteristic of the form presented in Eq. 8.1 is achieved. In order to get an approximate idea for the gate widths and biasing points of the transistors in the derivative superposition structure the intrinsic RF derivatives were calculated in a numerical package called FET FIT [10]. The model used was a Parker Skellern MESFET model of the MMT F20

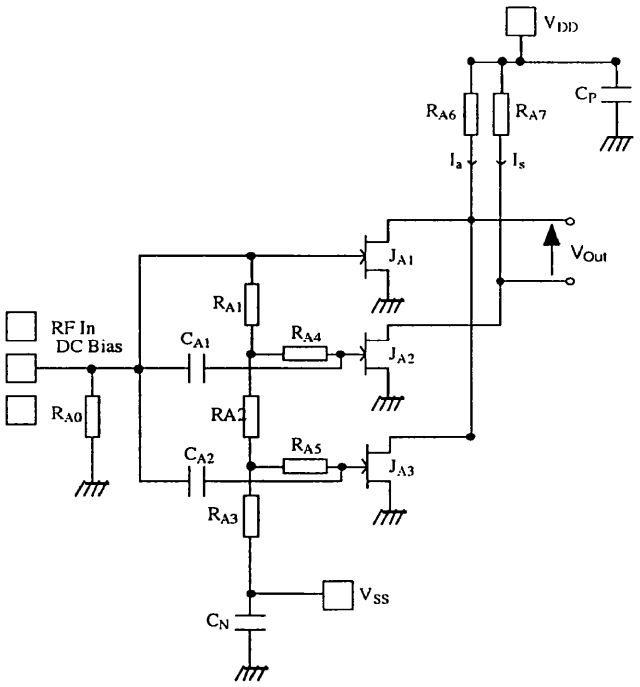
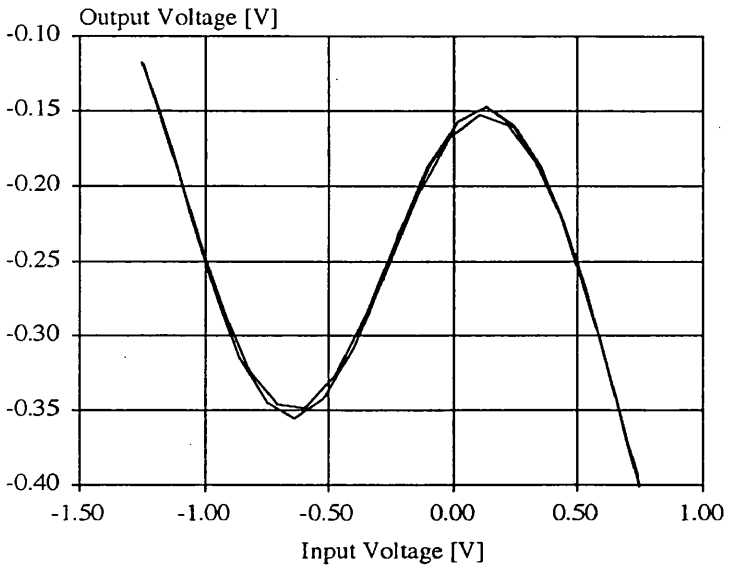


Figure 8.1: The schematic diagram of the derivative superposition structure for implementing a frequency tripler.

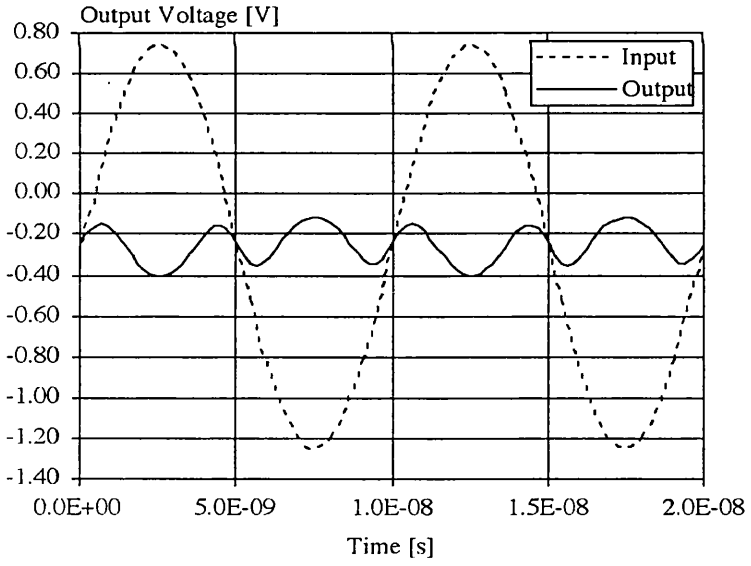
MESFET. The model parameters of this device are the same as those presented in Table 7.1 of Chapter 7 of this thesis. The model was extracted for a 0.5 μm gate length MESFET with the DC drain biased at $V_{DS} = 3V$, with the DC gate bias swept from $V_{GS} = -2V$ to $V_{GS} = +0.5V$ in 20 mV steps. The intrinsic derivatives were converted to their extrinsic derivatives using a mathematical transformation. The extrinsic derivatives were then imported into a spread sheet. These derivatives were used in a look up table by means of index addressing, and formulas were used to scale and offset the derivatives to carry out the design. These preliminary results were then used in SPICE to get a more realistic circuit function.

The SPICE simulation of the dynamic transfer characteristic and the input and output signals of the derivative superposition tripler are shown in Figure 8.2(a) and (b), respectively. Figure 8.2(a) has the required transfer characteristic of Eq. 8.1 for implementing a frequency tripler. Figure 8.2(b) shows the tripled output voltage of the DS section. In simulations it was noted that the transfer characteristic was degraded if the load resistance was too high ($> 20\ \Omega$ approximately). The passive and active component values are given in Table 8.1 and Table 8.2, respectively.

In a DS circuit it is important that the phase errors of the signals on the gates of the transistors are minimal. This was investigated using SPICE and the result is



(a)



(b)

Figure 8.2: Simulated response of the DS section. (a) The dynamic transfer characteristic and (b) time domain response.

Table 8.1: Passive parameter values of the DS MMIC frequency tripler. $R_{A0} = 50\Omega$, $R_{Load} = 50\Omega$ and de-coupling capacitors are 10 pF each.

Resistors [Ω]					
DS Section		Diff Pair Section		Driver Amp. Section	
Parameter	Value	Parameter	Value	Parameter	Value
R_{A1}	12.4k	R_{B1}	6k	R_{C1}	150
R_{A2}	14.8k	R_{B2}	5k	R_{C2}	5k
R_{A3}	37.6k	R_{B3}	6k	R_{C3}	5k
R_{A4}	10k	R_{B4}	5k	R_{C4}	250
R_{A5}	10k	R_{B5}	150	R_{C5}	2.5k
R_{A6}	20	R_{B6}	150		
R_{A7}	20	R_{B7}	12k		
		R_{B8}	75		
		R_{B9}	2k		
Capacitors [pF]					
DS Section		Diff Pair Section		Driver Amp. Section	
Parameter	Value	Parameter	Value	Parameter	Value
C_{A1}	20	C_{B1}	10	C_{C1}	10
C_{A2}	20	C_{B2}	10	C_{C2}	10
		C_{B3}	10		

shown in Figure 8.3. It can be seen from Figure 8.3 that the phase shifts between the signals are very small and decrease as the frequency increases.

Having described the derivative superposition design of the tripler, in the next section we will present a differential pair which is used to carry out the current subtraction required in the DS structure.

8.1.2.2 Differential Pair Section

In order to perform the subtraction of the output currents in the DS section, a differential pair was employed. In Figure 8.4 we show the schematic diagram of the complete derivative superposition frequency tripler design. It can be seen form Figure 8.4 that the entire design consists of 3 cascaded sections. The first stage is the derivative superposition block which was discussed in the previous section. The second stage is a differential pair section which is used to carry out

Table 8.2: Active parameter values of the DS MMIC tripler. Drain bias is 3 V.

Transistors								
DS Section			Diff Pair Section			Driver Amp. Section		
Par.	GW[μm]	V_{GS}[V]	Par.	GW[μm]	V_{GS}[V]	Par.	GW[μm]	V_{GS}[V]
J_{A1}	200	-0.34	J_{B1}	200	-0.91	J_{C1}	200	-0.12
J_{A2}	468	-0.89	J_{B2}	200	-0.91	J_{C2}	600	-0.40
J_{A3}	595	-1.60	J_{B3}	400	-0.93			
			J_{B4}	400	-0.85			

the required subtraction of the outputs of the derivative superposition section. The final section is a two stage amplifier in order to increase the amplitude of the output signal to an acceptable level which will be discussed in the next section.

An important issue in the design of the differential pair is the common mode rejection ratio (CMRR) [11]. The simulated CMRR of the differential pair section of the design in Figure 8.4 is shown in Figure 8.5. The passive and active component values are given in Table 8.1 and Table 8.2, respectively. It can be seen from Figure 8.5 that the CMRR is at an acceptable level (below -30 dB) for frequencies of operation up to 1 GHz. In order to achieve this kind of response for the CMRR we had to compromise on the gain of the differential pair section which resulted in loss of gain. This is not problematic since the final stage of the circuit will provide the required gain for the circuit. This will be discussed in the next section.

8.1.2.3 Amplifier Section

A single stage amplifier provides a gain of about 10 dB which was not satisfactory considering the small gain available from the DS section and the loss of the differential pair section. Therefore, a two stage amplifier was employed. The frequency response of the gain of the composite amplifier is shown in Figure 8.6. The passive and active component values are given in Table 8.1 and Table 8.2, respectively. It can be seen from Figure 8.6 that a gain of about 16-18 dB is achievable over the intended range of operation of the frequency tripler.

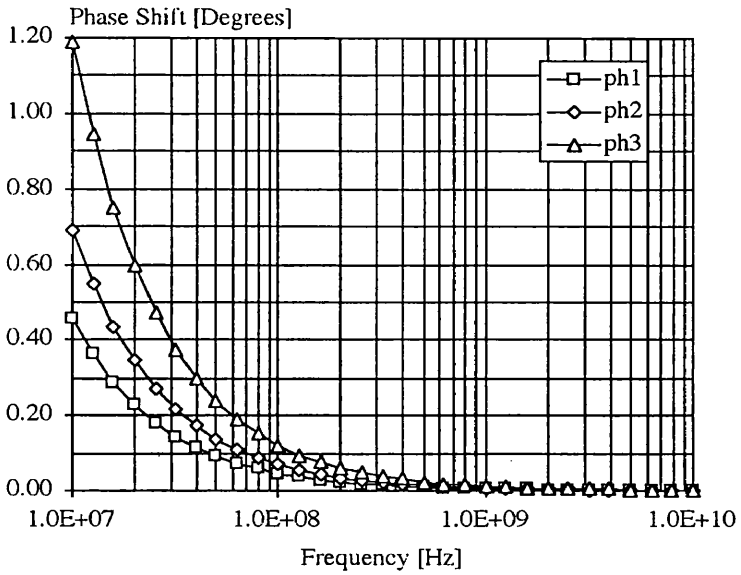


Figure 8.3: The phase shifts between the gates of the transistors of the DS section. ph_1, ph_2 and ph_3 represents the phase shifts on the gates of the transistors J_{A1}, J_{A2} and J_{A3} of Figure 8.1, respectively.

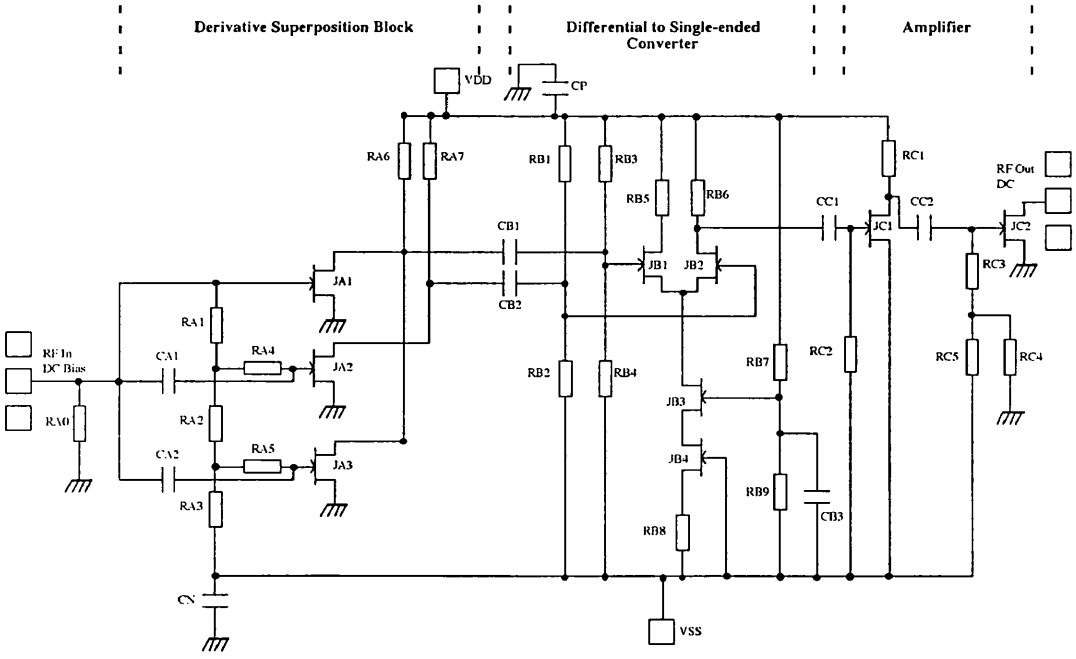


Figure 8.4: The schematic diagram of the entire DS frequency tripler circuit.

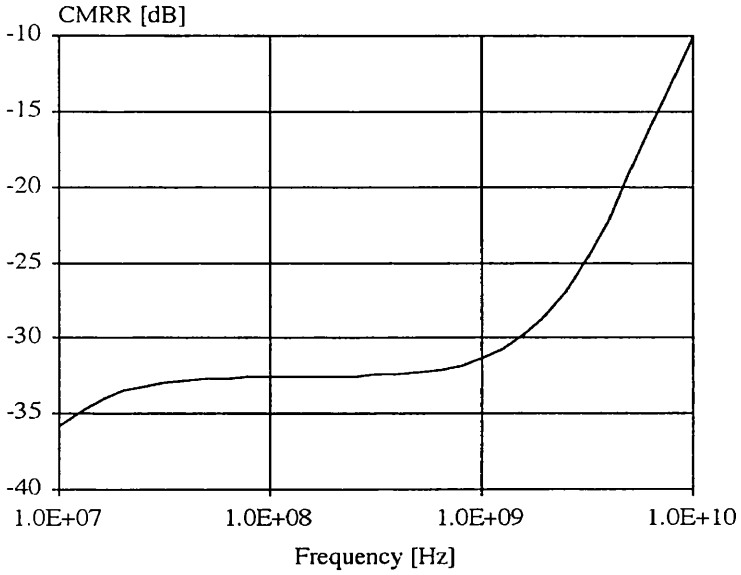


Figure 8.5: The CMRR of the differential pair section.

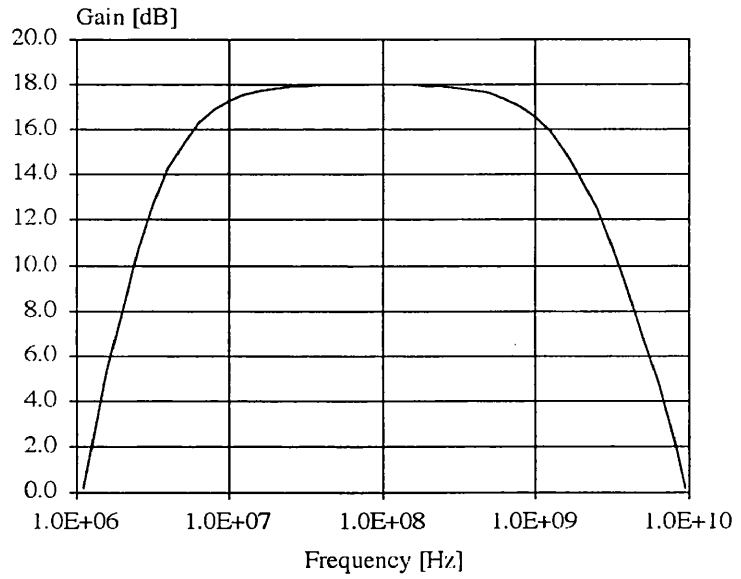


Figure 8.6: The gain response of the two stage driver amplifier.

8.1.3 Simulated Performance of the Entire Design

In this section we present the simulation results of the entire DS frequency tripler design.

8.1.3.1 Time Domain Response

In Figure 8.7(a) and (b) we show the time domain SPICE simulation of the input and output voltages for the complete design at 100 MHz and 1 GHz, respectively. It can be seen from Figure 8.7(a) and (b) that the required frequency tripling occurs in both cases. However, the tripling function in the 1 GHz case has deteriorated due to the finite bandwidth of the differential pair stage.

8.1.3.2 Harmonic Distortion Variation with Input Signal

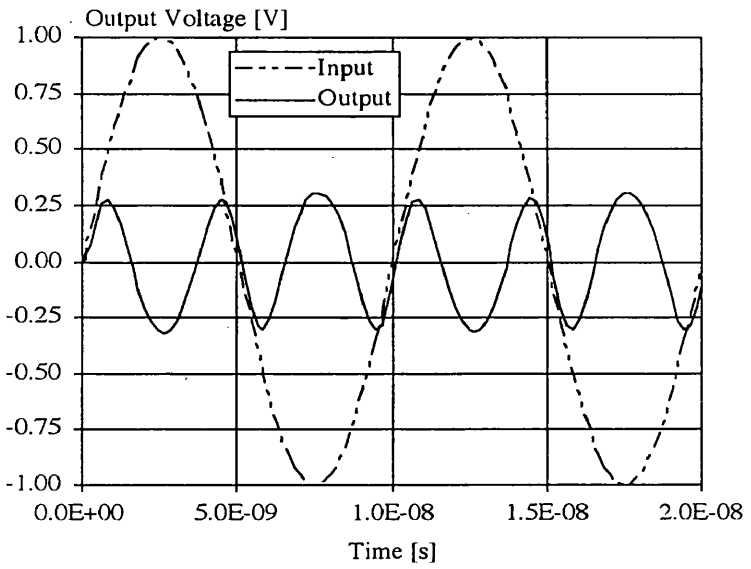
In Figure 8.8(a) and (b) we show SPICE simulations of the harmonic distortion as functions of input signal amplitude for the compete design at 100 MHz and 1 GHz, respectively. It can be seen from Figure 8.8(a) that the unwanted signals are suppressed by about 15 dB at -0.5 dBV_{pk} input signal level for the 100 MHz case. It can be seen from Figure 8.8(b) that the unwanted signals are suppressed by about 7 dB at -0.5 dBV_{pk} input signal level for the 1 GHz case.

Additional suppression of unwanted harmonics can be achieved using filtering and balancing techniques.

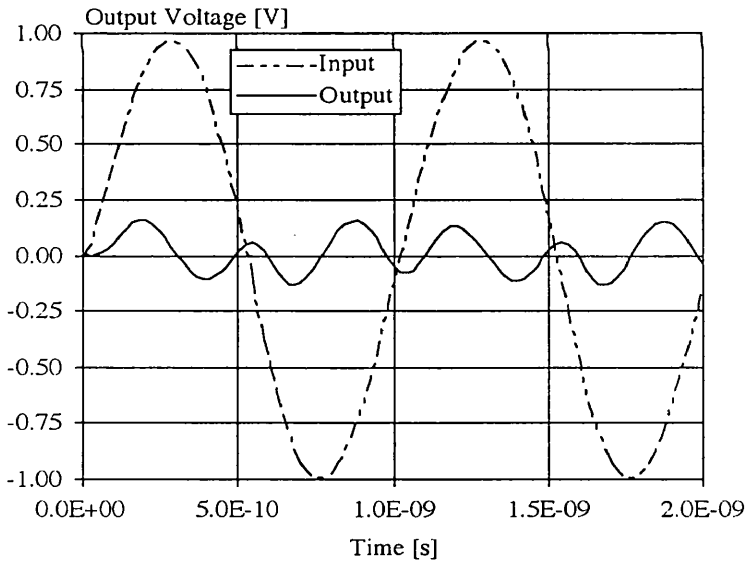
8.1.4 MMIC Layout

The circuit has been fabricated by MMT using the F20 GaAs MESFET process. A photograph of the MMIC frequency tripler is shown in Figure 8.9.

The RF input is applied to the gates of the FETs from the left hand side. The bias voltages required for the FETs are provided by a resistor chain. The drains of the top and bottom FETs of the DS section are joined to provide current summation and are fed to one side of the differential pair; the drain of the middle FET of the DS section is fed to the other side of the differential pair. This is done in order to achieve current subtraction. The output taken from the differential pair is fed to a two stage amplifier. The RF output pad is on the right hand side of the layout. The top and bottom DC pads are used for biasing. The total design has a chip area of 1915.5 μm x 1433.5 μm.

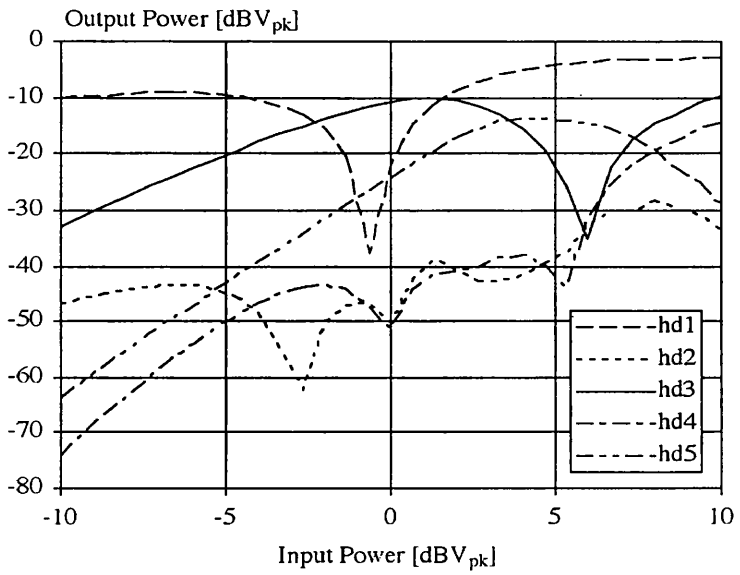


(a)

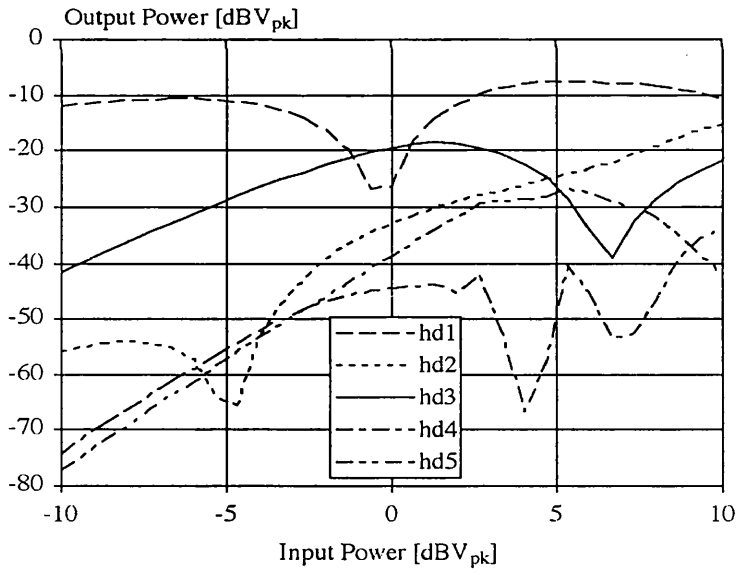


(b)

Figure 8.7: Simulated time domain responses of the entire circuit; (a) at 100 MHz input and (b) at 1 GHz input.



(a)



(b)

Figure 8.8: Simulated harmonic distortion (hd) versus input signal amplitude for the entire circuit; (a) at 100 MHz input and (b) at 1 GHz input.

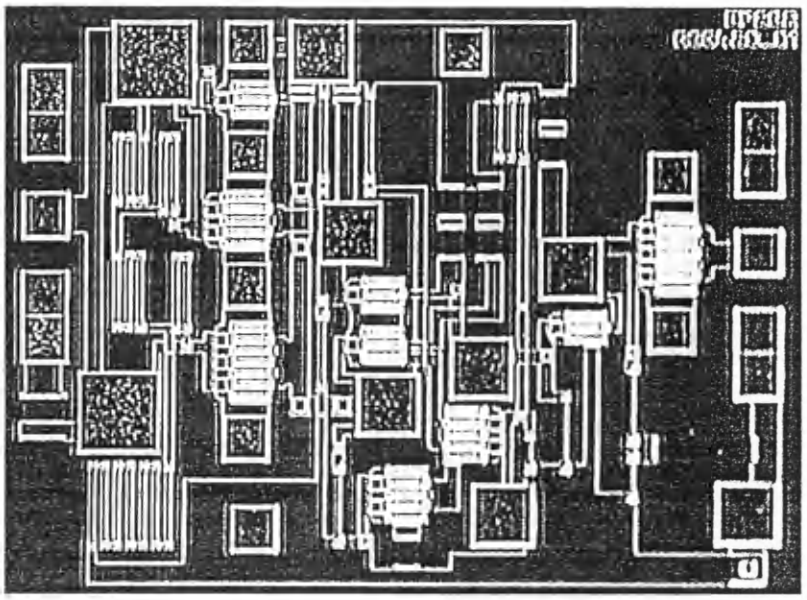


Figure 8.9: Photograph of the MMIC DS frequency tripler.

8.1.5 Measured Performance

Measurements were initially made at 100 MHz upon the MMIC DS frequency tripler in order to investigate the level of 3rd harmonic distortion product compared to the levels of other distortion products. The level of the measured 3rd harmonic distortion was found to be much lower than the fundamental and 2nd order distortion products. The nominal voltages of the circuit were tuned but this did not improve the level of the 3rd harmonic distortion significantly. At this point it was decided to examine the circuit in more detail. The following tests were carried out.

V_{SS} and V_{DD} of the circuit shown in Figure 8.4 were set to -3.5 V and 3 V, respectively. The 50 Ω input of the 4195A network/spectrum analyser was used as a load for the circuit. A drain bias of 3 V was applied to the transistor J_{C2} of the driver stage of the circuit shown in Figure 8.4. The network/spectrum analyser was set to network analyser mode. The signal power of the network analyser was set to be -20 dBm in order to make sure that the nonlinearity of the analyser does not interfere with the nonlinearity of the circuit. The frequency of operation was chosen to be 20 MHz. The small signal gain of the circuit was then measured. A comparison of the measured and simulated gain of the circuit as a function of input DC voltage is shown in Figure 8.10.

The explanation of the expected small signal behaviour of the circuit is as follows. When the input voltage (V_{IN}) is below pinch-off ($V_{IN} - V_{SS} = 0V$), all

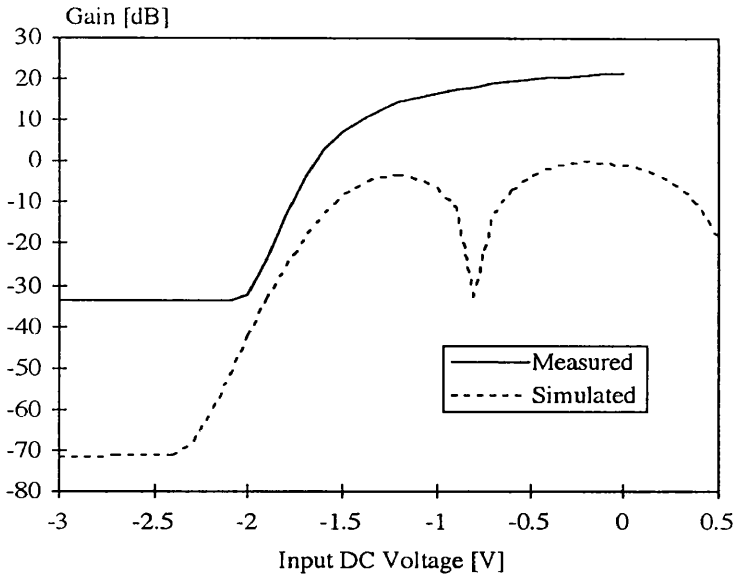


Figure 8.10: Measured and simulated comparison of the small signal gain of the MMIC frequency tripler.

three DS FETs of Figure 8.4 should be pinched off, i.e. there is no gain. When the input voltage is somewhat above pinch-off, only the 200 μm FET (J_{A1}) of the DS section of Figure 8.4 should turn on giving us gain with a phase shift of 180 degrees (3 inverting amplifier stages). As we increase the input voltage, at some point the 468 μm FET (J_{A2}) of the DS section of Figure 8.4 should also turn on. This will cause the gain to fall to zero, swap sign (i.e. phase shift is zero) and then it should increase again. As we increase the input voltage still further the 595 μm FET (J_{A3}) of the DS section of Figure 8.4 should also turn on, this should cause the gain to fall to zero and to swap sign (i.e. the phase shift is returned to 180 degrees). The overall effect is to give us a gain as a function of input DC voltage that is parabolic on a signed linear scale of the form $y = x^2$. The quiescent point of the circuit was designed to be at the minimum of this parabola. It can be seen from Figure 8.10 that the simulated gain of the circuit behaves as expected whereas the measured gain does not show any change of sign. This profile of the measured performance was observed in several chips which were tested.

The MMIC was then visually checked using a scanning electron microscope but no visible defect was detected.

It can be seen from Figure 8.10 that the gain of the measured circuit is much higher than the gain of the simulated circuit. Therefore, more simulations were performed in SPICE in order to investigate the reason for the significant discrepancy between the measured and simulated gain. It was found that if the capacitor

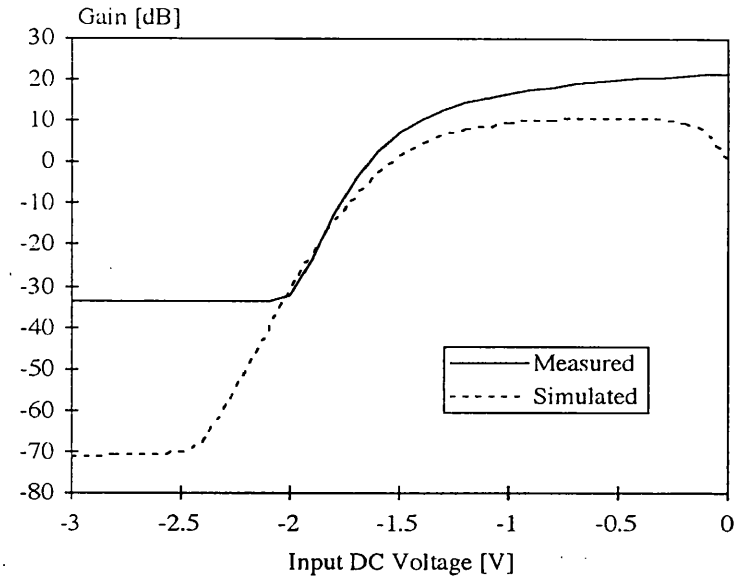


Figure 8.11: Measured and simulated comparison of the small signal gain of the MMIC frequency tripler. Note that in the simulation the capacitor C_{A2} of Figure 8.4 is short circuited.

(C_{A2}) connected to the gate of the 595 μm transistor (J_{A3}) of the DS section in Figure 8.4 is short circuited this will cause the 200 μm (J_{A1}) and 595 μm (J_{A3}) transistors of the DS section of Figure 8.4 to turn on at the same time resulting in high gain. Small signal simulation of the gain of the circuit was performed using SPICE with the capacitor C_{A2} of Figure 8.4 shorted. This simulated result is compared with measured data in Figure 8.11.

It can be seen from Figure 8.11 that the simulated result is now reasonably close to the measured curve. This shows, in principle, that the profile of the measured curve can be explained by component malfunction, however, since visual inspection using a scanning electron microscope did not show any errors, therefore, we can not be specific about the nature of the error.

In the next section we will present the design of a MIC frequency tripler for incorporation for microwave frequency operation.

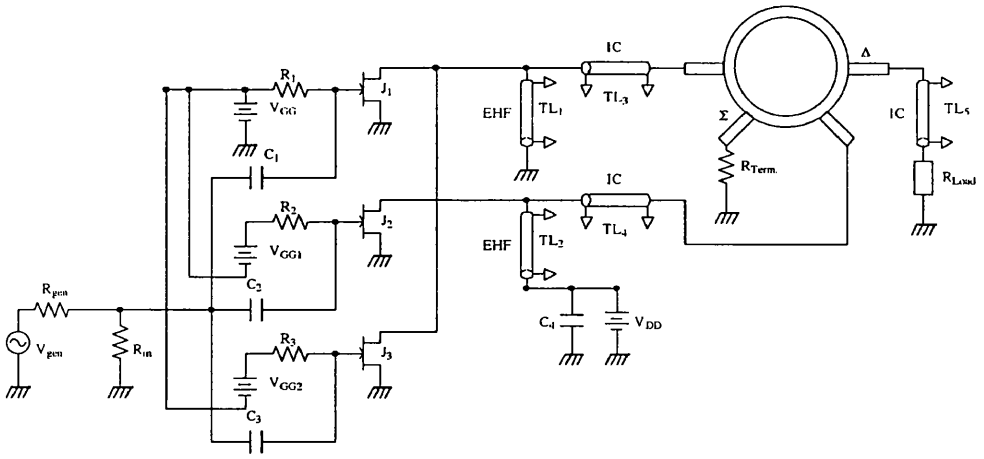


Figure 8.12: Schematic circuit diagram of the DS frequency tripler for microwave frequencies operation. EHF and IC transmission lines represent Even Harmonic Filters and Impedance Transformers, respectively.

8.2 Incorporation of MMIC on a MIC for Microwave Frequency Operation

8.2.1 General

In order to design a frequency tripler operating well into the microwave frequency range it is important to eliminate the differential pair section of the DS frequency tripler discussed in the previous section due to its finite bandwidth. Instead a rat race coupler can be employed.

In the next section we described the design of a MMIC DS frequency tripler suitable for incorporation on a MIC for microwave frequency operation which employs a rat race coupler in order to facilitate the required current subtraction.

8.2.2 Design

The schematic circuit diagram of the DS frequency tripler is shown in Figure 8.12. It can be seen from Figure 8.12 that the circuit consists of a DS section and a rat race coupler to perform the required subtraction. The design of the DS section was the same as for the one described in Section 8.1. Short circuited stubs were used to suppress the 2nd harmonic at the input of the rat race. The parameter values are given in Table 8.3.

Table 8.3: Parameter values of the DS MMIC tripler suitable for incorporation on a MIC for $V_{DD} = 4$.

Trans Lines				Resistors		Capacitors	
Par.	Z[Ω]	E[°]	f[MHz]	Par.	Value[Ω]	Par.	Value[pF]
TL_1	25	90	30	R_{in}	50	C_1	10
TL_2	25	90	30	R_1	1k	C_2	10
TL_3	100	90	30	R_2	1k	C_3	10
TL_4	100	90	30	R_3	1k	C_4	10
TL_5	100	90	30	$R_{Term.}$	25		
				R_{Load}	400		
				R_{gen}	50		

Transistors		
Parameter	GW[μm]	V_{GS}[V]
J_1	400	-0.50
J_2	700	-0.85
J_3	840	-1.61

8.2.3 Simulated Performance

In this section we present the preliminary simulation results of the design.

8.2.3.1 Time Domain Response

In Figure 8.13 we show time domain simulation using MDS for the complete design at 1 GHz. It can be seen from Figure 8.13 that the required frequency tripling action is obtained. It can also be seen that the signal swing of this circuit simulated at 1 GHz has a considerable improvement over that of the circuit using a differential pair which was discussed in the previous section.

8.2.3.2 Harmonic Distortion Variation with Input Signal

In Figure 8.14(a) and (b) we show the results of a harmonic distortion simulation using MDS for the design as a function of the input signal amplitude at 100 MHz and 1 GHz, respectively. It can be seen from Figure 8.14(a) that the unwanted signals are suppressed by about 40 dB at 9 dBm input signal level for the 100 MHz case. It can be seen from Figure 8.14(b) that the unwanted signals are suppressed

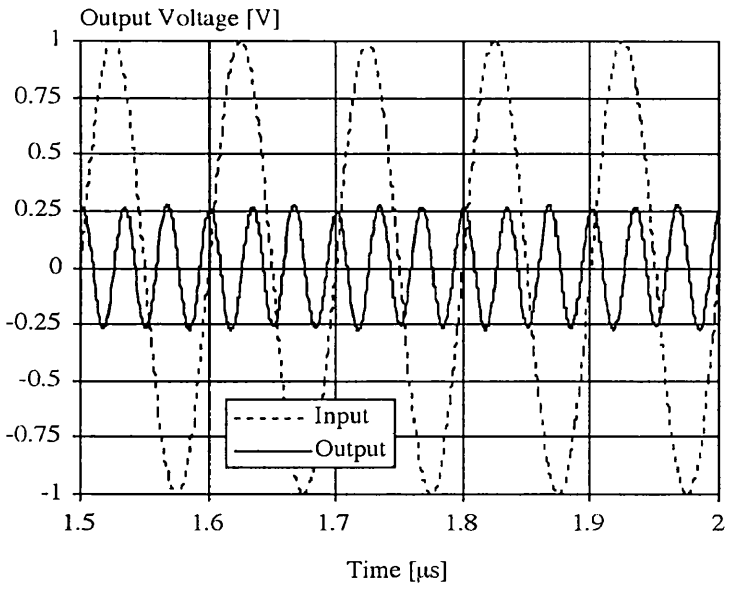


Figure 8.13: Simulated time domain response of the DS tripler at 1 GHz input.

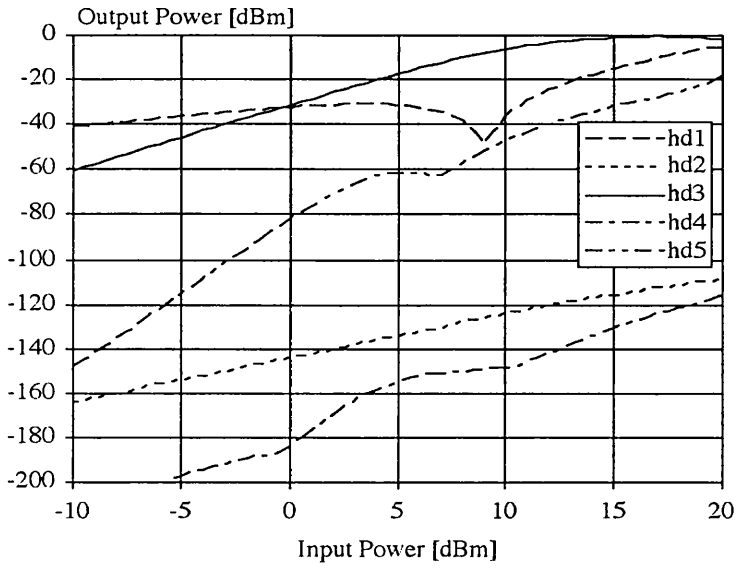
by about 18 dB at 9 dBm input signal level for the 1 GHz case.

8.2.4 MMIC Layout Suitable for MIC Incorporation

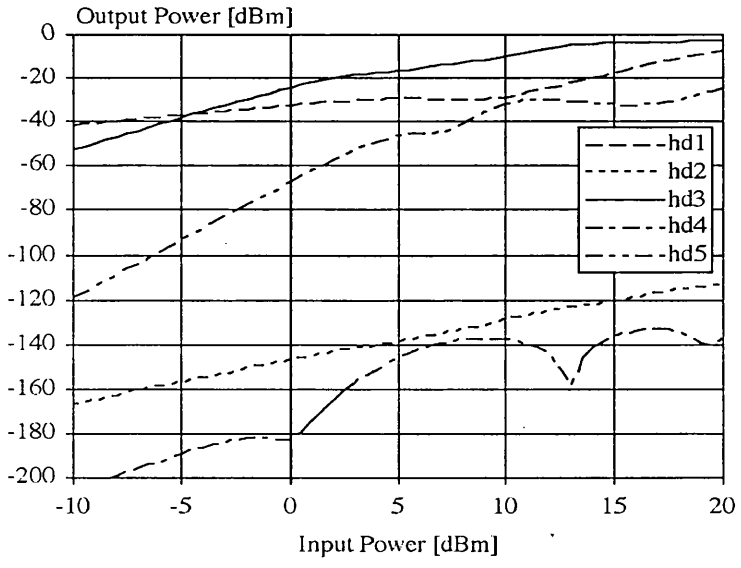
A possible MMIC layout plot of the DS frequency tripler suitable for incorporation on a MIC is shown in Figure 8.15. The RF input is applied to the gates of the FETs from the middle pad. This also provides the gate bias for the 400 μm transistor (J_1) of Figure 8.12. The DC pads on either side of the RF input provide the gate bias voltages for the 700 μm (J_2) and 840 μm (J_3) transistors of Figure 8.12. The drains of the transistors J_1 and J_3 of Figure 8.12 are connected to provide current summation. This is the pad on the top right hand side of Figure 8.15. The drain of transistor J_2 of Figure 8.12 is connected to the pad on the top left hand side of Figure 8.15. Due to the time restriction, the fabrication and testing of this circuit fell outside the scope of the present thesis.

8.3 Summary

We have demonstrated the possibility of designing frequency triplers with the derivative superposition method both at 100 MHz and at microwave frequencies. The circuit for the lower frequency of operation uses a differential pair for the required subtraction whereas, the design for the microwave frequency operation employs a rat race. The design procedure and the simulated performance of the



(a)



(b)

Figure 8.14: Simulated harmonic distortion (hd) versus input signal amplitude of the DS tripler; (a) at 100 MHz input and (b) at 1 GHz input.

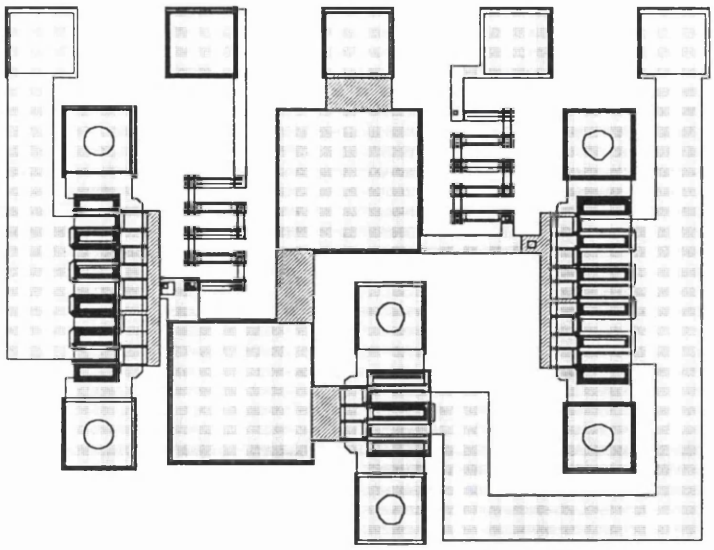


Figure 8.15: A possible MMIC layout plot of the DS tripler suitable for incorporation on a MIC.

MMIC DS frequency tripler together with comments on its measured performance for lower frequency operation have been presented. Although the simulated performance of the circuit was shown to be promising the measured results were not as expected. The specific reason for the nature of this error is not clear.

The possibility of implementing a MMIC derivative superposition frequency tripler suitable for incorporation on a MIC for microwave frequency operation has been discussed. The design uses a rat race coupler for the required subtraction. The simulation results appear to be promising.

In this chapter it was shown that it is possible to employ derivative superposition to design frequency triplers. In Chapter 9 we draw general conclusions of the work presented in this thesis and outline some possible future work.

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Chapter 9

Conclusions and Further Work

9.1 Conclusions

In this work progress has been made on improving and extending the scope of derivative superposition circuits.

Several linear and nonlinear circuits using derivative superposition have been designed. These include a MMIC DS power amplifier using the sign reversal technique for achieving low 3rd order intermodulation distortion near 1 dB compression; DS frequency triplers capable of working well into microwave frequency region and a specific nonlinear function circuit for a quasi-optical tracking system.

The potentiality of designing a new simple form of derivative superposition power amplifier using sign reversal of the 3rd derivative of drain current with respect to gate source voltage of 2 FETs was investigated. The design has been fabricated in MMIC using the MMT F20 process. Good 3rd order intermodulation distortion suppression is achievable with modest back-off at the expense of 5th order intermodulation distortion performance. The MMIC power amplifier achieved a two tone carrier to interference ratio of 45 dBc and an efficiency of 22.5 % when backed off by 4 dB from the 1 dB compression point around 0.5 GHz.

A novel composite Doherty-DS structure was shown to be capable of providing a wider dynamic range for better c/i performance close to 1 dB compression point and a good compromise in terms of efficiency compared to those of the Doherty and the DS amplifiers on their own. The preliminary c/i and efficiency simulations carried out on this structure have been shown to be promising.

The possibility of designing a frequency tripler with the derivative superposition method for 100 MHz operation was investigated. The circuit uses a differential pair for the required subtraction. The design procedure and the simulated performance of the MMIC DS frequency tripler together with comments on its measured

performance for lower frequency operation have been presented. Although the simulated performance of the circuit was shown to be promising the measured results were not as expected. The specific reason for the nature of this error is not clear.

The prospect of implementing a MMIC derivative superposition frequency tripler suitable for incorporation on a MIC for microwave frequency operation has been explored. The design uses a rat race coupler for the required subtraction. The simulation results appear to be promising. However, due to time limitations, the fabrication and testing of this circuit fell outside the scope of the present thesis.

The possibility of implementing a nonlinear function circuit for a quasi-optical tracking system preliminary working at 100 MHz using the derivative superposition approach was also explored. SPICE simulation results were shown to be promising. The circuit has been designed for implementation using the University of Glasgow MONOFAST MESFET MMIC process as a single chip.

As part of the more general aspect of this work, various FETs have been compared in order to investigate the common factors that influence their small signal intermodulation distortion performance. It was found that soft pinch-off produces a characteristic distortion signature that occurs in a wide range of FETs including Si-JFETs, MOSFETs, MESFETs and HEMTs. Also, the intermodulation distortion of a HEMT is considerably less sensitive to voltage gain than for a MESFET. Increasing drain bias can reduce 3rd order intermodulation distortion in a MESFET by more than 10 dB for a limited range of load resistance values. The repeatability of the pinch-off voltage and soft pinch-off behaviour of a process directly affects repeatability of a low distortion design. By using a contour mapping technique to describe the nonlinear behaviour of a FET, it has been possible to identify low distortion regions of operation whilst still giving small signal matching.

9.2 Future Work

The work presented is encouraging for further work along the lines presented and several tasks which can be envisaged are as follows:

Detailed spectral regrowth measurements should be carried out on the MMIC DS power amplifier presented in Section 7.2 of this thesis. A preliminary off chip matching network was designed in Section 7.2.5.4. This should be developed further and fabricated in a MIC form suitable for incorporation with the MMIC DS power amplifier. Therefore, further measurements should be carried out upon the DS amplifier at microwave frequencies.

The simulations carried out on the Doherty-DS composite structure proposed in Section 7.3 are promising. A MMIC form of this structure should be fabricated and tested.

A MMIC version of the DS frequency tripler suitable for incorporation on an MIC which was described in Section 8.2 of this thesis should be fabricated and tested.

A MMIC low noise HEMT amplifier using derivative superposition method should be designed using a number of FETs in parallel with each other in order to minimise the 3rd order derivative with respect to drain current leading to low 3rd order intermodulation distortion over a wide input power levels.