Novel transceiver architectures for automatic target recognition in UAV-based SAR systems

Alan Bannon, Michael Woollard, Prof. Hugh Griffiths, Dr Matthew Ritchie
Department of Electronic and Electrical Engineering

Context

This project involved SAR simulation, FMCW radar construction, ASIC design and radar signal processing. The focus of the work was to address the high power consumption issues faced by previous work implementing onboard ATR processing for vehicle classification on low-equity surveillance radar systems for UAV applications. A prototype of the RF transceiver was constructed using COTS hardware and minimal in-house fabrication; data from this system has been used to support the development of the signal processing architecture.

SAR Simulation

Simulated SAR imagery was constructed using the RaySAR engine proposed by Stephen Auer. The original simulator was modified to run in a pipelined fashion on the High Performance Compute clusters at UCL, and is now capable of producing 6000 images per hour on a single node.

A convolutional neural network, Tiny-YOLO, was used to classify simulated SAR images of vehicles. Work is ongoing to improve the realism of the generated imagery through a programme of modifications to the existing RaySAR package, and to integrate the ATR analysis into a full closed-loop system.

Hardware

The radar transceiver operates at X-band with programable bandwidths of up to 1 GHz. It is a direct conversion architecture based around a TI LMX2492 PLL; the waveform is programmed as a series of linear sections. Cavity antennas with dual FSS front planes are used for both transmit and receive channels.

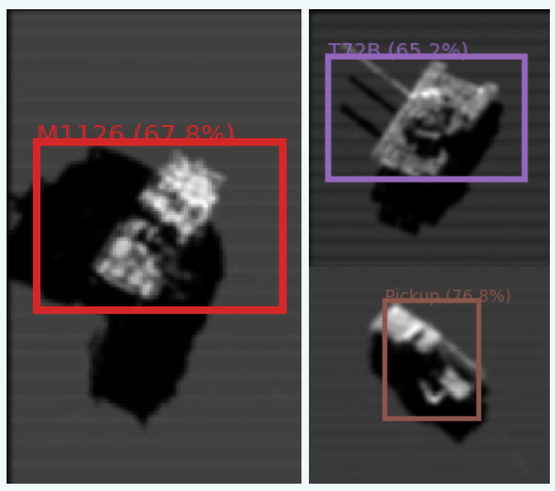
An accelerator for the filtered backprojection process has been developed as an ASIC design using VLSI techniques. The proposed architecture is parallelised on a per-pixel basis, making it scalable to the available die area, and is fully pipelined for maximum throughput. The current design was completed using an X-Fab 180 nm process, in anticipation of a trial production run.

Radar Results

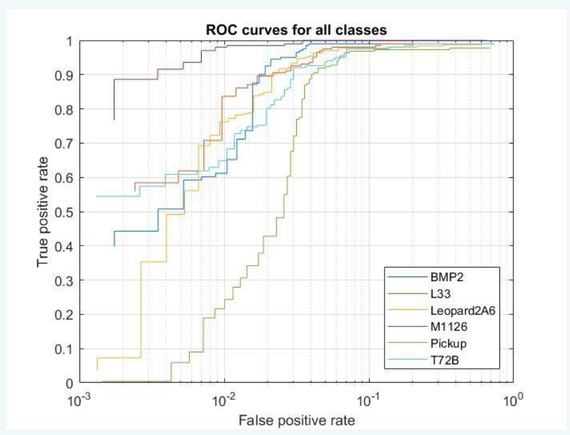
The radar unit has been tested in a number of configurations against a wide range of target. The first field trials demonstrated short-range mobility sensing and micro-Doppler capture against pedestrian targets. Later tests have shown mobility surveillance at greater ranges against small boats, and promising results have been achieved in SAR capture exercises, despite undersampled apertures.

Conclusions

This project has demonstrated significant performance advantages over previous FPGA-based architectures. Several routes for ongoing improvements have been identified, and this system appears set to support related research at UCL for several years to come.



Simulated bistatic SAR images showing vehicular targets and the associated predictions



ROC curves for multiclass classification using Tiny-YOLO classifier on simulated 15 cm resolution SAR imagery of vehicular targets from RaySAR

SAR Simulation

Packaged FMCW radar unit during field trials

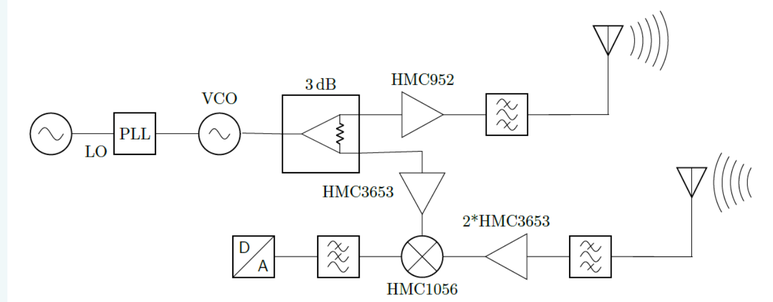
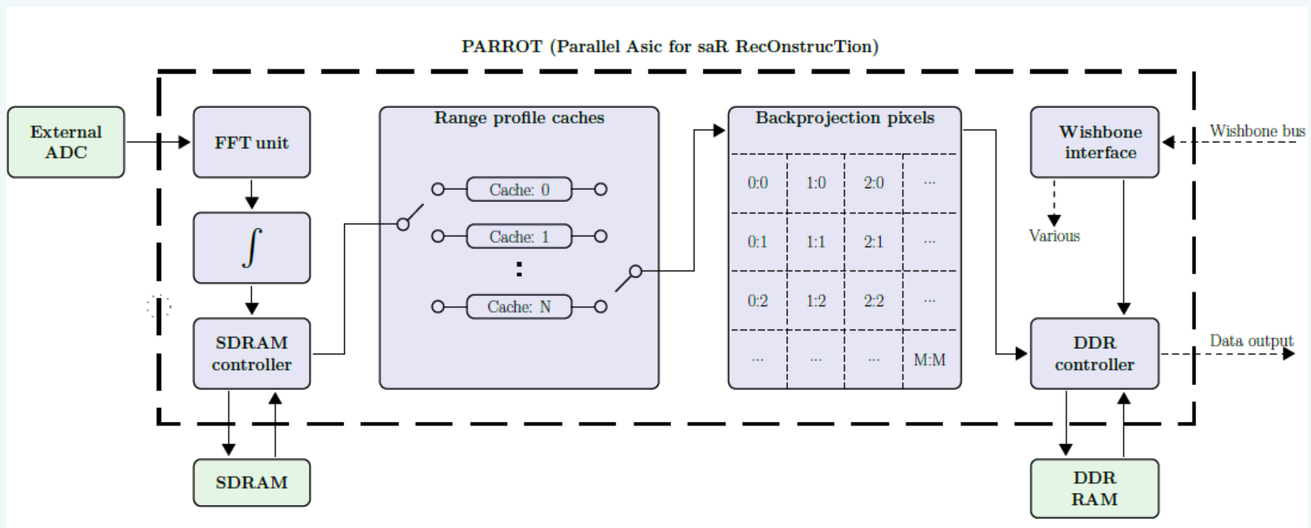


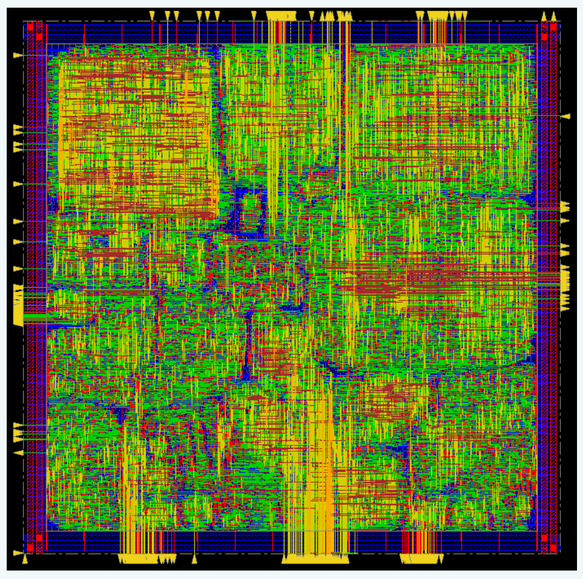
Figure 6.1: A high-level block diagram of the proposed homodyne transceiver

RF schematic for the radar unit used for trials. A second revision is being prepared for airborne tests during the summer

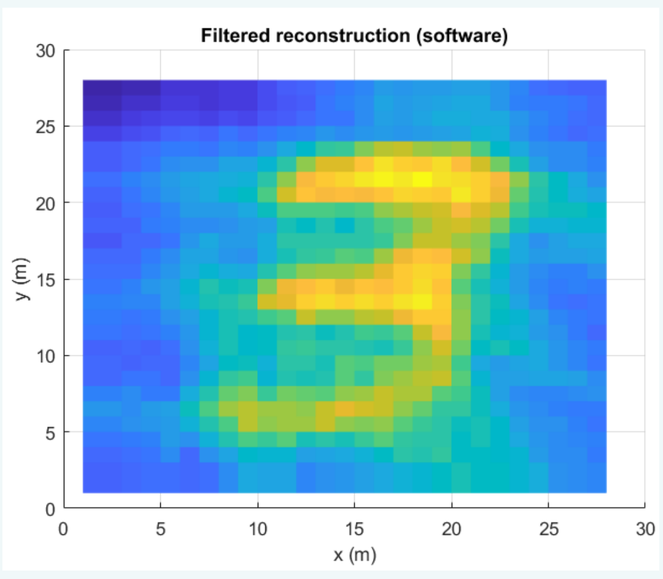
Build of an FMCW RADAR



Block diagram of proposed filtered backprojection accelerator, realised as an ASIC design

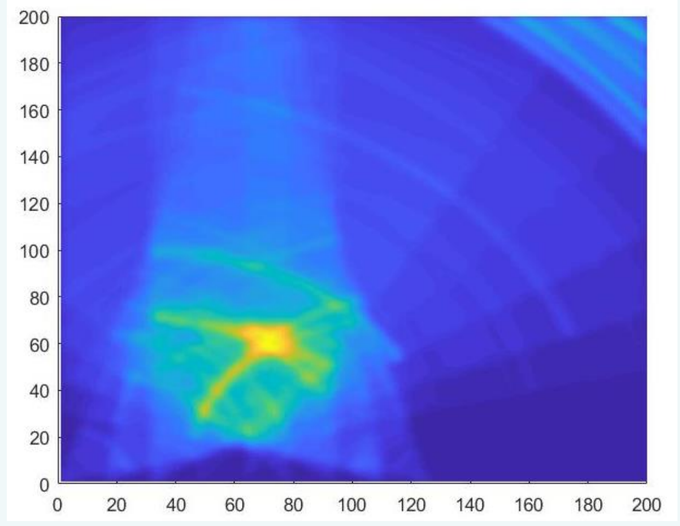


Routing display for 4-pixel PARROT implementation (Cadence Innovus)

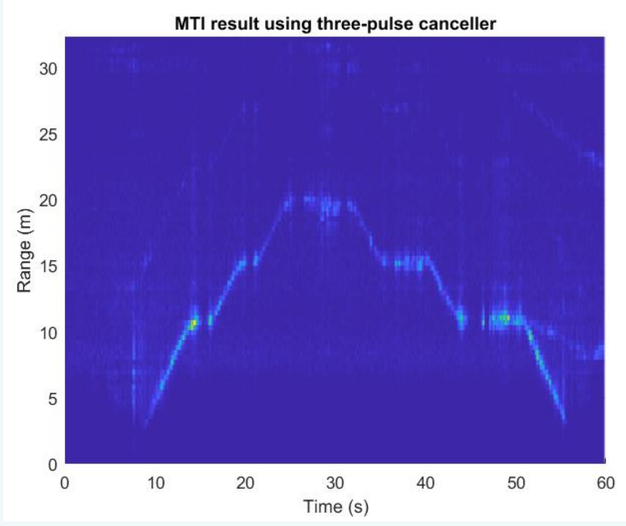


Reconstruction result from PARROT Verilog model for simulated MNIST target

ASIC Design For SAR ATR



Example spotlight mode SAR reconstruction for a small building in the UCL main quad



Example MTI for pedestrian target from initial field trials

Radar Signal Processing