Ultra–Broadband Common Collector-Cascode 4-cell Distributed Amplifier in 250nm InP HBT Technology with over 200 GHz Bandwidth

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Abstract—An ultra broadband MMIC amplifier is designed using InP double-heterojunction bipolar transistors and its on-chip measurements are reported. The multi-cell distributed amplifier uses four gain cells where each consists of a common collector input stage followed by a cascode gain stage. The chip includes bias, decoupling and terminating circuits for the dc and RF interconnects; it measures 0.72 mm by 0.4 mm. It consumes 210 mW of power and can deliver up to 5.5 dBm of output power at 195 GHz. The amplifier achieves an average gain of 13.5 dB with an overall bandwidth over 200 GHz and a $\pm$ 2 dB gain ripple. The measurements indicate that this is the widest band dc-coupled amplifier reported to date and has the highest bandwidth reported among non-cascaded distributed amplifiers.

I. Introduction

In today's electronic systems with ultra broadband communication links and the requirements for systems that can handle data at rates exceeding 100 Gbit/s, ultra-broadband amplifiers with high gain and high linearity have become a hot topic in research. Although traditionally distributed amplifiers (DA) have been designed using field effect devices [1], bipolar devices as such devices have advantages in terms of gain and linearity. The continuation of this trend was made possible with the introduction of newer fabrication techniques and materials, such as SiGe, InP and InGaP, that push the f_t and gain of the transistors into regions approaching the THz.

Distributed amplification is a design technique often used in order to achieve the gain and bandwidth requirements [1]. By connecting multiple, normally identical, amplification stages in input and output artificial transmission line (ATL) arrangements, the stage gains adds up while the bandwidth does not deteriorate as it would in cascaded topologies.

For bipolar based DAs, the gain stage is typically a simple common emitter (CE) cell, but recent works have utilized cascode cells in order to benefit of their higher bandwidth and high frequency gain compared to their CE counterparts. Multiple cell distributed amplification with bandwidths higher than 220 GHz has been demonstrated recently using cascode cells [2]–[5].
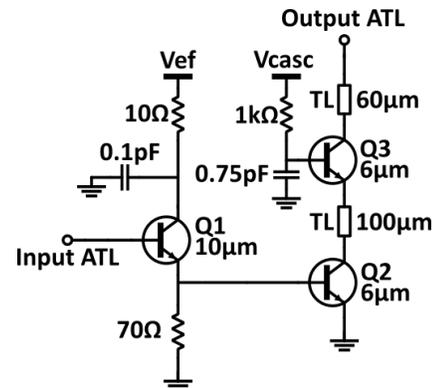

Fig. 1: Schematic of a single gain cell.

The cascode gain cell solves the serious bandwidth limitation associated with Miller capacitance of the CE, however an important gain limitation still exists in the form of the resistive input impedance of the cascode. That in turn means that the input transmission line will be lossy, thus introducing more attenuation for every successive gain cell, eventually resulting in a zero net gain with added cells [6].

In this work we demonstrate a practical implementation and measurements of a distributed amplifier with cells comprising a common collector (CC) input stage followed by a cascode gain stage, in a topology similar to that proposed by Kobayashi etal in [7]. The common collector transforms the input capacitance of the cascode (C_π) to a negative impedance at the input, reducing the input losses of the ATL. This, however, comes at the expense of extra power consumed by the CC stage. DAs based on the the common collector-cascode (CC-cascode) topology have been reported using InP double heterojunction bipolar transistor (DHBT) to achieve 120 GHz bandwidth [8].

II. Design

The amplifier is designed in an InP double heterojunction bipolar transistor process with $250\,\mathrm{nm}$ emitter width provided by Teledyne Scientific Company. The process has a current unity-gain frequency (f_t) of $350\,\mathrm{GHz}$ and a maximum frequency of oscillation (f_{max}) of $650\,\mathrm{GHz}$. The HBT models
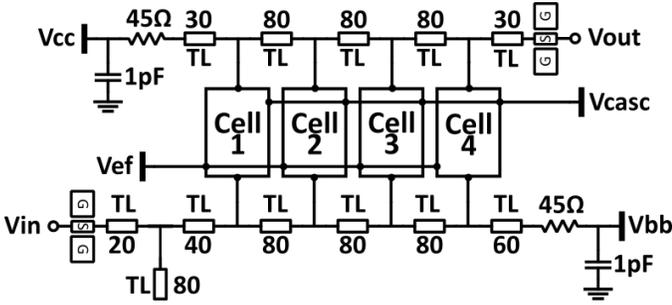
Fig. 2: Schematic of the complete DA. Transmission line dimensions in μm.

were also provided by Teledyne Scientific company. The process is described in more detail in [2].

A. Cell Design

The proposed topology enhances the previous design described in [2] by including a common collector stage at the input of each gain cell. The schematic of the cell is shown in Fig. 1. The current of transistor *Q1* is selected to achieve optimum matching of each cell to the input ATL and to the cascode gain stage that follows it.

The main gain stage is composed of transistors in a cascode configuration with a $100\,\mu m$ inter-stage peaking transmission line between them, and an additional $60\,\mu m$ peaking transmission line between the collector of the common base stage and the output ATL. The cascode topology increases the bandwidth by diminishing the effects of the Miller capacitance of *Q2* and provides increased isolation between the output and input of the gain cell. The bias current of the 2 cascode-stage identical transistors *Q2* and *Q3* is optimized for the best possible bandwidth and acceptable gain.

B. Amplifier Design

The artificial transmission lines (ATL) were designed to achieve approximately $50\,\Omega$ matching across the whole band of operation, from near dc to $200\,GHz$. M-sections [1] were used at the output line to enhance the high frequency behaviour through using $60\,\mu m$ peaking transmission line at the collector of *Q3*. The complete DA schematic is shown in Fig. 2.

The L-sections in both the input and output line have a length of $80\,\mu m$ or $2\times40\,\mu m$. The first and last segments on each line however, are not half-length, but have been co-optimized for the best input and output matching based on the simulated performance of the design. The input line includes an $80\,\mu m$ open stub to improve the input matching.

Both the input and output ATLs are designed to have $50\,\Omega$ impedance and to, respectively, accomodate the CC base bias current (from V_{bb}) and the cascodes collector bias current (from V_{cc}), to pass through. The termination resistances on both ATLs were optimized to $45\,\Omega$. The dc decoupling on chip is done with $1\,pF$ capacitors placed close to dc pads.

The CC collector bias voltage (V_{ef}) and the cascode base bias voltage (V_{casc}), use small decoupling capacitors on each cell as seen in Fig. 1.

TABLE I: Bias conditions of the measurements.

		V_{cc}	V_{ef}	V_{casc}	V_{bb}
High BW	V (V)	4.8	3.2	3.2	1.612
	I (mA)	23.15	40.2	1.1	1.8
High Gain	V (V)	4.6	3.3	3.2	1.62
	I (mA)	28.2	41.8	1.2	2.1

The input and output RF pads (V_{in}, V_{out}) do not include dc blocking capacitors since the amplifier is designed to operate from dc.

III. RESULTS

A microphotograph of the amplifier chip is shown in Fig. 3 where the dc pads, RF pads and a single cell are highlighted. The chip has dimensions of $720\,\mu m \times 400\,\mu m$.

A. Measurement Setup

Since the bandwidth of the DA is so wide, there is no single measurement setup to cover the whole spectrum. Due to the lack of such equipment, the measurement was separated into three different bands of interest: $100\,MHz - 67\,GHz$, $70\,GHz - 120\,GHz$ and $140\,GHz - 220\,GHz$. The low frequency ($100\,MHz - 67\,GHz$) measurements were done with Anritsu ME7838A vector network analyzer (VNA) with included dc-block capacitors, via coaxial Cascade Infinity $67\,GHz$ GSG probes. The $75\,GHz - 110\,GHz$ measurements were done using Keysight PNA-X N5247A with VDI WR-10 frequency extenders and WR-10 waveguide probes. The $140\,GHz - 220\,GHz$ measurements were done in a similar fashion using VDI WR-5.1 frequency extenders and WR-5.1 waveguide probes. The splitting of the bandwidth in different bands resulted in a non-continuous frequency response.

The measurements were done under two different dc bias conditions, optimized empirically for maximum bandwidth and for higher gain respectively. The biasing was done via dc-probes which included additional dc-decoupling capacitors. The bias voltages and currents for the two bias conditions are given in Table I.

The tile was mounted on a $300\,\mu m$ thick lossy silicon substrate in order to reduce substrate resonances [9]. Additionally, for the high frequency measurements, great care has been
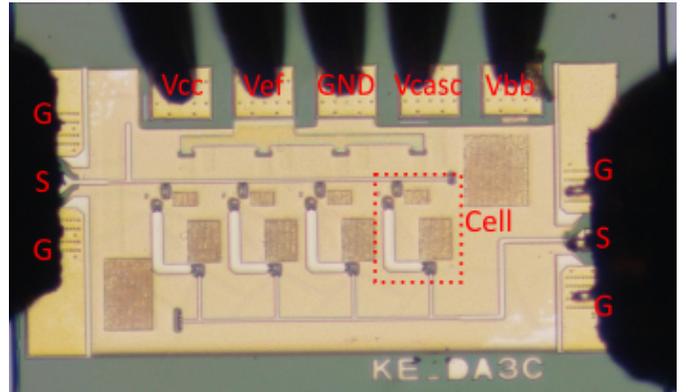

Fig. 3: Microphotograph of the fabricated MMIC.

taken to probe at the very edge of the RF pads, in order to avoid the introduction of an open stub behind the probe tip which would negatively affect the matching [10].

B. Small Signal Response

The measured S-parameters of the DA and its simulated results (dashed line) are presented in Fig. 4. The DA has a gain of gain of $13.5\,\mathrm{dB}$ $\pm 2\,\mathrm{dB}$ and a measured $3\,\mathrm{dB}$ point at $207\,\mathrm{GHz}$. In the low frequency region, the measurements show a resonance peak at $5\,\mathrm{GHz}$ in the S_{21} which matches a resonance in S_{11} and S_{22}. These may be attributed to the combination of dc-probe inductances and insufficient dc-decoupling and would be expected to disappear when mounting the MMIC on a carrier board and using additional dc-decoupling capacitors on the dc bias supplies.

A comparison between the simulated and measured S-parameters indicates some disagreement and that the simulation over-estimates the bandwidth by $\approx 15\%$. This is not surprising, especially given the potential lack of accuracy of the device models provided in the design kit at high frequencies.

When the DA is driven in the high gain bias configuration, the average gain increases to $16.5\,\mathrm{dB}$ but the bandwidth suffers compared to the high bandwidth configuration and is reduced to nearly $140\,\mathrm{GHz}$. The main physical effect that facilitates this performance change is the increase of Vcc, which in turn increases the current density of the cascode configured transistors. The higher current increases the gain, but the output impedance of the cascode changes, which in affects both the peaking of the cell and the ATL overall impedance.

C. Large Signal Response

Two different measurement setups were utilized to measure the output power of the amplifier. A $100\,\mathrm{MHz} - 100\,\mathrm{GHz}$
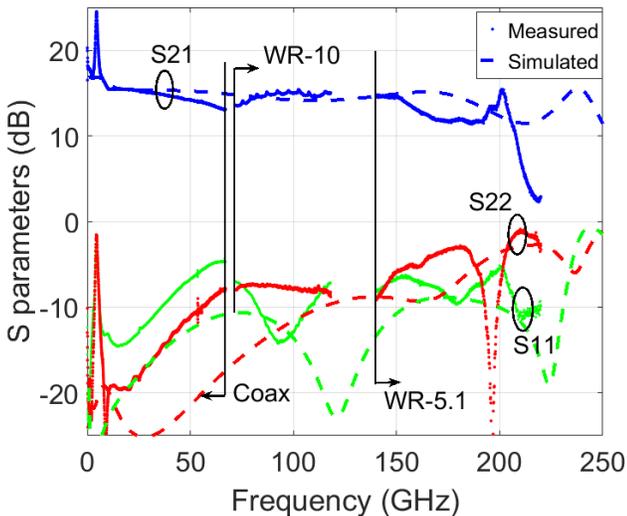

Fig. 4: S-parameters of the DA vs frequency in the three measured bands, for -20 dBm input power along with the simulated results (dashed line).
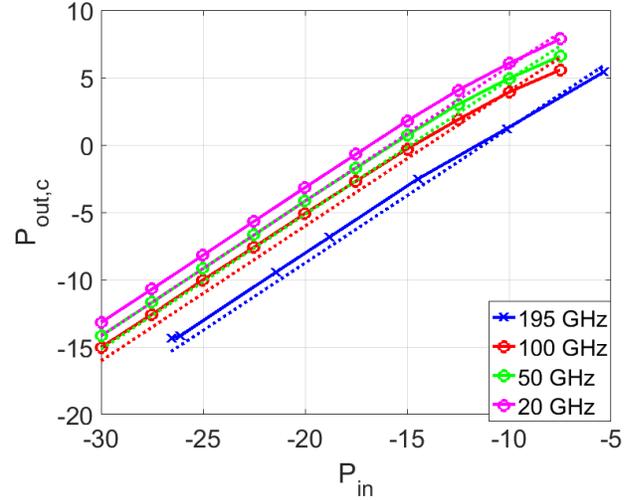

Fig. 5: $P_{out,calc}$ versus P_{in} for various frequency points (solid lines) along with their respective 1-dB compression lines (dashed lines).

measurement with input power ranging from -30 dBm to -7.5 dBm, in which the DA was biased at the high gain configuration and a $140\,\mathrm{GHz} - 220\,\mathrm{GHz}$ measurement, with input power between -25 dBm to -5 dBm in which the DA was biased at the high bandwidth configuration.

From the measurements, S_{21} and P_{in} data were extracted and the output power was calculated from (1). The resulting plots for several frequency points are presented in Fig. 5.

$$P_{out}(\mathrm{dBm}) = S_{21}(\mathrm{dB}) + P_{in}(\mathrm{dBm}) \qquad (1)$$

Fig. 5 shows that in the high gain configuration the compression point is around -9 dBm of input power and it remains relatively unaffected by frequency variation. The calculated output power at the 1 dB compression point is close to $6.7\,\mathrm{dBm}$ for $20\,\mathrm{GHz}$ and drops to $3.7\,\mathrm{dBm}$ at $100\,\mathrm{GHz}$.

In the high bandwidth bias condition, at $195\,\mathrm{GHz}$, the compression behaviour is similar to that of the high gain condition. The calculated output power 1 dB compression point is, however, lower at $1.9\,\mathrm{dBm}$ due to the reduced gain at this frequency. At the highest input power, the amplifier can output up to $5.5\,\mathrm{dBm}$ of power without reaching saturation. More detailed results from the aforementioned measurements are presented in Table II.

D. Comparison with literature

A comparison of the designed DA with other state-of-the-art DAs found in literature is presented in Table III.

As shown in the table, the amplifier presented in this paper has the highest bandwidth of all single ended, single

TABLE II: Power compression for various frequency points.

Frequency (GHz)	20	50	100	195
$P_{in,comp}$ (dBm)	-9.1	-9.8	-10.3	-9.3
S_{21} meas. (dB)	16.8	15.8	15.0	12.2
P_{out} calc. (dBm)	6.7	5	3,7	1.9

TABLE III: Comparison with state-of-the-art DAs in literature.

Technology	BW (GHz)	Gain (dB)	GBW (GHz)	Pdc (mW)	Area (mm^2)	Output power (dBm)	DA Topology	Ref
700 nm InP HBT	120	21	1346	610	2	-	CC-Cascode	[8]
250 nm InP HBT	182	10	576	105	0.33	8.5 @134 GHz	Cascode	[3]
250 nm InP HBT	180	12.8	786	110	0.32	-	Cascode	[2]
250 nm InP HBT	235	16	1480	117	0.41	-	Cascode 2-CS	[2]
130 nm SiGe HBT	170	19	1515	560	0.91	13.5 @134 GHz	Stacked trans.	[11]
55 nm SiGe HBT	135	8.5	359	99	0.36	∼9.5 @20 GHz	Cascode	[5]
130 nm SiGe HBT	170	13	759	74	0.22	-	Cascode 1-CS	[12]
130 nm SiGe HBT	180	18.7	1550	86	0.61	2.5 @100 GHz	Cascode 3x4CS	[13]
250 nm InP HBT	**207**	**13.5**	**980**	**210**	**0.288**	**5.5 @195 GHz**	**CC-Cascode**	**This work**

stage, multi-cell distributed amplifiers. To the authors best knowledge, there is only one design with higher bandwidth; a two-stage single cell distributed amplifier presented in [2]. However, that amplifier had input, output and dc-blocking capacitors in order to cascade the two stages, therefore suffers in the lower end of the frequency spectrum and can not function at dc.

The CC-cascode amplifier described in this work is more suitable for applications where performance down to dc is required and therefore is usable in ultra high bit rate optical communication links where no line coding is used and therefore long strings of 1's and 0's may be encountered [14]. However, the power consumption would suffer in that case due to the current consumption of the termination resistor. With a 207 GHz bandwidth and a GBW product of 980 GHz, this amplifier has the widest bandwidth of all reported distributed amplifiers operating from dc, although with a higher power consumption, due to the use of the additional common collector stages. Furthermore, it is our view that this amplifier is the best performing ultra wide band amplifier to-date, in terms of its power handling capabilities; up to 5.5 dBm output power can be reached at frequencies up to 195 GHz without saturation.

IV. Conclusion

A dc to 207 GHz ultra-broadband amplifier is reported with an average gain of 13.5 dB and a gain ripple of ± 2 dB giving it a gain-bandwidth product of 980 GHz. The amplifier is a 4 cell distributed amplifier where each cell is a CC-cascode configuration designed with optimized artificial transmission lines to allow extended bandwidth operation.

Comparison of the measured to the simulated S-parameters show slight overestimation of the bandwidth which is attributed to the possibility of inaccurate device models at high frequencies. The amplifier is measured to provide uncompressed output power of 1.9 dBm and up to 5.5 dBm at 195 GHz without saturating. The amplifier MMIC consumes 210 mW of power.

To the authors' best knowledge, given the over 200 GHz bandwidth, this amplifier sets the world record in being the widest band reported amplifier operating from DC.

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