

Investigation of Resistance Switching in SiO_x RRAM Cells Using a 3D Multi-Scale Kinetic Monte Carlo Simulator

Toufik Sadi^{1,2*}, Adnan Mehonic³, Luca Montesi³, Mark Buckwell³, Anthony Kenyon³, and Asenov¹

¹School of Engineering, Electronic and Nanoscale Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK

²Department of Neuroscience and Biomedical Engineering, Aalto University, P.O. Box 12200, FI-00076 AALTO, Finland

³Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, UK

*Email: Toufik.Sadi@aalto.fi

Abstract

We employ an advanced three-dimensional (3D) electro-thermal simulator to explore the physics and potential of oxide based resistive random-access memory (RRAM) cells. The physical simulation model has been developed recently, and couples a kinetic Monte Carlo study of electron and ionic transport to the self-heating phenomenon, while accounting carefully for the physics of vacancy generation and recombination, and trapping mechanisms. The simulation framework successfully captures resistance switching, including electroforming, set and reset processes, by modeling the dynamics of conductive filaments in the 3D space. This work focuses on the promising yet less studied RRAM structures based on silicon-rich silica (SiO_x) RRAMs. We explain the intrinsic nature of resistance switching of the SiO_x layer, analyze the effect of self-heating on device performance, highlight the role of the initial vacancy distributions acting as precursors for switching, and also stress the importance of using 3D physics-based models to capture accurately the switching processes. The simulation work is backed by experimental studies. The simulator is useful for improving our understanding the little-known physics of SiO_x resistive memory devices, as well as other oxide-based RRAM systems (e.g. transition metal oxide RRAMs), offering design and optimization capabilities with regard to the reliability and variability of memory cells.

1. INTRODUCTION

Resistive random-access memories (RRAMs) are promising nonvolatile memory based devices. They have attracted considerable attention in the last 10 years [1]–[15]. The 2010 International Technology Roadmap for Semiconductors (ITRS) report on emerging devices details the incentives for developing RRAM device technologies, namely reduced power dissipation and cost-per-bit, increased endurance, and suitability for chip incorporation as 3D crossbar arrangements. Resistive RAMs are suitable for a multitude of technological applications, including neuromorphic computing [16] and neural networks [17], [18].

RRAMs are often linked with the concept of memristors. The concept of a memristor was suggested in the 1970's [19], but it was only in 2008 that one of the first links between the theoretical framework and experiments was demonstrated, by using e.g. titanium dioxide (TiO_2) [13]. Several RRAM technologies are nowadays under investigation. In this context, oxide-based RRAMs represent one of the most studied device; materials of interest include metal oxides [13], such as TiO_x and HfO_x , and SiO_x [1], [20], [37]. There is also a huge interest in RRAMs based on phase-change materials, such as perovskites, Ge sulphide and selenide, and chalcogenides [10], [38], [39]; particularly, chalcogenide-based RRAMs [38], [39] show a great potential in applications based on the Programmable Metallization Cell (PMC) technology platform. There is also an interest in less known memristor structures, e.g. the ferroelectric memristor [7] whose operation is entirely due to electronic phenomena. Transition metal oxides (TMOs) are generally characterized by a high dielectric constant, which is a highly desirable feature towards high-density electronic integration. While RRAMs based on TMOs are nowadays considered as the most promising technology, they face many significant challenges, most notably Si microelectronics integration. On the other hand, the development of RRAM devices based on silicon-rich silica (SiO_x ; $x < 2$), as studied in this article, can potentially result in low-cost integration in silicon CMOS chips.

This article is organized as follows. In Section 2, we discuss the current progress in RRAM device modelling and the main features of our simulator. In Section 3, we present a detailed description of the simulation framework. In section 4, we show results from the application of the simulator to $\text{TiN/SiO}_x/\text{TiN}$ RRAM structures. The results are analysed and their significance is discussed. In section 5, we make conclusions about the main results and the simulation work is general.

2. RRAM SIMULATION: STATE-OF-THE-ART AND BEYOND

Resistance switching in oxide RRAMs occurs via the electro-formation and rupture of conductive filaments (CFs) in the oxide [1], as oxygen vacancies are created and ions are redistributed under the influence of the local electric field and temperature distribution. Most work on RRAMs focuses on devices based on TMOs, as highlighted above. Moreover, previous RRAM simulation studies relied heavily on phenomenological modeling techniques (e.g. the resistor breaker network method) [14], [33] and two-dimensional approaches [9], [22]. These models do not calculate in a self-consistent manner the electric fields and do not consider accurately the physics of device self-heating (heat generation and conduction).

The drive to develop reliable simulation models for RRAMs is still strong, as illustrated by the continued increase in the number of publications on this topic (please see Refs. [29]–[33]). There is an interest in both developing advanced models – of analytical (e.g. Ref. [32]), circuit-based

(e.g. Ref. [33]) and multi-physical (e.g. Ref. [29]–[31]) nature – and studying specific effects such as the crosstalk effect [29]. Continuous efforts are also made to understand further the physics of SiO_x RRAM structures [34].

We utilize a recently developed three-dimensional (3D) kinetic Monte Carlo (KMC) simulator to investigate the behavior of SiO_x RRAM memory cells. The novel aspects of our work lie in the advanced features of our simulator as well as in the focus on the less-studied but highly-interesting SiO_x RRAM devices. Our modeling approach has unique capabilities that distinguish it from previously presented models [9], [14], [22]. Firstly, the simulator employs a powerful framework, considering electron-ion interactions to reconstruct realistically the electroforming and rupture of the CF in the 3D real space. Secondly, it couples in a self-consistent fashion time-dependent oxygen ion and electron transport (stochastic KMC) simulations to the local temperature and electric field 3D distributions, determined by solving the relevant physical equations. Thirdly, the simulator accounts accurately for the dynamic nature of the ion-vacancy generation process in SiO_x, as detailed in [23]. **Fourthly**, the simulator accounts carefully for trapping dynamics and electron transport mechanisms in the oxide [24], [25]. **Fifthly**, the simulation work is supported by experimental studies by the authors demonstrating switching in SiO_x RRAMs at room temperature (see e.g. Refs. [1], [26]).

3. SIMULATION METHODOLOGY AND STUDIED RRAM DEVICES

We study the SiO_x-based structure shown in Fig. 1 [26]. The structure consists of a SiO_x layer of thickness $H=10\text{nm}$ sandwiched between two titanium nitride (TiN) contacts. The TiN plates in an experimental device have a typical area of $100\mu\text{m}\times 100\mu\text{m}$ [1]. In this study, we can limit this simulation study to a much smaller area (e.g. $L\times W=20\text{nm}\times 20\text{nm}$), corresponding to a region containing e.g. a grain boundary. Indeed, experiments by the authors suggest the existence of only one dominating conductive filament per plate [1], in typical structures. The simulation framework involves the rigorous time-dependent coupling of electron and oxygen ion dynamics to the local temperature and electric field in the oxide volume. The flowchart shown in Fig. 2 illustrates the simulation procedure. Figure 3 illustrates the mechanisms governing electron transport in the oxide. The simulator is supported by experimental results obtained from SiO_x RRAM devices [1], [26], **as discussed before**. The simulator employs a structure generation editor, which allows the building of a device structure of any arbitrary geometrical features and material composition.

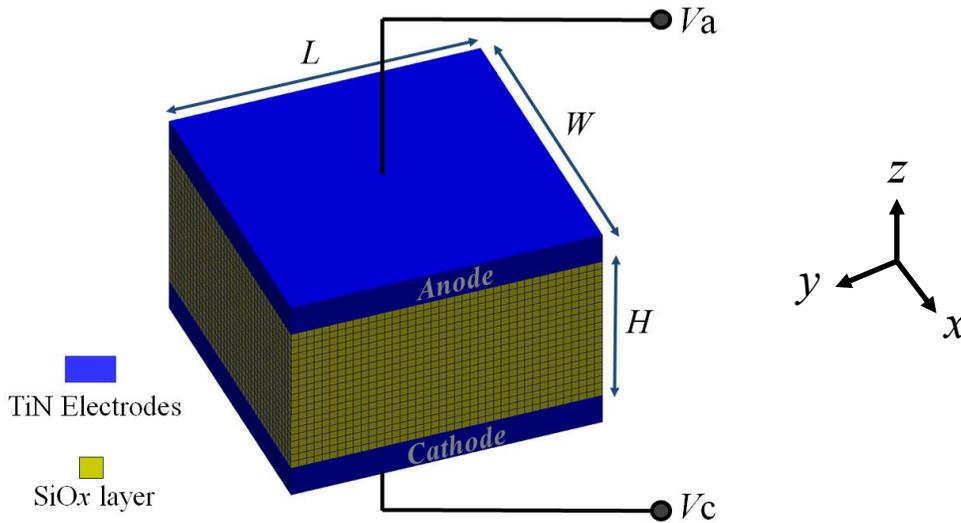


Fig. 1. The simulated SiO_x RRAM structure, with an oxide layer of thickness $H=10\text{nm}$ sandwiched between two TiN contacts. While experimental devices have typical areas of $100\mu\text{m}\times 100\mu\text{m}$ [1], we can limit the simulations to a much smaller (Si-rich) area (e.g. $L\times W=20\text{nm}\times 20\text{nm}$), corresponding to a region containing e.g. a grain boundary.

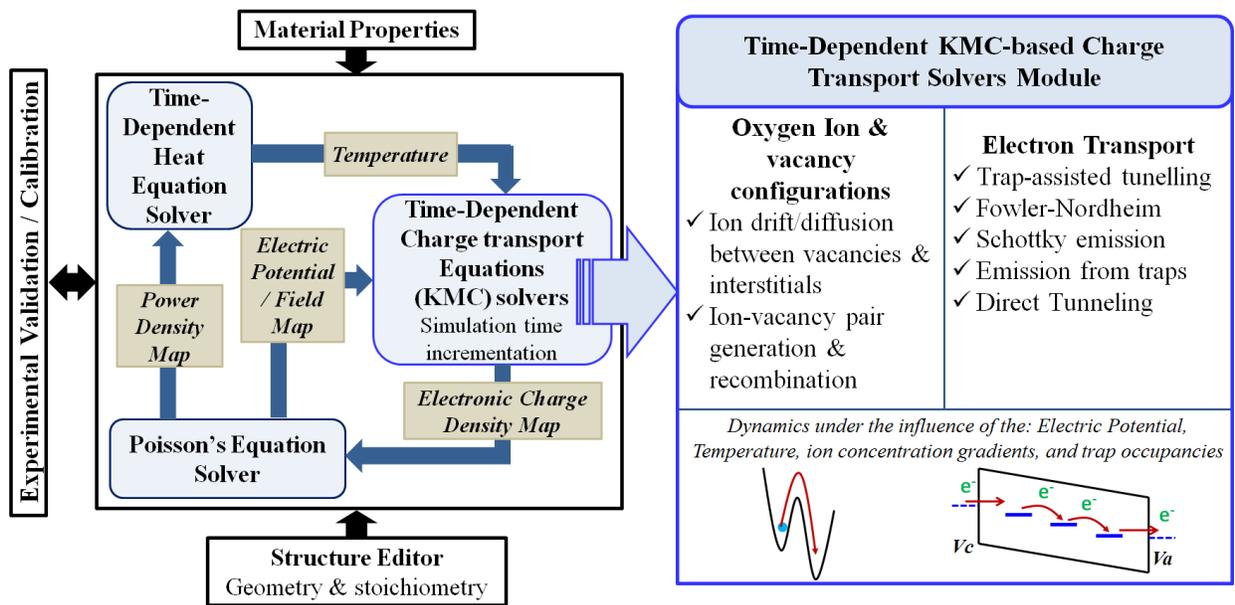


Fig. 2. The full simulation procedure, which involves the self-consistent coupling of KMC description of the electron and oxygen ion transport phenomena to the temperature and electric field distributions in the oxide volume. The simulator accounts carefully for the dynamic nature of the ion-vacancy generation mechanism.

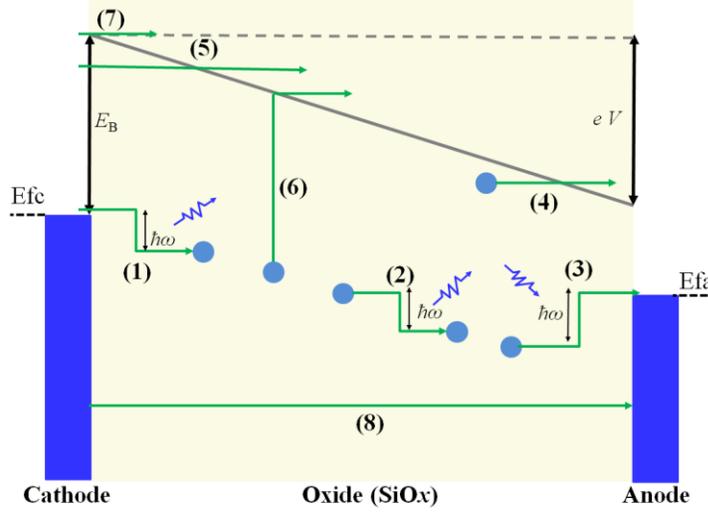


Fig. 3. The mechanisms governing electron transport, as implemented in the simulator. They include trap-assisted tunneling processes [i.e. (1) electrode-to-trap tunneling, (2) trap-to-trap tunneling, and (3) trap-to-electrode tunneling, (4) electron tunneling from a trap to the conduction band (CB)], (5) Fowler-Nordheim tunneling mechanism, (6) Poole-Frenkel mechanism (emission of an electron from a certain trap to the CB), (7) Schottky emission, and (8) direct electron tunneling (from one contact terminal to another).

3.1. Ion and Vacancy Dynamics

The simulator allows the accurate study of switching through the formation and destruction of conductive filaments. Oxygen ion drift and diffusion between vacancies and interstitial sites, and ion-vacancy generation and recombination events are modelled via a stochastic kinetic Monte Carlo (MC) model. The KMC method effectively solves for the following equation, governing oxygen ion transport:

$$\frac{\partial n_l(\vec{r}, t)}{\partial t} = \nabla \cdot [D \nabla n_l(\vec{r}, t) - V_{ion} n_l(\vec{r}, t)] + G, \quad (1)$$

where n_l is the oxygen ion concentration, D is the diffusivity, V_{ion} is the ion velocity, and G is the net ion generation rate. In principle, vacancies can also move. However, the inclusion of vacancy dynamics is not important in the studied devices, as their diffusion barrier is very high (4eV, as compared to 0.3eV for ions). As the field and temperature distributions are updated regularly, relevant physical quantities are re-calculated, including the attempt-to-escape rate for oxygen to jump over the barrier P_g (ion-vacancy generation rate), and the probability of ion-vacancy recombination P_r :

$$P_g = f_0 \exp \left[-\frac{(E_a - \gamma e E)}{k_b T} \right], \quad (2)$$

$$P_r = C_{ion} f_0 \exp \left[-\frac{(E_r - \gamma e E)}{k_b T} \right], \quad (3)$$

where E_a is the formation energy, E_r is the recombination barrier, γ is the contribution of the bond polarization to the local electric field \mathbf{E} (with magnitude E), C_{ion} is the ion concentration, T is the lattice temperature, k_b is the Boltzmann constant, and e is the electronic charge. The generated ions

move through lattice sites (including interstitials and vacancies), either by drifting with an average velocity V_{ion} (field and temperature-assisted ion hopping), or diffusing according to the related diffusion constant D . Ions drift or diffuse according to probabilities P_{dr} and P_{df} given by:

$$P_{dr} = f_0 \exp\left(-\frac{(E_m - eaE)}{k_b T}\right), \quad (4)$$

$$P_{df} = \frac{1}{2} f_0 \exp\left(-\frac{E_m}{k_b T}\right), \quad (5)$$

leading to average velocities and diffusion constants given be:

$$V_{ion} = af_0 \exp\left(-\frac{E_m}{k_b T}\right) \sinh\left(\frac{eaE}{2k_b T}\right), \quad (6)$$

and

$$D = 1/2a^2 f_0 \exp\left(-\frac{E_m}{k_b T}\right), \quad (7)$$

where a is the lattice constant and E_m is the oxygen migration barrier. The values of relevant parameters are summarized in [Table 1](#), which are collected from selected publications including [27] and [28].

For the reliable modelling of switching in SiO_x RRAM devices, the process of vacancy generation through bond breakage needs to be carefully accounted for. Extensive data related to bond breakage and breakdown in silica has been collected, as reported in Ref. [27]. Two sets of values have been suggested for the activation energy (E_a) and the contribution of the bond polarization to the local electric field parameter (γ): (i) $E_a=1\text{eV}$ and $\gamma=7\text{e}\text{\AA}$, and (ii) $E_a=2\text{eV}$ and $\gamma=13\text{e}\text{\AA}$. Both data sets (i) and (ii) give a breakdown field of ~ 15 MV/cm. We use the vacancy generation model reported by the authors in Ref. [23]. In this model, a generation event produces an oxygen vacancy and a negatively charged oxygen interstitial ion O^{2-} . The generated ion moves rapidly through the oxide layer (with a migration barrier of around 0.3eV), as discussed in previous experimental work [28]. While the normal generation process data are used in SiO_2 ($E_a=1\text{eV}$ and $\gamma=7\text{e}\text{\AA}$), Ref. [23] describes how oxygen vacancies occupied by two electrons result in lowering E_a ($<1\text{eV}$; $\sim 0.7\text{eV}$) and enhancing the generation rate in defect-rich areas. The recombination process is assumed to be the exact reverse process of the generation mechanism with a recombination rate $P_r = C_{\text{ion}} P_g$, where C_{ion} is the relative concentration indicating the presence ($C_{\text{ion}}=1$) or absence ($C_{\text{ion}}=0$) of an ion at a vacancy site. As is the standard practice (see e.g. Ref. [35]), recombination only occurs if the vacancy is depleted of electrons to satisfy charge conservation.

Table 1. The main parameters used in the simulations, which are collected from selected publications including [27] and [28].

Parameter	Value
f_0 : vibration frequency	10^{13} s^{-1}
E_a : formation energy	1eV
E_r : recombination barrier	1eV
E_m : Oxygen migration barrier	0.3eV
a : Lattice constant	5Å
γ : contribution of the bond polarization to the local electric field	7eÅ

3.2. Electron Transport

In principle, there are several mechanisms influencing electron transport in oxide-based RRAM structures, as considered in this work and illustrated in Fig. 3. The mechanisms include trap-to-trap tunneling (Mott hopping), electrode-to-trap and trap-to-electrode tunneling, Schottky emission, Fowler-Nordheim tunneling, Poole-Frenkel emission (from traps to the conduction band (CB)), tunneling from traps to the CB, and direct tunneling from one electrode to the other [24]. Careful consideration of trap-assisted tunneling (TAT) is especially necessary to update correctly the traps occupancy. In this work, we track down the trapped electron population in the oxide and update the trap occupancies using the kinetic Monte Carlo simulator, instead of the previously used current solver presented in [9]. Below is a discussion of the dominating transport mechanisms, including trap-assisted tunneling. Other mechanisms are thoroughly discussed in literature (see e.g. Ref. [24]).

1) *Trap-to-trap hopping*: Trap-to-trap hopping, also referred to as Mott hopping, is an important mechanism for electric conduction in relatively thick oxide layers, as considered here (see e.g. Ref. [24] for more information). Consider two trap states located at a distance R apart, with energies E_1 and E_2 . In the case “ $W = E_1 - E_2 > 0$ ”, an electron hops from vacancy (1) to vacancy (2) by the **emission** of phonons with a total energy $W = p\hbar\omega$, with a hopping rate R_{1-2} :

$$R_{1-2} = f_0 \exp\left(-\frac{2R}{\xi}\right) f_1 (1 - f_2) \exp(-W/k_b T) \quad , \quad (8)$$

where f_0 is the vibration frequency, ξ is the localization length, f_1 and f_2 are the trap occupancies for the left and right traps respectively, and \hbar is the reduced Planck’s constant. Hopping from trap (2) to trap (1) is accompanied by the **absorption** of phonons (a total energy $W = p\hbar\omega$), with a rate R_{2-1} :

$$R_{2-1} = f_0 \exp\left(-\frac{2R}{\xi}\right) f_2 (1 - f_1) \quad (9)$$

2) *Electrode-trap tunneling*: Electric current flow through the contacts occurs via electrode-to-trap (ET) and trap-to-electrode (TE) tunneling mechanisms, as illustrated in Fig. 3. The tunneling from an electrode into a trap and the reverse process of emission of trapped electrons into the

electrode are described as a multi-phonon assisted tunneling process. The tunneling rates (to or from trap position z_T) are given by:

$$R_{ET}(E_e) = N(E_e)F(E_e)T_{ET}(E_e)c_{ET}(E_e, z_T), \quad (10)$$

and

$$R_{TE}(E_e) = N(E_e)[1 - F(E_e)]T_{TE}(E_e)c_{TE}(E_e, z_i), \quad (11)$$

where E_e is the tunneling electron energy, N is the density of states in the electrode, F is the Fermi-Dirac distribution function, T_{ET} and T_{TE} are the transmission coefficients, and c_{ET} and c_{TE} denote the corresponding electron-phonon scattering rates, as detailed in Ref. [24]. In this work, T_{ET} and T_{TE} are calculated using the Wentzel-Kramers-Brillouin (WKB) approximation, as follows:

$$T_{ET}(E_e) = \exp\left(-\frac{2}{\hbar} \int_{z_E}^{z_T} \sqrt{2m^*(E_C - E_e)} dz\right), \quad (12)$$

$$T_{TE}(E_e) = \exp\left(-\frac{2}{\hbar} \int_{z_T}^{z_E} \sqrt{2m^*(E_C - E_e)} dz\right), \quad (13)$$

where z_E is the electrode position, m^* is the effective oxide mass ($\sim 0.42m_0$ for SiO_2), and E_C is the conduction band.

3) *Trap levels:* To model accurately electron transport via trap-assisted tunneling, we need to employ reliable energy levels for the different traps that are present in the oxide. The types and details of the traps contributing to trap-assisted tunneling in SiO_x are described in Ref. [25]. In principle, any trap type (positively charged, neutral or negatively charged) can contribute to trap-to-trap hopping and other TAT mechanisms. Albeit, the rate can vary significantly with trap energy levels. Considering the thermal ionization energies E_T for each trap type (5eV for a positive vacancy; 3.37eV for a neutral vacancy;), the neutral oxygen vacancy is the defect assisting the electron TAT in silica, as highlighted in Ref. [25]. This is in contrast to HfO_x , where positive oxygen vacancies ($E_T=1.4-2.4\text{eV}$) assist the electron TAT mechanisms [25].

4) *Other mechanisms:* Considering the relatively thick oxide layer ($>10\text{nm}$), the probability of direct tunneling between the two electrodes is extremely low. At high applied biases, direct tunneling merges into the Fowler-Nordheim tunneling. These mechanisms are also modelled within the WKB approximation. As discussed in Ref. [24], these effects are only important when the conduction band offset (CBO) is very small, which is not the case for the $\text{TiN}/\text{SiO}_x/\text{TiN}$ structure studied here. Poole-Frenkel mechanisms start to visibly contribute to transport if large electric fields are applied [24]. In the simulated devices, Poole-Frenkel events are relatively rare considering the depth of the trap.

3.3. Self-Consistent Fields and Self-Heating

As the positions of oxygen ions and electrons at traps are tracked in time (and vacancies are created or destroyed), the local electric potential ϕ is updated self-consistently, according to the resulting charge distribution, using an in-house Poisson's equation solver in 3D. The simulator is efficiently designed to minimize computational time, which can be high due to the differences (up to few orders of magnitude) in the time scales between ionic and electron transport phenomena [36]. The

simulation framework uses an adaptive field-adjusting time, allowing accurate self-consistent field coupling with minimized cost. In this scheme, Poisson's equation is only solved when there is an event that leads to a change in the local charge density (e.g. an electron hopping/TAT event or an ion hopping event). The electric field is simply related to the local potential ϕ via the relationship $\vec{E} = -\nabla\phi$. Simultaneously, temperature rise due to self-heating is calculated by the resolution of the time-dependent heat diffusion equation (HDE)

$$\nabla \cdot [\kappa(\vec{r}, T) \nabla T(\vec{r}, t)] + g(\vec{r}, t) = \rho C \frac{\partial T(\vec{r}, t)}{\partial t}, \quad (14)$$

using an advanced in-house solver. In equation (14), T and g are the temperature and heat generation, respectively, at a given position \vec{r} and time t , κ is the temperature-dependent thermal conductivity, ρ is the material density and C is the specific heat capacity. The contributions of ion and electron dynamics to heat generation are determined by the dot product of the local field and current density vectors $\vec{J} \cdot \vec{E}$, assuming Joule heating is the dominant mechanism for dissipation. As in the standard practice in time-dependent stochastic (Monte Carlo) simulations, the local current density is also updated regularly, as ions and electrons move and vacancies are created or destroyed in the oxide.

3.4. Kinetic Monte Carlo Algorithm: Motivation and Application

In our previous publication [23], we highlighted the importance of trapping and electron-ion interactions in influencing the vacancy generation processes in SiO_x. To model such processes, it is important to track down the real occupancy of each trap in time, which can only be achieved using direct solvers based on the stochastic KMC algorithm, not just for ions, but also for electrons. In this case, steady-state models are not best suited for studied SiO_x RRAM devices.

1) *KMC algorithm for ions:* The simulator constructs the device geometry by assuming a 3D matrix of SiO₂ molecules and (initial) oxygen vacancies at lattice sites, sandwiched between two contacts where Dirichlet boundary conditions are imposed. Ion-vacancy generation events are selected (in time) according to the probability P_g using random numbers. As ions are generated, they move from one lattice point to another neighbouring lattice point, which can be either a vacancy or an interstitial, or to one of the electrodes. The trajectory of a moving ion is selected using the KMC algorithm, by building cumulative drifting and diffusion probability (P_{dr} and P_{df}) ladders (considering all possible neighboring lattice sites and/or electrodes) and using a random number to choose the subsequent destination of each ion. Similar to the generation process, an ion-vacancy recombination process is selected randomly according to probability P_r .

2) *KMC algorithm for electrons:* Similar to the ion KMC algorithm, we model electron movements according to the hopping and tunneling rates given by equations (8)–(13). For each electron in the oxide layer, we build a cumulative hopping and tunneling rate ladder including all possible destinations (vacancies or electrodes). The final destination is selected from the ladder using a random number. Furthermore, electrons are injected from the electrodes (to occupy a vacancy or tunnel through) using the same cumulative ladder approach, considering rates from equations (10)–(13).

4. RESULTS AND DISCUSSION

First, we discuss how the experimental studies of the SiO_x RRAM devices guide the simulation work. Then, we validate and illustrate the capabilities of our simulator by studying the corresponding structures. Finally, we discuss the importance of 3D KMC modelling and self-heating, and show how the initial concentrations of intrinsic traps can affect resistance switching.

4.1. Experimental Characteristics

Figure 4 demonstrates the operation of SiO_x RRAMs by showing an example of experimental I - V characteristics, including the electroforming, set and reset processes, for a typical $\text{TiN}/\text{SiO}_x/\text{TiN}$ structure. The I - V curve demonstrates a typical unipolar mode of resistance switching. Electroforming and set processes are obtained by sweeping the devices and applying the current compliance to prevent hard breakdown. The reset process occurs in the same polarity at the voltages lower than the set voltage, by removing the current compliance and allowing the higher current to pass through the device. Our structures include defect/Si-rich regions, which in general facilitate the creation of CFs, by allowing lower forming/set biases, as compared to pristine structures. Previously (experimentally) studied metal-free poly-Si/ SiO_x /Si structures [1] showed similar behavior. Also, many studied experimental devices showed surface oxygen bubbles at the anode related to oxygen emission during operation [26]. The results lead to the conclusion that switching is an intrinsic property of the SiO_x layer, and SiO_x RRAMs do not require the diffusion of metallic ions (which can affect adversely the surrounding devices), and confirm that including the metallic diffusion in our model is not necessary. Also, as compared to pristine SiO_2 structures, the existence of Si-rich regions minimizes the possibility of hard breakdown and hence irreversible ON/OFF state transitions. In Ref. [1], the authors reported devices that can be cycled between high resistance OFF and low resistance ON states with a resistance contrast of at least 10,000, for a relatively long period.

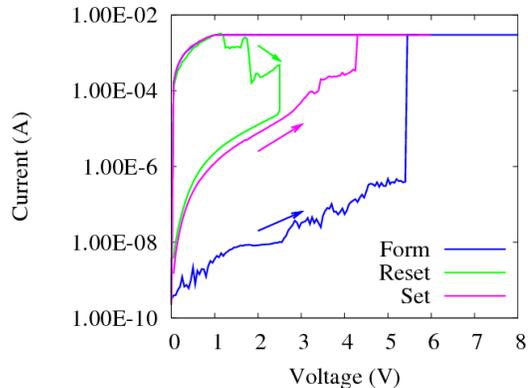


Fig. 4. Experimental I - V characteristics of a typical SiO_x RRAM structure, for unipolar switching.

4.2. Time-to-Failure Tests

The first step in verifying our KMC simulator model is to reconstruct established data related to time-to-failure (TF) in thin layers, based on pristine silica and (for the sake of comparison) hafnia. For this purpose we employ the vacancy generation parameters described in work by McPherson *et al.* [27]; the activation energy and field acceleration parameter for SiO_2 (HfO_2) are taken to be

1eV (1.55eV) and 3.5cm/MV (15.4cm/MV), respectively. Figure 5 shows the variation of the TF with the applied electric field, at 300K, as obtained from our simulations (for a 10nm oxide structure) and published results in Ref. [27]. As can be observed, very good agreement is obtained for both material systems.

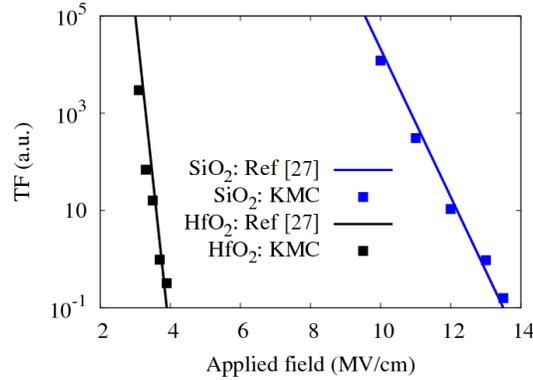


Fig. 5. Time-to-failure using our model, and the data/parameters presented in [27], for both SiO₂ and HfO₂.

4.3. Simulated Characteristics

Figure 6 shows the simulated I - V characteristics (bipolar mode) of an example structure (50nm x 50nm x 10nm simulation volume) and the corresponding local peak temperatures, using a bias ramping rate of 0.2V/ μ s. The simulator reconstructs correctly the memristive I - V characteristics, including the electroforming, set and reset processes, in agreement with the experimental trends [1]. The peak temperature follows the same trend, reaching values as high as 450K after a conductive filament is formed and the device is at a low-resistance state (LRS). It is noteworthy that the I - V characteristics calculated in this paper are from the first cycle after the forming of the conductive filament. Due to the stochastic nature of charge transport in the device, the I - V characteristics (and hence the effective resistance) varies from one cycle to another [40]. The stochastic nature of transport is very well captured by the KMC approach. The dependence of the I - V characteristics on the number of testing cycles was illustrated experimentally by the authors in Ref. [26] (up to 150 cycles); results show visible variation of the effective resistance at both the LRS and HRS states with a resistance resolution of up to 1,000. In general, the extent of such dependence depends on several factors, such as the device structure and geometry, operation mode (unipolar or bipolar), and bias sweeping rate. Detailed analysis of such dependence is beyond the scope of this paper, but will be performed in forthcoming publications.

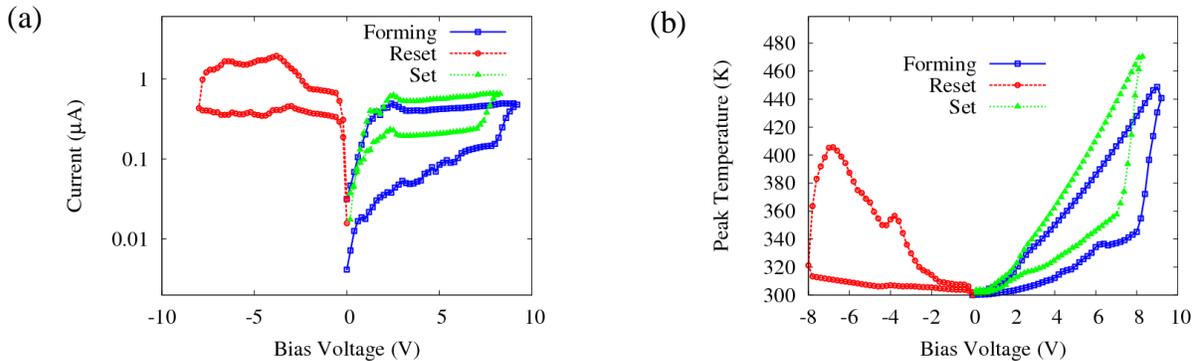


Fig. 6. (a) I - V characteristics, showing the forming, set and reset processes, for an arbitrary initial vacancy distribution. We apply a current compliance limit of 10^{-6} A. (b) Variation of the peak temperature. The bias ramping rate is 0.2V/ μ s.

Figure 7 shows temperature profiles in the oxide layer, demonstrating heat generation and diffusion during switching, as the conductive filament is constructed during the ‘electroforming’ process, ruptured during the ‘reset’ process, and reconstructed once more during the ‘set’ process. While the peak temperature occurs within the conductive filament region, the local temperature can still be high outside the filament due to the heat diffusion phenomenon. As expected, self-heating plays an important role, especially during forming and the on-state. The peak temperature can reach values as high as 450K, in spite of the relatively low currents flowing through the oxide and the reduced power consumption. Indeed, self-heating effects cannot be ignored because of two main reasons: (i) the very high current densities through the created percolation paths and (ii) the low thermal conductivity of the oxide, all leading to the observed high operating temperatures.

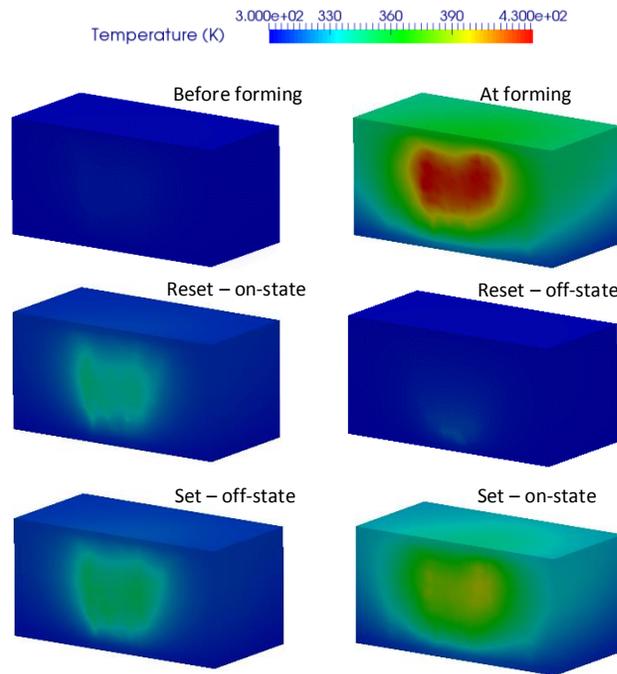


Fig. 7. Temperature map snapshots in the oxide layer, taken to show heat diffusion during the switching processes, for a structure with arbitrary initial vacancy distribution.

To demonstrate the dynamic nature of heat flow, we show in Fig. 8 the variation of the local peak temperature with time, for different biasing conditions: (i) at a low bias before the forming of the CF, (ii) at a high bias where individual vacancies start to form, and (iii) at around the forming bias where a continuous generation of vacancy-ion pairs occurs leading to the CF creation. Fig. 8 shows very short spikes in temperature, resulting from the ionic currents occurring when vacancy-ion pairs are created, moving relatively quickly to the anode. At a low bias, the temperature is $\sim 300\text{K}$, as the device current is very low. The peak temperature starts to increase in a modest fashion, as bias is increased and more vacancies (conductive channels) are generated. At a high bias, before the forming of the CF, several vacancy-ion pairs are generated but the overall temperature stays low, as no fully-formed conductive paths are present between the two electrodes. At around the forming bias and as time progresses, more vacancies are created, and the average peak temperature

increases gradually due to the presence of more vacancies facilitating electron transport via trap-assisted tunneling. The peak temperature reaches a maximum value when the conductive filament is completely formed.

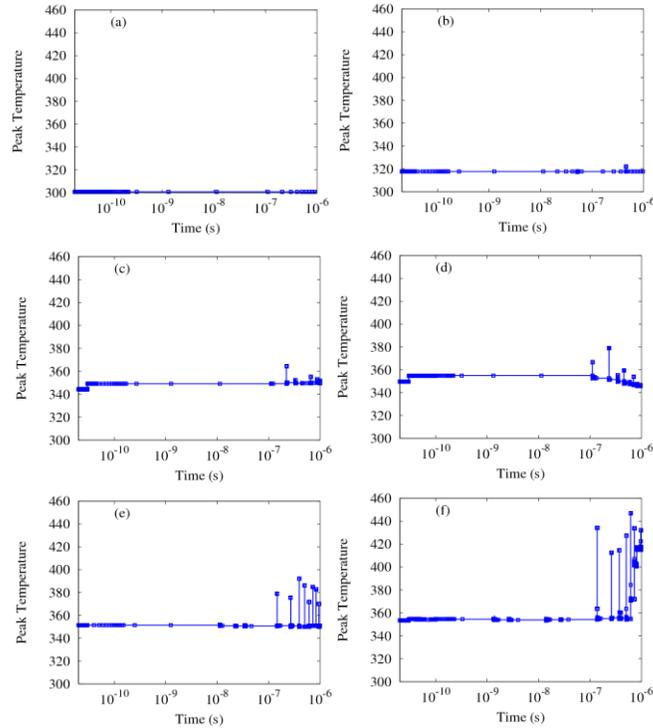


Fig. 8. Variation of the peak temperature with time, as bias is increased (from top to bottom) leading to the creation of the conductive filament.

4.4. Impact of Intrinsic Defects

We compare switching in two different structures: (i) a SiO_2 structure with a very low initial vacancy concentration and (ii) a SiO_x structure with a Si-rich (high initial concentration) volume. Figs. 9 and 10 show the vacancy distributions for both structures, as bias is increased to form the conductive filament. For the SiO_2 structure, almost no vacancies are generated at low biases (e.g. 0.2V). As bias is increased (e.g. 6V), more vacancies are generated and filament seeds appear. The seeds start to grow as bias is increased, and at $\sim 7\text{V}$, an accelerated generation of oxygen vacancies occurs and forms a complete conductive filament, bridging the two electrodes. The same process occurs for the Si-rich structure, but the filament creation occurs at lower biases; This is because (as explained in section 3.1) as oxygen vacancies occupied by two electrons result in lowering the activation energy for ion-vacancy generation E_a , defect-rich areas (e.g. in the form of perpendicular columns – as discussed in Ref. [1]) facilitate the creation of a CF at lower applied biases. For the SiO_2 structure, higher forming biases increase the possibility of hard breakdown and hence irreversible ON/OFF transitions. Figs. 9 and 10 illustrate the 3D nature of conductive filaments, which highlights the necessity of using 3D simulators to predict correctly switching and device characteristics.

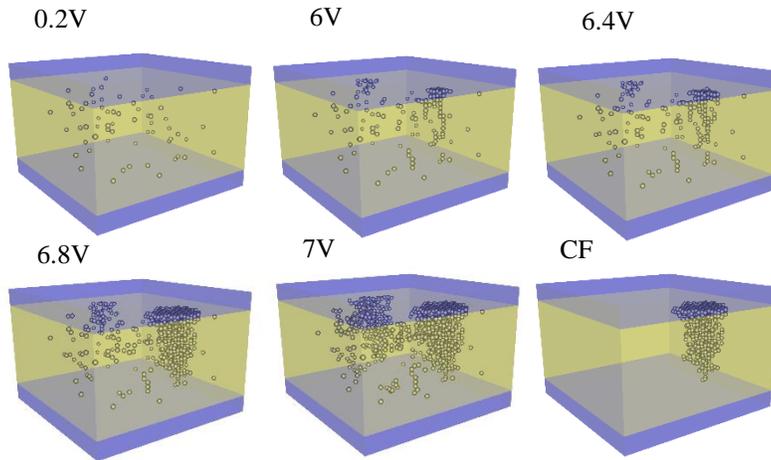


Fig. 9: Vacancy distributions for the pristine (SiO_2) structure with low initial vacancy concentrations, as bias voltage is increased up to the forming bias value of $\sim 7\text{V}$. The figure labeled ‘CF’ illustrates the strongest percolation paths, which are identified using Dijkstra algorithm.

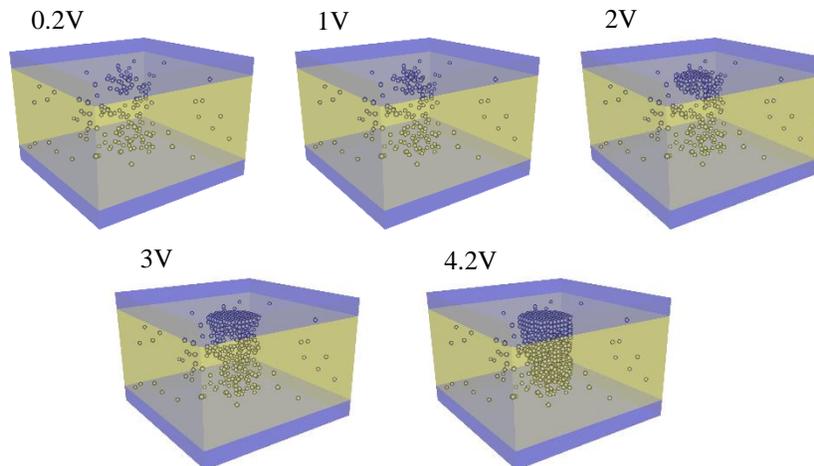


Fig. 10: Vacancy distributions as bias is increased, to form the CF in the silicon-rich silica structure incorporating a defect-rich volume in the form of a column.

5. CONCLUSION

We employed a self-consistent 3D electrothermal KMC simulator to explore resistance switching in silicon-rich silica (SiO_x) RRAM devices. The results reinforced the hypothesis that switching is an intrinsic property of the SiO_x layer, as a result of the forming and rupture of conductive filaments in the highly sub-stoichiometric oxide. We demonstrated the impact of self-heating effects, the role of the initial vacancy distributions acting as precursors for switching, and also the necessity of 3D physical modelling to predict correctly the switching phenomena. The developed simulator provides new insight into RRAM device physics, and could prove useful in facilitating efficient designs in terms of performance, variability and reliability in RRAM devices, and circuits in general.

ACKNOWLEDGEMENT

This work is funded by The Engineering and Physical Sciences Research Council (EPSRC–UK) under grant agreement EP/K016776/1.

References

- [1] A. Mehonic, S. Cuff, M. Wojdak, S. Hudziak, O. Jambois, C. Labbé, B. Garrido, R. Rizk and A. J. Kenyon, “Resistive switching in silicon sub-oxide films,” *J. Appl. Phys.*, vol. 111, pp. 074 507–1–9, April 2012.
- [2] L. Chua, “Resistance switching memories are memristors,” *Appl. Phys. A*, vol. 102, pp. 765–783, January 2011.
- [3] M. Buckwell, L. Montesi, A. Mehonic, O. Reza, L. Garnett, M. Munde, S. Hudziak, and A. J. Kenyon, “Microscopic and spectroscopic analysis of the nature of conductivity changes during resistive switching in silicon-rich silicon oxide,” *physica status solidi (c)*, vol. 12, pp. 211–217, January 2015.
- [4] A. Mehonic, A. Vrajitoarea, S. Cuff, S. Hudziak, H. Howe, C. Labbe, R. Rizk, M. Pepper, and A. J. Kenyon, “Quantum conductance in silicon oxide resistive memory devices,” *Scientific Reports*, vol. 3, pp. 2708–1–7, September 2013.
- [5] A. Mehonic, S. Cuff, M. Wojdak, S. Hudziak, C. Labbé, R. Rizk, A. J. Kenyon, “Electrically tailored resistance switching in silicon oxide,” *Nanotechnology*, vol. 23, no 45, pp. 455 201–1–9, October 2012.
- [6] J. Yao, L. Zhong, D. Natelson and J. M. Tour, “In situ imaging of the conducting filament in a silicon oxide resistive switch,” *Nanotechnology*, vol. 2, pp. 242–1–5, January 2012.
- [7] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, and J. Grollier, “A ferroelectric memristor,” *Nat. Mater.*, vol. 11, pp. 860–864, September 2012.
- [8] J. Yao, L. Zhong, D. Natelson, and J. M. Tour, “Intrinsic resistive switching and memory effects in silicon oxide,” *Applied Physics A*, vol. 102, pp. 835–839, January 2011.
- [9] S. Yu, X. Guan, and H.-S. P. Wong, “On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization,” in *In Electron Devices Meeting (IEDM), 2011 IEEE International*, December 2011, pp. 17.3.1-4.
- [10] R. E. Simpson, P. Fons, A. V. Kolobov, T. Fukaya, M. Krbal, T. Yagi, and J. Tominaga, “Interfacial phase-change memory,” *Nature Nanotechnology*, vol. 6, pp. 501–505, July 2011.
- [11] J. Yao, Z. Sun, L. Zhong, D. Natelson, and J. M. Tour, “Resistive switches and memories from silicon oxide,” *Nano Lett.*, vol. 10, pp. 4105–4110, August 2010.
- [12] “The ITRS 2010 report,” [http://http://www.itrs.net/](http://www.itrs.net/).
- [13] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” *Nature*, vol. 453, pp. 80–83, March 2008.
- [14] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D.-W. Kim, C. U. Jung, S. Seo, M.-J. Lee, and T. W. Noh, “Random circuit breaker network model for unipolar resistance switching,” *Advanced Materials*, vol. 20, pp. 1154–1159, March 2008.
- [15] R. Waser and M. Aono, “Nanoionics-based resistive switching memories,” *Nat. Mater.*, vol. 6, no 11, pp. 833–840, November 2007.
- [16] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems." *Nano letters*, vol. 10, no 4, pp. 1297-1301, March 2010.
- [17] Y. V. Pershin and M. Di Ventra. "Experimental demonstration of associative memory with memristive neural networks." *Neural Networks*, vol. 23, no. 7, pp. 881-886, September 2010.
- [18] A. Mehonic and A. J. Kenyon, "Emulating the electrical activity of the neuron using a silicon oxide RRAM cell." *Frontiers in neuroscience*, vol. 10, no 57, pp. 1-10, February 2016.
- [19] L. Chua, “Memristor-the missing circuit element,” *IEEE Trans. Circuit Theory*, vol. 18, no 5, pp. 507–519, September 1971.
- [20] A. Mehonic and A. J. Kenyon, “Resistive Switching in Oxides. In Defects at Oxide Surfaces,” *Springer Series in Surface Sciences*, Springer International Publishing, pp. 401-428, February 2015.
- [21] M. Buckwell, L. Montesi, S. Hudziak, A. Mehonic, A. J. Kenyon. "Conductance tomography of conductive filaments in intrinsic silicon-rich silica RRAM." *Nanoscale*, vol. 7, no 43, pp. 18030-18035, November 2015.

- [22] S. Kim, S.-J. Kim, K. M. Kim, S. R. Lee, M. Chang, E. Cho, Y.-B. Kim, C. J. Kim, U. -I. Chung, and I.-K. Yoo, "Physical electro-thermal model of resistive switching in bi-layered resistance-change memory," *Scientific Reports*, vol. 3, Article number 1680, pp. 1-6, April 2013.
- [23] T. Sadi, L. Wang, D. Gao, A. Mehonic, L. Montesi, M. Buckwell, A. Kenyon, A. Shluger, and A. Asenov, "Advanced Physical Modeling of SiO_x Resistive Random Access Memories", In Proc. Simulation of Semiconductor Processes and Devices (SISPAD), pp. 149–152, September 6-8, 2016, Nuremberg, Germany
- [24] G. C. Jegert, "Modeling of Leakage Currents in High-k Dielectrics", Ph.D. Dissertation, Tech. Univ. Munich, Germany, December 2011.
- [25] L. Vandelli, A. Padovani, L. Larcher, R. G. Southwick, III, W. B. Knowlton, and G. Bersuker, "A Physical Model of the Temperature Dependence of the Current Through SiO₂/HfO₂ Stacks" *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2878–2887, September 2011.
- [26] A. Mehonic, M. Buckwell, L. Montesi, L. Garnett, S. Hudziak, S. Fearn, R. Chater, D. McPhail, and A. J. Kenyon, "Structural changes and conductance thresholds in metal-free intrinsic SiO_x resistive random access memory", *J. Appl. Phys.*, vol. 117, pp. 124505-1-8, March 2015.
- [27] J. McPherson, J.-Y. Kim, A. Shanware, and H. Mogul, "Thermochemical description of dielectric breakdown in high dielectric constant materials" *Appl. Phys. Lett.* vol. 82, pp. 2121-2123, March 2003.
- [28] A. Mehonic, M. Buckwell, L. Montesi, M. S. Munde, D. Gao, S. Hudziak, R. J. Chater, S. Fearn, D. McPhail, M. Bosman, A. L. Shluger, and A. J. Kenyon. "Nanoscale Transformations in Metastable, Amorphous, Silicon-Rich Silica," *Advanced Materials*, vol. 28, 7486–7493, June 2016.
- [29] S. Li, W. Chen, Y. Luo, J. Hu, P. Gao, J. Ye, K. Kang, H. Chen, E. Li, and W.-Y. Yin, "Fully Coupled Multiphysics Simulation of Crosstalk Effect in Bipolar Resistive Random Access Memory" *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3647–3653, Sept. 2017
- [30] D. Ielmini and V. Milo, "Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications" *Journal of Computational Electronics*, vol. 16, no 4, pp. 1121–1143, November 2017.
- [31] M. A. Villena, J. B. Roldán, F. Jiménez-Molinos, E. Miranda, J. Suñé, M. Lanza, "SIM² RRAM: a physical model for RRAM devices simulation" *Journal of Computational Electronics*, vol. 16, no 4, pp 1095–1120, December 2017
- [32] Z. Wei and K. Eriguchi, "Analytic Modeling for Nanoscale Resistive Filament Variation in ReRAM With Stochastic Differential Equation" *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2201 – 2206, May 2017.
- [33] S. Brivio and S. Spiga, "Stochastic circuit breaker network model for bipolar resistance switching memories" *Journal of Computational Electronics*, vol. 16, no. 4, pp. 1154–1166, December 2017.
- [34] A. Mehonic, T. Gerard, and A. J. Kenyon, "Light-activated resistance switching in SiO_x RRAM devices" *Appl. Phys. Lett.*, vol. 111, p. 233502, 2017.
- [35] P. Huang, X.Y. Liu, W.H. Li, Y.X. Deng, B. Chen, Y. Lu, B. Gao, L. Zeng, K.L. Wei, G. Du, X. Zhang, and J.F. Kang, "A Physical Based Analytic Model of RRAM Operation for Circuit Simulation" in *In Electron Devices Meeting (IEDM), 2011 IEEE International*, December 2012, pp. 26.6.1-4.
- [36] A. Makarov, V. Sverdlov and S. Selberherr, "Stochastic model of the resistive switching mechanism in bipolar resistive random access memory: Monte Carlo simulations" *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 29, no. 1, pp. 01AD03-1-5, January 2011.
- [37] T. Sadi, L. Wang, and A. Asenov, "Multi-Scale Electrothermal Simulation and Modelling of Resistive Random Access Memory Devices", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 33–37, September 21-23, 2016, Bremen, Germany.
- [38] M. Saremi, "Carrier mobility extraction method in ChGs in the UV light exposure," *IET Micro & Nano Letters*, vol. 11, no. 11, pp. 762–764, 2016.
- [39] M. Saremi, H. J. Barnaby, A. Edwards and M. N. Kozicki, "Analytical Relationship between Anion Formation and Carrier-Trap Statistics in Chalcogenide Glass Films," *ECS Electrochemistry Letters*, vol. 4, no 7, pp. H29–H31, 2015.
- [40] S. N. Mozaffari, S. Tragoudas, and T. Haniotakis, "More Efficient Testing of Metal-Oxide Memristor-Based Memory," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 6, pp. 1018–1029, June 2017.