The IeMRC Opto-PCB Flagship Project

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Outline

- Electronic versus Optical interconnects
- The OPCB project
- OPCB University Research Overview
  - Heriot Watt
  - Loughborough
  - UCL
- System Demonstrator
Copper Tracks versus Optical Waveguides for High Bit Rate Interconnects

- **Copper Track**
  - EMI Crosstalk
  - Loss
  - Impedance control to minimize back reflections, additional equalisation, costly board material

- **Optical Waveguides**
  - Low loss
  - Low cost
  - Low power consumption
  - Low crosstalk
  - Low clock skew
  - WDM gives higher aggregate bit rate
  - Cannot transmit electrical power
On-board Platform Applications
On-board Platform Applications

Reconfigurable Network Interconnections

RF/EO Sensors & comms data

High Bandwidth Signals
The Integrated Optical and Electronic Interconnect PCB Manufacturing (OPCB) project

- Hybrid Optical and Electronic PCB Manufacturing Techniques

- 8 Industrial and 3 University Partners led by industry end user

- Multimode waveguides at 10 Gb/s on a 19 inch PCB

- Project funded by UK Engineering and Physical Sciences Research Council (EPSRC) via the Innovative Electronics Manufacturing Research Centre (IeMRC) as a Flagship Project

- 2 years into the 3 year, £1.3 million project
Integration of Optics and Electronics

- Backplanes
  - Butt connection of “plug-in” daughter cards
  - In-plane interconnection
- Focus of OPCB project

- Out-of-plane connection
  - 45 mirrors
  - Chip to chip connection possible
Exxelis  
Polymer supply and photolithography

Cadence  
PCB design tools and rules

Dow Corning  
Polymer supply and photolithography

Heriot-Watt University  
Polymer formulation  
Supply of laser written waveguides

UCL  
Optical modelling  
Waveguide design rules  
Optical measurements

Loughborough University  
Laser ablation and ink-jet printing of waveguides

NPL  
Physical Measurements

Stevenage Circuits Ltd  
Sample PCBs, dry film  
CAD conversion, laser work

End Users

Xyratex  
Network storage interconnect

BAE Systems  
In-flight interconnect

Renishaw  
Precision measurement
• **Slotted baseplate** mounted vertically over translation, rotation & vertical stages; components held in place with magnets
• By using two opposing 45° beams we minimise the amount of substrate rotation needed
Writing sharply defined features
– flat-top, rectangular laser spot

Gaussian beam diameter = 1.1 mm

Imaging system / lenses

60 μm square aperture

TEM$_{00}$

Gaussian Beam
Imaged aperture

Images of the resulting waveguide core cross-sections
Laser written polymer structures

SEM images of polymer structures written using imaged 50 µm square aperture (chrome on glass)

- Writing speed: ~75 µm / s
- Optical power: ~100 µW
- Flat-top intensity profile
- Oil immersion
- Single pass

Optical microscope image showing end on view of the 45° surfaces
Waveguide terminated with 45-deg mirror

Out-of-plane coupling, using 45-deg mirror (silver)

Microscope image looking down on mirror coupling light towards camera

OPTICAL INPUT
Current Results

Laser-writing Parameters:
- Intensity profile: Gaussian
- Optical power: ~8 mW
- Cores written in oil

Polymer:
- Custom multifunctional acrylate photo-polymer
- Fastest “effective” writing speed to date: 50 mm/s

(Substrate: FR4 with polymer undercladding)
Large Board Processing: Writing

- Stationary “writing head” with board moved using Aerotech sub-μm precision stages
- Waveguide trajectories produced using CAD program

- 600 x 300 mm travel
- Requires a minimum of 700 x 1000 mm space on optical bench
- Height: ~250 mm
- Mass:
  - 300 mm: 21 kg
  - 600 mm: 33 kg
- Vacuum tabletop
The spiral was fabricated using a Gaussian intensity profile at a writing speed of 2.5 mm/s on a 10 x 10 cm lower clad FR4 substrate. Total length of spiral waveguide is \(~1.4 \text{ m}\). The spiral was upper cladded at both ends for cutting.
Laser Ablation for Waveguide Fabrication

- Ablation to leave waveguides
- Excimer laser – Loughborough
- Nd:YAG – Stevenage Circuits

![Diagram of FR4 PCB with layers and laser ablation process]

Deposit cladding and core layers on substrate

SIDE VIEW

FR4 PCB

Laser ablate polymer

Deposit cladding layer
Nd:YAG Ablation

- Nd:YAG laser based at Stevenage Circuits
- Grooves machined in optical polymer and ablation depth characterised for machining parameters
- Initial waveguide structures prepared
Excimer Laser Ablation

- Straight structures machined in polymer
- Future work to investigate preparation of curved mirrors for out of plane interconnection
Inkjetting as a Route to Waveguide Deposition

- Print polymer then UV cure
- Advantages:
  - controlled, selective deposition of core and clad
  - less wastage: picolitre volumes
  - large area printing
  - low cost

Deposit Lower Cladding
Deposit Core
Deposit Upper Cladding
Challenges of Inkjet Deposition

- Viscosity tailored to inkjet head via addition of solvent
- “Coffee stain” effects

![Graph showing viscosity vs. temperature for two solvents](image)

- Cross-section of dried droplet “coffee-stain” effect
- A 4x4 array of inkjet printed drops
Changing Surface Wettability

Contact Angles

Core material on cladding

Core material on modified glass surface (hydrophobic)

Large wetting - broad inkjetted lines

Reduced wetting – discrete droplets

Identical inkjetting conditions - spreading inhibited on modified surface
Towards Stable Structures

Stable line structures with periodic features

Cross section of inkjetted core material surrounded by cladding (width 80 microns)

A balance between wettability, line stability and adhesion
Waveguide components and measurements

- Straight waveguides 480 mm x 70 µm x 70 µm
- Bends with a range of radii
- Crossings
- Spiral waveguides
- Tapered waveguides
- Bent tapered waveguides
- Loss
- Crosstalk
- Misalignment tolerance
- Surface Roughness
- Bit Error Rate, Eye Diagram
Optical Power Loss in 90° Waveguide Bends

- Radius $R$, varied between $5.5 \text{ mm} < R < 35 \text{ mm}$, $\Delta R = 1 \text{ mm}$
- Light lost due to scattering, transition loss, bend loss, reflection and back-scattering
- Illuminated by a MM fiber with a red-laser.

Schematic diagram of one set of curved waveguides.

Light through a bent waveguide of $R = 5.5 \text{ mm} – 34.5 \text{ mm}$

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BPM, beam propagation method modeling of optical field in bend segments

\[ w = 50 \mu m, \quad R = 13 \text{ mm} \]

(left picture) in the first segment (first 10°).
(right picture) in the 30° to 40° degree segment.
Differences in misalignment tolerance and loss as a function of taper ratio

• Graph plots the differences between a tapered bend and a bend
• There is a trade off between insertion loss and misalignment tolerance
Crosstalk in Chirped Width Waveguide Array

- Light launched from VCSEL imaged via a GRIN lens into 50 µm x 150 µm waveguide
- Photolithographically fabricated chirped with waveguide array
- Photomosaic with increased camera gain towards left

100 µm 110 µm 120 µm 130 µm 140 µm 150 µm
Surface roughness

- RMS side wall roughness: 9 nm to 74 nm
- RMS polished end surface roughness: 26 nm to 192 nm.
Design rules for waveguide width depending on insertion loss and cross-talk

6~7dB for a 70 μm width waveguide

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Bit error rate for laterally misaligned 1550 nm 2.5 Gb/s DFB laser

(-) Direction

Power at the receiver (dBm)

(+ ) Direction

Power at the receiver (dBm)

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Contour map of VCSEL and PD misalignment

(a) Contour map of relative insertion loss compared to the maximum coupling position for VCSEL misalignment at $z = 0$.

- Dashed rectangle is the expected relative insertion loss according to the calculated misalignments along $x$ and $y$.
- The minimum insertion loss was 4.4 dB, corresponded to $x = 0, y = 0, z = 0$.

(b) Same for PD misalignment at $z = 0$. Resolution step was $\Delta x = \Delta y = 1 \, \mu m$. 

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Coupling Loss for VCSEL and PD for misalignments along optic axis

VCSEL

Photo Detector

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Fabrication Techniques and Waveguides Samples

Straight waveguides – Optical InterLinks

90° Crossings – Dow Corning

90° Crossings – Heriot Watt University

50° Crossings – Exxelis

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Photolithographic Fabrication of Waveguides

UV Exposure → ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ 50 μm
Lower cladding → FR4

UV Exposure → ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ 50 μm
Mask → FR4

Spacer → Core layer

250 μm → 50 μm → 50 μm → 50 μm
Waveguide → FR4

UV Exposure → ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ 50 μm
Upper cladding → FR4

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Optical Loss Measurement

850 nm VCSEL

Index matching fluid
70 μm pinhole

50/125 μm step index fibre

mode scrambler

Integrating sphere photodetector

0 dBm
-1.63 dBm

nW Power Meter

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VCSEL Array for Crosstalk Measurement

Source: Microsemi Corporation

Source: ULM Photonics GmbH

Source: GRINTech GmbH

MT compatible interface
Design Rules for Inter-waveguide Cross Talk

- 70 μm × 70 μm waveguide cross sections and 10 cm long
- In the cladding power drops linearly at a rate of 0.011 dB/μm
- Crosstalk reduced to -30 dB for waveguides 1 mm apart

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Schematic Diagram Of Waveguide Crossings at 90° and at an Arbitrary Angle, $\theta$
Design Rules for Arbitrary Angle Crossings

- Loss of 0.023 dB per 90° crossing consistent with other reports
- The output power dropped by 0.5% at each 90° crossing
- The loss per crossing ($L_c$) depends on crossing angle ($\theta$), $L_c=1.0779 \cdot \theta^{-0.8727}$. 
Loss of Waveguide Bends

<table>
<thead>
<tr>
<th>Width (μm)</th>
<th>Optimum Radius (mm)</th>
<th>Maximum Power (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>13.5</td>
<td>-0.74</td>
</tr>
<tr>
<td>75</td>
<td>15.3</td>
<td>-0.91</td>
</tr>
<tr>
<td>100</td>
<td>17.7</td>
<td>-1.18</td>
</tr>
</tbody>
</table>
System Demonstrator

Fully connected waveguide layout using design rules
# Power Budget

<table>
<thead>
<tr>
<th>Input power (dBm/mW)</th>
<th>-2.07 / 0.62</th>
</tr>
</thead>
</table>

## Bend 90°

<table>
<thead>
<tr>
<th>Radii (mm)</th>
<th>15.000</th>
<th>15.250</th>
<th>15.500</th>
<th>15.725</th>
<th>16.000</th>
<th>16.250</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss per bend (dB)</td>
<td>0.94</td>
<td>0.91</td>
<td>0.94</td>
<td>0.94</td>
<td>0.95</td>
<td>0.95</td>
</tr>
</tbody>
</table>

## Crossings

<table>
<thead>
<tr>
<th>Crossing angles (°)</th>
<th>22.27</th>
<th>29.45</th>
<th>36.23</th>
<th>42.10</th>
<th>47.36</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss per crossing (dB)</td>
<td>0.078</td>
<td>0.056</td>
<td>0.047</td>
<td>0.041</td>
<td>0.037</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Min. detectable power (dBm)</th>
<th>-15 / 0.03</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Min. power no bit error rate</th>
<th>-12 / 0.06</th>
</tr>
</thead>
</table>
Demonstrator Dummy Board
The Shortest Waveguide Illuminated by Red Laser
Waveguide with 2 Crossings Connected 1\textsuperscript{st} to 3\textsuperscript{rd} Linecard Interconnect
Output Facet of the Waveguide Interconnection
Backplane and Line Cards Orthogonal

Optical Backplane Connection Architecture

- Lens Interface
- Backplane
- Connector housing
- Parallel optical transceiver
- Copper layers
- FR4 layers
- Optical layer
Butt-coupled connection approach without 90º deflection optics
Hybrid Electro-Optical Printed Circuit Board

- Standard Compact PCI backplane architecture
- 12 electrical layers for power and C-PCI signal bus and peripheral connections
- Electrical C-PCI connector slots for SBC and line cards
- 1 polymeric optical layer for high speed 10 GbE traffic
- 4 optical connector sites
- Dedicated point-to-point optical waveguide architecture

Optical connector site

Compact PCI slot for single board computer

Compact PCI slots for line cards
Hybrid Electro-Optical Printed Circuit Board

- Standard Compact PCI backplane architecture
- 12 electrical layers for power and C-PCI signal bus and peripheral connections
- Electrical C-PCI connector slots for SBC and line cards
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- 4 optical connector sites
- Dedicated point-to-point optical waveguide architecture
**Parallel optical transceiver circuit**
- Small form factor quad parallel optical transceiver
- Microcontroller supporting $I^2C$ interface
- Samtec “SEARAY™” open pin field array connector
- Spring loaded platform for optical engagement mechanism
- Custom heatsink for photonic drivers

**Backplane connector module**
- Samtec / Xyratex collaborate to develop optical PCB connector
- 1 stage insertion engagement mechanism developed
- Xyratex transceiver integrated into connector module
Engagement process

- Optical transceiver interface floats
- Backplane receptacle “funnels” connector
- Cam followers force optical interface up
- Optical transceiver lens butt-couples to backplane lens
HIGH SPEED SWITCHING LINE CARD

- XFP ports
- 8 x 8 Crosspoint switch
- SMP connector sites
- Array connector for pluggable active optical connector
- FPGA
- Compact PCI bus connector
- PCI Bridge
- Transceiver programming port
Demonstrator with Optical Interconnects
Demonstration Assembly

- Electro-optical backplane
- Pluggable optical backplane connectors
- Compact PCI chassis
- High speed switch line cards
- XFP front end
- Single board computer
GUI control interface

- Remote admin
- XFP control
- Crosspoint switch configuration
- Full transceiver control (VCSEL/PIN settings)
- Selectable between any line card in system
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