Design and implementation of an electro-optical backplane with pluggable in-plane connectors

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Overview

- Design challenges in data storage systems
- Electro-optical backplane with polymer waveguides
- Active in-plane optical backplane connector
- Demonstration platform
Design challenges in modern data storage systems

Source: IDC, 2007
Data storage protocol and form factor trends

Disk drive form factors decreasing

- 3.5” HDD
- 2.5” HDD
- 2.5” SSD
- 1.8” SSD

Data storage interconnect speeds increasing

- 3Gb/s SAS
- 6Gb/s SAS
- 12Gb/s SAS

Source: SCSI Trade Association Sep 08 | www.scsita.org
Data storage array backplane topology

**Redundant dual star architecture**

- Data storage devices
- Controller modules
- Midplane interconnect
Design and performance constraints
Design and performance constraints

- Decreasing form factors cause increase in density
- Increasing interconnect data rates on midplane
Design and performance constraints

- Copper layers for power distribution
- Copper layers for low speed communication
- Optical layers for high speed communication
Electro-optical backplane with polymer waveguides

Source: Exxelis
Optical polymer

- Low loss at 850 nm

Waveguide characteristics

- $n_{core} = 1.56$
- $n_{cladding} = 1.524$
- $\Delta n = 2.3\%$
- N.A. = 0.33

Core dimensions

- Cross-section = 70 $\mu$m x 70 $\mu$m
- Pitch (centre) = 250 $\mu$m
Optical interconnect design

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**Bends**
- RoC = 17 mm
- Negative and positive cascades

**Min. Pitch**
- 250 μm

**Waveguide layout**
- UCL
- Xyratex
- IBM Zurich

**Crossovers**
- Non-orthogonal
- 130° to 160°
Electro-optical PCB fabrication process

1. Deposit lower refractive index polymer (cladding) onto substrate surface
2. Cure polymer layer with exposure to ultra-violet light to harden
3. Deposit higher refractive index (core) polymer onto lower cladding layer
4. Align UV laser write head into position
5. Activate laser and move write head to pattern waveguide features in core layer
6. Remove uncured portions of the core layer
7. Deposit lower refractive index polymer onto patterned core layer
8. Cure upper cladding layer with UV light

Polyimide Substrate

Upper cladding
Core layer
Lower cladding

Waveguides

UV Exposure

Embedded Optical Interconnect in Data Storage Domain
Richard Pitwon
Electro-optical midplane

- Multilayer electro-optical PCB
- Compact PCI bus connectors
- Optical connector sites
Passive alignment and assembly

Mechanical registration features

- Deposit lower cladding layer
- Deposit core layer
- Pattern core layer including registration waveguides
- Deposit upper cladding layer
- Remove part of upper cladding for mechanical access
- Align MT compliant receptacle with microlens array
Optical connector receptacles

Primary receptacle
- Low tolerance
- Pluggable connector

Secondary receptacle
- High tolerance
- Lens holder
- MT compliant

Electro-optical midplane

Microlens array
- MT compliant

Connector site
Alignment stubs
Waveguide insertion loss measurements

- Measured loss without index matching fluid
- Measured loss with index matching fluid
- Calculated loss

![Waveguides sorted by length](image.png)
Active optical backplane connector
Optical backplane connection architecture

Orthogonal docking of line cards

- Lens Interface
- Backplane
- Connector housing
- Parallel optical transceiver
- Copper layers
- FR4 layers
- Optical layer

 SPIE Photonics West 2010
Opto: 7607-18
Optical backplane connection architecture

Butt coupled connection without 90° deflection

Single waveguide illuminated
Parallel optical transceiver

- Mechanically flexible optical platform
- MT compatible optical interface
- Geometric microlens array
- Quad VCSEL driver and TIA/LA
- VCSEL / PIN arrays on pre-aligned frame
ACTIVE PLUGGABLE OPTICAL CONNECTOR

Parallel Optical Transceiver

- Spring loaded platform

Microcontroller

Connector Module

SPIE Photonics West 2010
Opto: 7607-18
- Cam followers guided along cam track
- Allows for orthogonal movement of optical platform
- Ramped plug for reversible connection
Optical backplane connection architecture
Dual lens coupling interface

**Free space coupling arrangement**
- Optimised for loss minimisation
- Maximum beam expansion

**VCSEL**
- $\lambda = 850\text{nm}$
- $\Theta = 7\mu\text{m}$
- Div = $25^\circ$

**PIN**
- $\lambda = 850\text{nm}$
- $\Theta = 70\mu\text{m}$

**Predicted interface loss:**
- 0.72 dB
- 1.11 dB

**Polymer waveguides**
- $\Theta = 70\mu\text{m} \times 70\mu\text{m}$
- $n_{\text{core}} = 1.56$
- $n_{\text{cladding}} = 1.524$
- NA = 0.33

**Dual lens coupling solution**
- Beam expansion at coupling interface
- Reduces susceptibility to contamination
Demonstration assembly
Demonstration platform with peripheral test cards

- Electro-optical backplane
- Pluggable optical connectors
- Compact PCI chassis
- High speed switch line cards
- XFP front end
- Single board computer
Demonstration assembly

Procedure

- 10 GbE LAN test traffic @ 10.3 Gb/s into demo front end (1st line card)

- Data passed across pluggable connectors and optical backplane

- Data retrieved through front end of 2nd line card
High speed data transmission measurements

Procedure

- 10 GbE LAN test traffic @ 10.3 Gb/s into demo front end (1\textsuperscript{st} line card)
- Data passed across pluggable connectors and optical backplane
- Data retrieved through front end of 2\textsuperscript{nd} line card

Results

- Test data captured with typical peak to peak jitter ~30ps (after front end CDR)
- Total optical waveguide interconnect loss ranges from -6 dB to -13 dB
Acknowledgements

Will write something here

EPSRC
DTI
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Thank you for your attention

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